EVALUATION KIT AVAILABLE

MAX5073

2.2MHz, Dual-Output Buck or Boost Converter with Internal Power MOSFETs

General Description

The MAX5073 is a dual-output DC-DC converter with integrated high-side n-channel power MOSFETs. Each output can be configured either as a buck converter or a boost converter. The device is capable of operating from a wide 5.5V to 23V input voltage range. Each output is programmable down to 0.8V in the buck mode and up to 28V in the boost mode with an output voltage accuracy of ±1%. In the buck mode, converter 1 and converter 2 can deliver 2A and 1A, respectively. The output switching frequency of each converter can be programmed from 200kHz to 2.2MHz to avoid harmonics in a radio power supply or to reduce the size of the power supply. Each output operates 180° out-of-phase thus reducing input-capacitor ripple current, size, and cost. A SYNC input facilitates external frequency synchronization. Moreover, a CLKOUT output provides out-of-phase clock signal with respect to converter 2, allowing four-phase operation using two MAX5073 ICs in master-slave configuration.

The MAX5073 includes an internal digital soft-start that reduces inrush current, eliminates output-voltage overshoot, and ensures monotonic rise in output voltage during power-up. The device includes individual shutdown and a power-good output for each converter. Protection features include output short-circuit protection for buck mode and maximum duty-cycle limit for boost operation, as well as thermal shutdown.

The MAX5073 is available in a thermally enhanced 28-pin thin QFN package that can dissipate 2.7W at +70°C ambient temperature. The device is rated for operation over the -40°C to +85°C extended, or -40°C to +125°C automotive temperature range.

Applications

- Point-of-Load DC-DC Converters
- Telecom Line Card
- Networking Line Card
- Power-Over-Ethernet Postregulation for PDs

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE
MAX5073ETI	-40°C to +125°C	28 Thin QFN-EP* (5mm x 5mm)	T2855-6
MAX5073ETI+	-40°C to +125°C	28 Thin QFN-EP* (5mm x 5mm)	T2855-6

**EP = Exposed pad.*

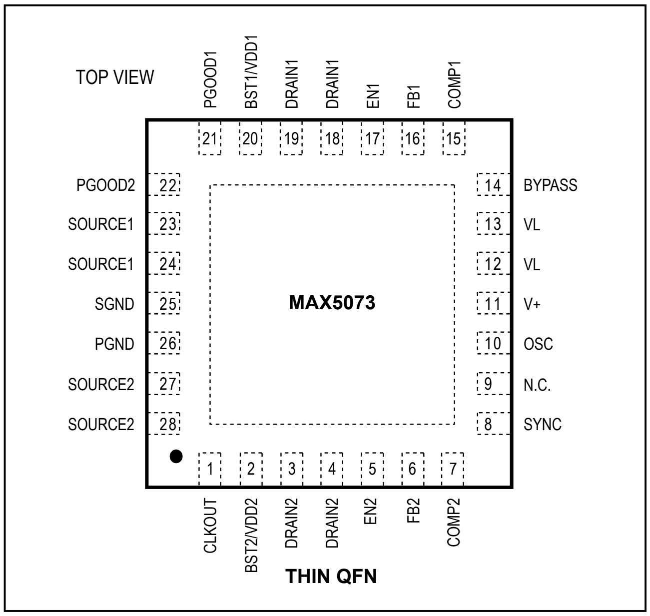
+Denotes lead-free package.

***Ordering Information* continued at end of data sheet.**

Features

- 4.5V to 5.5V or 5.5V to 23V Input Supply Voltage Range
- 0.8V (Buck) to 28V (Boost) Output Voltage
- Two Independent Output DC-DC Converters with Internal Power MOSFETs
- Each Output can be Configured in Buck or Boost Mode
- I_{OUT1} and I_{OUT2} of 2A and 1A (Respectively) in Buck Mode
- 180° Out-of-Phase Operation
- Clock Output for Four Phase Operation
- Switching Frequency Programmable from 200kHz to 2.2MHz
- Digital Soft-Start and Sync Input
- Individual Converter Shutdown and Power-Good Output
- Short-Circuit Protection (Buck)/Maximum Duty-Cycle Limit (Boost)
- Thermal Shutdown
- Thermally Enhanced 28-Pin Thin QFN Package Dissipates up to 2.7W at +70°C

Pin Configuration



19-3504; Rev 3; 5/14

Absolute Maximum Ratings

V+ to PGND ....-0.3V to +25V
SGND to PGND..-0.3V to +0.3V
VL to SGND.................-0.3V to the lower of +6V or (V+ + 0.3V)
BST1/VDD1, BST2/VDD2, DRAIN_, PGOOD2, PGOOD1 to
SGND ....-0.3V to +30V
BST1/VDD1 to SOURCE1,
BST2/VDD2 to SOURCE2 ....-0.3V to +6V
SOURCE_ to SGND...-0.6V to +25V
EN_ to SGND...-0.3V to (VL to +0.3V)
CLKOUT, BYPASS, OSC, COMP1,
COMP2, SYNC, FB_ to SGND................-0.3V to (VL + 0.3V)
SOURCE1, DRAIN1 Peak Current ....5A for 1ms
SOURCE2, DRAIN2 Peak Current ....3A for 1ms
VL, BYPASS to SGND Short Circuit ....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN (derate 21.3mW/°C above +70°C).. 2758mW*
Package Junction-to-Case Thermal Resistance (θ_{JC})......2°C/W
Operating Temperature Ranges:
MAX5073ETI (T_{MIN} to T_{MAX})......................... -40°C to +85°C
MAX5073ATI (T_{MIN} to T_{MAX})....................... -40°C to +125°C
Junction Temperature...+150°C
Storage Temperature Range............................ -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
**As per JEDEC51 standard*.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V+ = VL = 5.2V or V+ = 5.5V to 23V, EN_ = VL, SYNC = GND, I_{VL} = 0mA, PGND = SGND, C_{BYPASS} = 0.22µF, C_{VL} = 4.7µF (ceramic), R_{OSC} = 10kΩ (circuit of Figure 1), $T_A = T_J = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS						
Input Voltage Range	V+	(Note 2)	5.5		23.0	V
		VL = V+	4.5		5.5	
Operating Supply Current	I_Q	VL unloaded, no switching, $V_{FB\_}$ = 1V, V+ = 12V, R_{OSC} = 60kΩ		2.2	4	mA
V+ Standby Supply Current	I_{STBY}	EN_ = 0, PGOOD_ floating, V+ = 12V, R_{OSC} = 60kΩ (MAX5073ETI)		0.6	1.2	mA
		EN_ = 0, PGOOD_ floating, V+ = 12V, R_{OSC} = 60kΩ (MAX5073ATI)		0.6	1.4	
Efficiency	η	V_{OUT1} = 3.3V at 1.5A, V_{OUT2} = 2.5V at 0.75A (f_{SW} = 1.25MHz), V+ = VL = 5V		82		%
		V+ = 12V		80		
		V+ = 16V		78		
STARTUP/VL REGULATOR						
VL Undervoltage Lockout Trip Level	UVLO	VL falling	3.95	4.1	4.25	V
VL Undervoltage Lockout Hysteresis				175		mV
VL Output Voltage	VL	V+ = 5.5V to 23V, I_{SOURCE} = 0 to 40mA	4.9	5.2	5.5	V
BYPASS OUTPUT						
BYPASS Voltage	V_{BYPASS}	I_{BYPASS} = 0, R_{OSC} = 60kΩ (MAX5073ETI)	1.98	2.00	2.02	V
		I_{BYPASS} = 0, R_{OSC} = 60kΩ (MAX5073ATI)	1.975	2.00	2.025	
BYPASS Load Regulation	ΔV_{BYPASS}	$0 \le I_{BYPASS} \le 50\mu A$, R_{OSC} = 60kΩ	0	2	10	mV
SOFT-START						
Digital Ramp Period		Internal 6-bit DAC		2048		f_{OSC} clock cycles
Soft-Start Steps				64		Steps

Electrical Characteristics (continued)

(V+ = VL = 5.2V or V+ = 5.5V to 23V, EN_ = VL, SYNC = GND, I_{VL} = 0mA, PGND = SGND, C_{BYPASS} = 0.22µF, C_{VL} = 4.7µF (ceramic), R_{OSC} = 10kΩ (circuit of Figure 1), T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE-ERROR AMPLIFIER						
FB_ Input Bias Current	$I_{B(EA)}$				250	nA
FB_ Input Voltage Set Point		0°C ≤ T_A ≤ +70°C	0.792	0.8	0.808	V
		-40°C ≤ T_A ≤ +85°C	0.788	0.8	0.812	
		-40°C ≤ T_J ≤ +125°C (MAX5073ATI only)	0.788	0.8	0.812	
FB_ to COMP_ Transconductance	gM	0°C to +85°C	1.25	2	2.70	mS
		40°C to +85°C	1.2	2	2.9	
		-40°C to +125°C (MAX5073ATI only)	1.2	2	2.9	
INTERNAL PMOSFETS						
On-Resistance Converter 1	R_{ON1}	I_{SWITCH} = 100mA, V_{BST1}/V_{DD1} to $V_{SOURCE1}$ = 5.2V (MAX5073ETI)		195	290	mΩ
		I_{SWITCH} = 100mA, V_{BST1}/V_{DD1} to $V_{SOURCE1}$ = 5.2V (MAX5073ATI)		195	330	
		I_{SWITCH} = 100mA, V_{BST1}/V_{DD1} to $V_{SOURCE1}$ = 4.5V (MAX5073ETI)				
		I_{SWITCH} = 100mA, V_{BST1}/V_{DD1} to $V_{SOURCE1}$ = 4.5V (MAX5073ATI)				
On-Resistance Converter 2	R_{ON2}	I_{SWITCH} = 100mA, V_{BST2}/V_{DD2} to $V_{SOURCE2}$ = 5.2V		330	630	mΩ
		I_{SWITCH} = 100mA, V_{BST2}/V_{DD2} to $V_{SOURCE2}$ = 4.5V		350	690	
Minimum Converter 1 Output Current	I_{OUT1}	V_{OUT1} = 3.3V, V+ = 12V (Note 3)		2		A
Minimum Converter 2 Output Current	I_{OUT2}	V_{OUT2} = 2.5V, V+ = 12V (Note 3)		1		A
Converter 1 MOSFET Leakage Current	I_{LK1}	EN1 = 0V, V_{DS} = 23V			10	µA
Converter 2 MOSFET Leakage Current	I_{LK2}	EN2 = 0V, V_{DS} = 23V			10	µA
INTERNAL SWITCH CURRENT LIMIT						
Current-Limit Converter 1	I_{CL1}	V+ = 12V (MAX5073ETI)	2.3	3	4.3	A
		V+ = 12V (MAX5073ATI)	2.3	3	4.6	
Current-Limit Converter 2	I_{CL2}	MAX5073ETI	1.38	1.8	2.10	A
		MAX5073ATI	1.38	1.8	2.20	

Electrical Characteristics (continued)

(V+ = VL = 5.2V or V+ = 5.5V to 23V, EN_ = VL, SYNC = GND, I_{VL} = 0mA, PGND = SGND, C_{BYPASS} = 0.22µF, C_{VL} = 4.7µF (ceramic), R_{OSC} = 10kΩ (circuit of Figure 1), $T_A = T_J = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL OSCILLATOR/SYNC						
Maximum Duty Cycle	D_{MAX}	SYNC = SGND, f_{SW} = 1.25MHz	84	86	95	%
		SYNC = SGND, f_{SW} = 2.2MHz	84	86	95	
Switching Frequency Range	f_{SW}	Each converter	200		2200	kHz
Switching Frequency	f_{SET}	R_{OSC} = 10kΩ, each converter	1125	1250	1375	kHz
Switching Frequency Accuracy		5.6kΩ ≤ R_{OSC} ≤ 56kΩ, 1% each converter	-15		+15	%
SYNC Frequency Range	f_{SYNC}	SYNC input frequency is twice the individual converter frequency	400		4400	kHZ
SYNC High Threshold	V_{SYNCH}		2.4			V
SYNC Low Threshold	V_{SYNCL}				0.8	V
SYNC Input Min Pulse Width	t_{SYNCIN}			100		ns
Clock Output Phase Delay	CLKOUT PHASE	R_{OSC} = 60kΩ, 1%, with respect to converter 2 / SOURCE2 waveform		45		degrees
SYNC to SOURCE1 Phase Delay	$SYNC_{PHASE}$	R_{OSC} = 60kΩ, 1%		45		degrees
Clock Output High Level	$V_{CLKOUTH}$	VL = 5.2V, sourcing 5mA	4			V
Clock Output Low Level	$V_{CLKOUTL}$	VL = 5.2V, sinking 5mA			0.4	V
EN_ INPUTS						
EN_ Input High Threshold	V_{IH}	V+ = VL = 5.2V	2.4	1.8		V
EN_ Input Low Threshold	V_{IL}	V+ = VL = 5.2V		1.2	0.8	V
EN_ Bias Current	$I_{B(EN)}$				250	nA
POWER-GOOD OUTPUT (PGOOD_)						
PGOOD_ Threshold	$PGOOD_{VTH\_}$	PGOOD goes high after V_{OUT} crosses PGOOD_ threshold	90	92.5	95	$\%V_{OUT}$
PGOOD_ Output Voltage	$V_{PGOOD\_}$	I_{SINK} = 3mA (MAX5073ETI)			0.4	V
		I_{SINK} = 3mA (MAX5073ATI)			0.52	
PGOOD_ Output Leakage Current	$I_{LKPGOOD\_}$	V+ = VL = 5.2V, $V_{PGOOD\_}$ = 23V, $V_{FB\_}$ = 1V			1	µA
THERMAL MANAGEMENT						
Thermal Shutdown	T_{SHDN}	Junction temperature		+150		°C
Thermal Hysteresis	T_{HYST}	Junction temperature		30		°C

Note 1: Specifications at -40°C are guaranteed by design and not production tested.

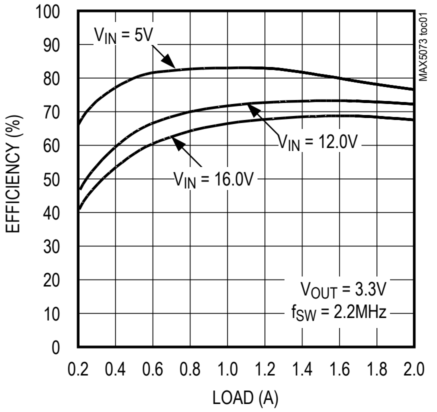
Note 2: Operating supply range (V+) is guaranteed by VL line regulation test. Connect V+ to VL for 5V operation.

Note 3: Output current may be limited by the power dissipation of the package, refer to the *Power Dissipation section in the Applications Information*.

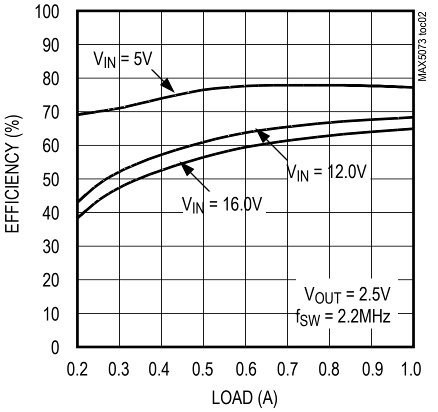
Typical Operating Characteristics

(V+ = VL = 5.2V, T_A = +25°C, unless otherwise noted.)

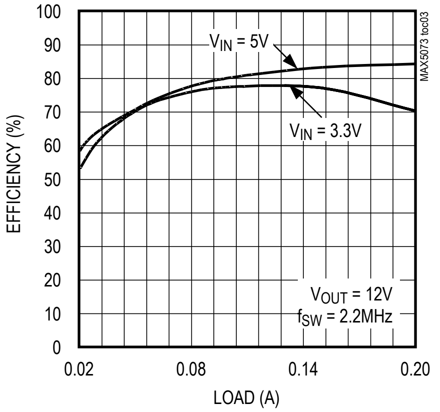
OUTPUT1 EFFICIENCY (BUCK CONVERTER) vs. LOAD CURRENT



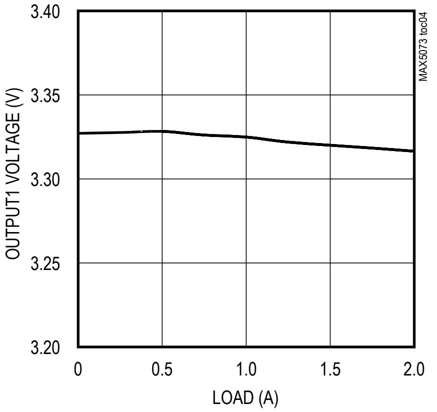
OUTPUT2 EFFICIENCY (BUCK CONVERTER) vs. LOAD CURRENT



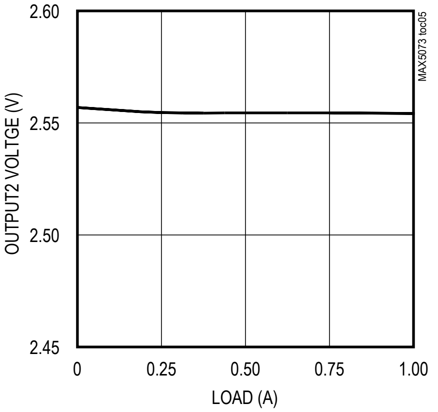
OUTPUT2 EFFICIENCY (BOOST CONVERTER) vs. LOAD CURRENT



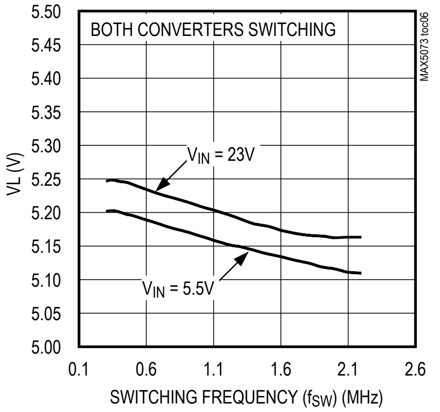
OUTPUT1 VOLTAGE (BUCK CONVERTER) vs. LOAD CURRENT



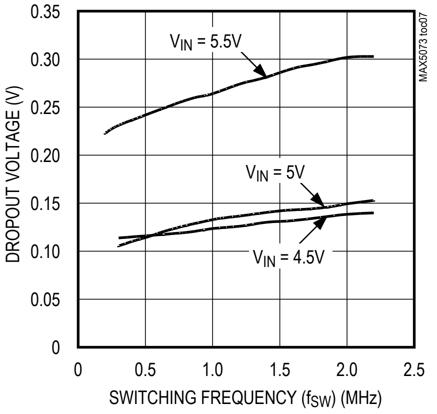
OUTPUT2 VOLTAGE (BUCK CONVERTER) vs. LOAD CURRENT



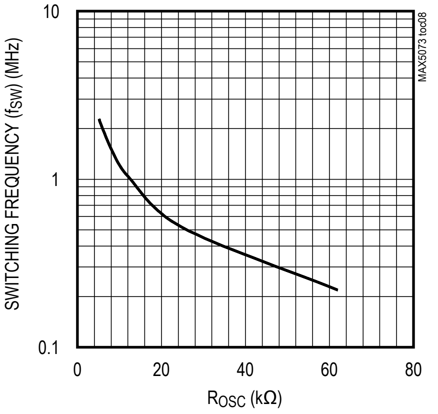
VL OUTPUT VOLTAGE vs. CONVERTER SWITCHING FREQUENCY



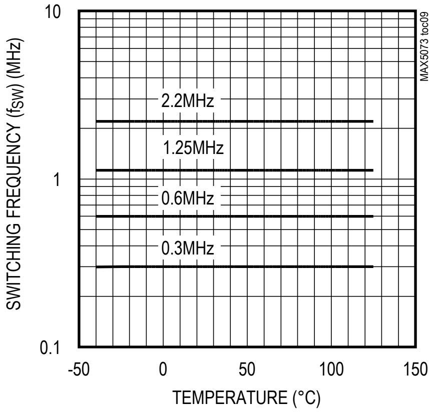
VL DROPOUT VOLTAGE vs. EACH CONVERTER SWITCHING FREQUENCY



EACH CONVERTER SWITCHING FREQUENCY vs. R_{OSC}



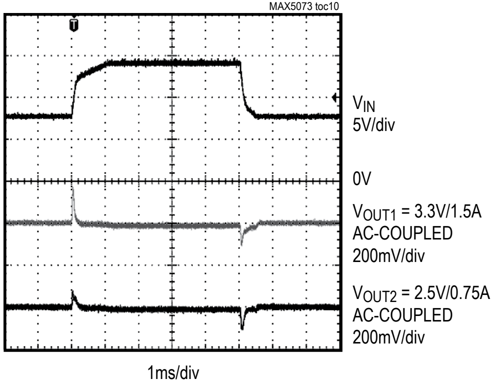
EACH CONVERTER SWITCHING FREQUENCY vs. TEMPERATURE



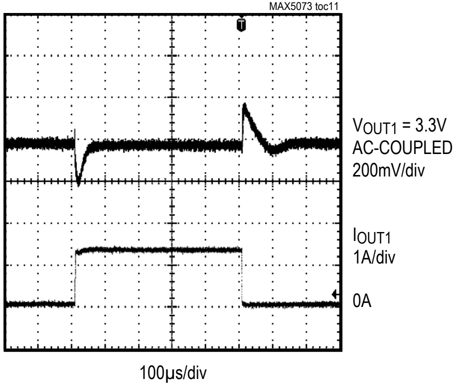
Typical Operating Characteristics (continued)

(V+ = VL = 5.2V, T_A = +25°C, unless otherwise noted.)

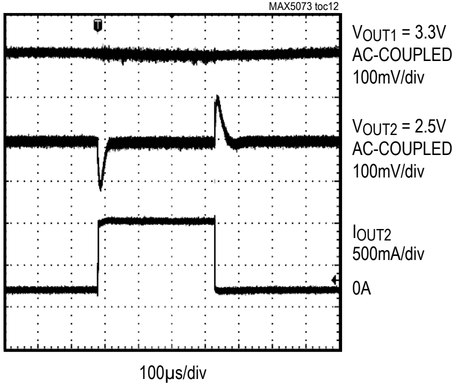
LINE-TRANSIENT RESPONSE (BUCK CONVERTER)



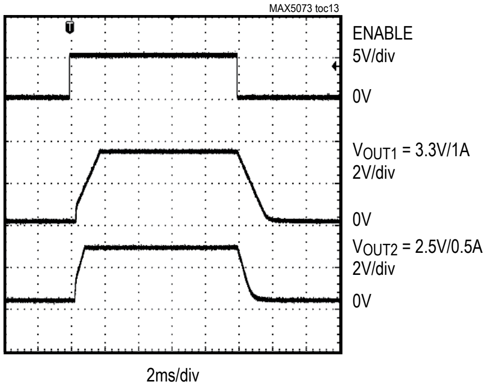
CONVERTER 1 LOAD-TRANSIENT RESPONSE (BUCK CONVERTER)



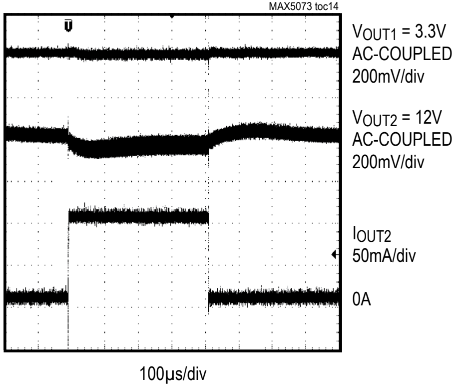
CONVERTER 2 LOAD-TRANSIENT RESPONSE (BUCK CONVERTER)



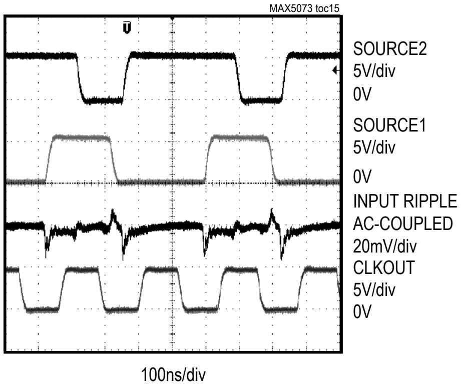
SOFT-START/SOFT-STOP



LOAD-TRANSIENT RESPONSE (BOOST CONVERTER)

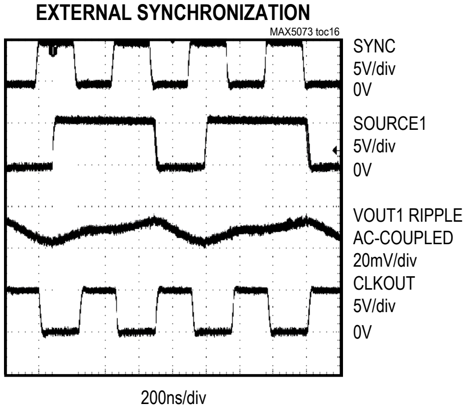


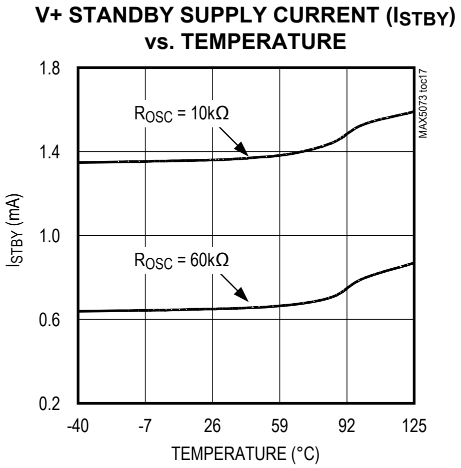
OUT-OF-PHASE OPERATION

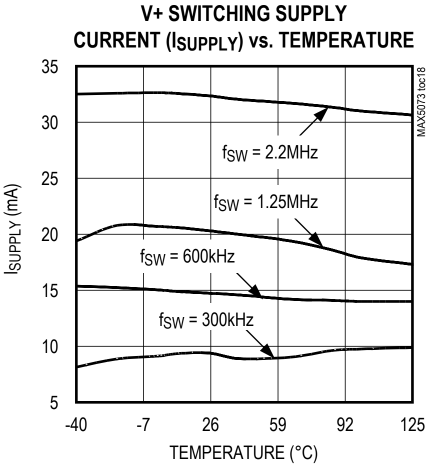


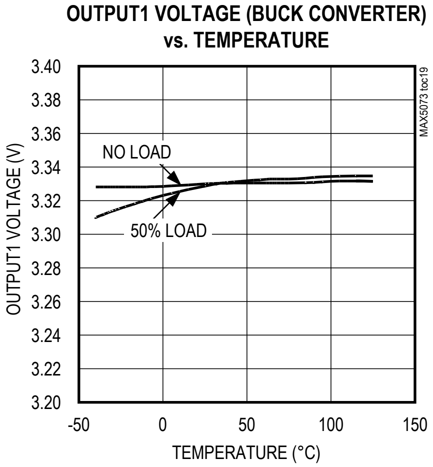
Typical Operating Characteristics (continued)

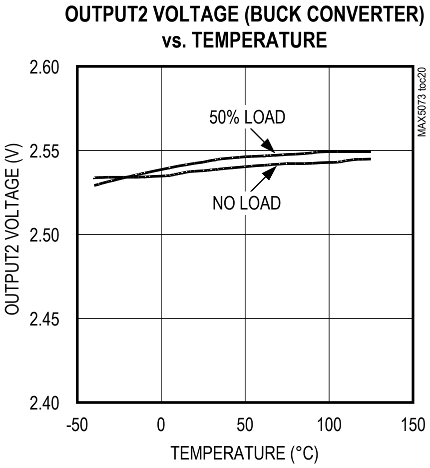
(V+ = VL = 5.2V, T_A = +25°C, unless otherwise noted.)





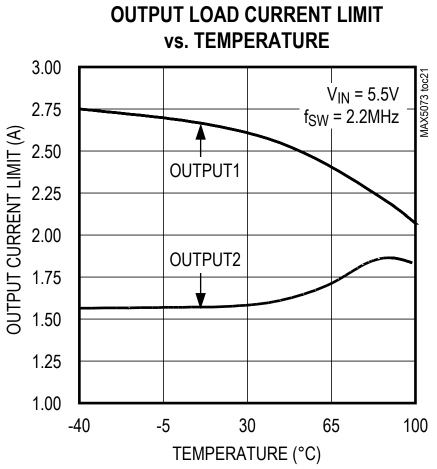


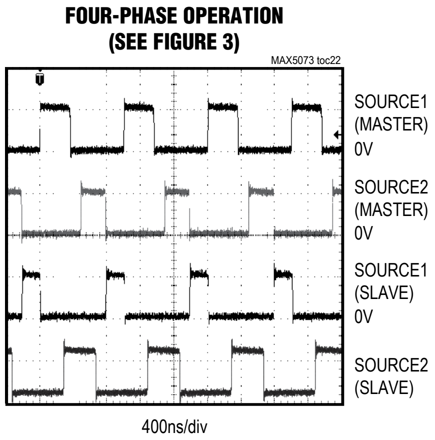




Typical Operating Characteristics (continued)

(V+ = VL = 5.2V, T_A = +25°C, unless otherwise noted.)





Pin Description

PIN	NAME	FUNCTION
1	CLKOUT	Clock Output. CLKOUT is 45° phase-shifted with respect to converter 2 (SOURCE2, Figure 3). Connect CLKOUT (master) to the SYNC of a second MAX5073 (slave) for a four-phase converter.
2	BST2/VDD2	Buck Converter Operation—Bootstrap Flying-Capacitor Connection for Converter 2. Connect BST2/VDD2 to an external ceramic capacitor and diode according to the standard application circuit (Figure 1). Boost Converter Operation—Driver Bypass Capacitor Connection. Connect a low-ESR 0.1µF ceramic capacitor from BST2/VDD2 to PGND (Figure 8).
3, 4	DRAIN2	Connection to Converter 2 Internal MOSFET Drain. Buck converter operation—use the MOSFET as a high-side switch and connect DRAIN2 to the input supply. Boost converter operation—use the MOSFET as a low-side switch and connect DRAIN2 to the inductor and diode junction (Figure 8).
5	EN2	Active-High Enable Input for Converter 2. Drive EN2 low to shut down converter 2, drive EN2 high for normal operation. Use EN2 in conjunction with EN1 for supply sequencing. Connect to VL for always-on operation.
6	FB2	Feedback Input for Converter 2. Connect FB2 to a resistive divider between converter 2's output and SGND to adjust the output voltage. To set the output voltage below 0.8V, connect FB2 to a resistive voltage-divider from BYPASS to regulator 2's output (Figure 5). See the *Setting the Output Voltage* section.
7	COMP2	Compensation Connection for Converter 2. See the *Compensation* section to compensate converter 2's control loop.
8	SYNC	External Clock Synchronization Input. Connect SYNC to a 400kHz to 4400kHz clock to synchronize the switching frequency with the system clock. Each converter frequency is one half the frequency applied to SYNC. Connect SYNC to SGND when not used.
9	N.C.	No Connection. Not internally connected.

Pin Description (continued)

PIN	NAME	FUNCTION
10	OSC	Oscillator Frequency Set Input. Connect a resistor from OSC to SGND (ROSC) to set the switching frequency (see the *Oscillator* section). Set ROSC for equal to or lower oscillator frequency than the SYNC input frequency when using external synchronization ($0.2f_{SYNC} < f_{OSC} < 1.2f_{SYNC}$). R_{OSC} is still required when an external clock is connected to the SYNC input.
11	V+	Input Supply Voltage. V+ voltage range from 5.5V to 23V. Connect the V+ and VL together for 4.5V to 5.5V input operation. Bypass with a minimum 0.1µF ceramic capacitor to SGND.
12, 13	VL	Internal 5.2V Linear Regulator Output. Use VL to drive the high-side switch at BST1/VDD1 and BST2/VDD2. Bypass VL with a 0.1µF capacitor to PGND and a 4.7µF ceramic capacitor to SGND.
14	BYPASS	2.0V Output. Bypass to SGND with a 0.22µF or greater ceramic capacitor.
15	COMP1	Compensation Connection for Converter 1 (See the *Compensation* Section)
16	FB1	Feedback Input for Converter 1. Connect FB1 to a resistive divider between converter 1's output and SGND to program the output voltage. To set the output voltage below 0.8V, connect FB1 to a resistive voltage- divider from BYPASS to regulator 1's output (Figure 5). See the Setting the Output Voltage section.
17	EN1	Active-High Enable Input for Converter 1. Drive EN1 low to shut down converter 1, drive EN1 high for normal operation. Use EN1 in conjunction with EN2 for supply sequencing. Connect to VL for always-on operation.
18, 19	DRAIN1	Connection to the Converter 1 Internal MOSFET Drain. Buck converter operation—use the MOSFET as a high-side switch and connect DRAIN1 to the input supply. Boost converter operation—use the MOSFET as a low-side switch and connect DRAIN1 to the inductor and diode junction.
20	BST1/VDD1	Buck Converter Operation—Bootstrap Flying-Capacitor Connection for Converter 1. Connect BST1/VDD1 to an external ceramic capacitor and diode according to the Standard Application Circuit (Figure 1). Boost Converter Operation—Driver Bypass Capacitor Connection. Connect a low-ESR 0.1µF ceramic capacitor from BST1/VDD1 to PGND.
21	PGOOD1	Converter 1 Power-Good Output. Open-drain output goes low when converter 1's output falls below 92.5% of its set regulation voltage. Use PGOOD1, PGOOD2, EN1, and EN2 to sequence the converters.
22	PGOOD2	Converter 2 Power-Good Output. Open-drain output goes low when converter 2's output falls below 92.5% of its set regulation voltage.
23, 24	SOURCE1	Connection to the Converter 1 Internal MOSFET Source. Buck converter operation—connect SOURCE1 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE1 to PGND.
25	SGND	Signal Ground. Connect SGND to the exposed pad. Connect SGND and PGND together at a single point.
26	PGND	Power Ground. Connect rectifier diode anode, input capacitor negative, output capacitor negative, and VL bypass capacitor returns to PGND.
27, 28	SOURCE2	Connection to the Converter 2 Internal MOSFET Source. Buck converter operation—connect SOURCE2 to the switched side of the inductor as shown in Figure 1. Boost converter operation—connect SOURCE2 to PGND (Figure 8).
EP	SGND	Exposed Paddle. Connect to SGND. Solder EP to the SGND plane for better thermal performance.

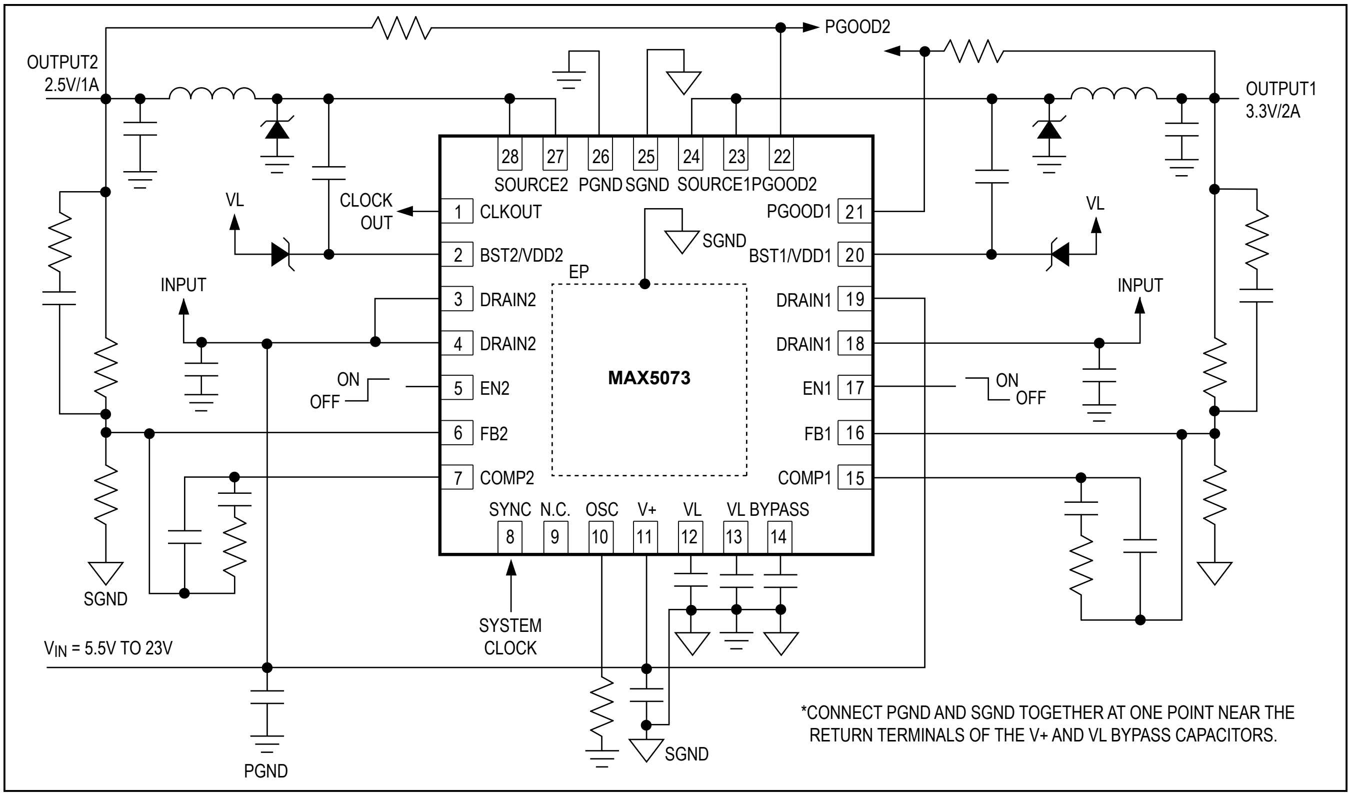


Figure 1. MAX5073 Dual Buck Regulator Application Circuit

Detailed Description

PWM Controller

The MAX5073 converter uses a pulse-width modulation (PWM) voltage-mode control scheme for each out-of-phase controller. It is nonsynchronous rectification and uses an external low-forward-drop Schottky diode for rectification. The controller generates the clock signal by dividing down the internal oscillator or the SYNC input when driven by an external clock, so each controller's switching frequency equals half the oscillator frequency ($f_{SW} = f_{OSC}/2$). An internal transconductance error amplifier produces an integrated error voltage at the COMP pin, providing high DC accuracy. The voltage at COMP sets the duty cycle using a PWM comparator and a ramp generator. At each rising edge of the clock, converter 1's high-side n-channel MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the maximum current limit for the switch is detected. Converter 2 operates out-of-phase, so the second high-side MOSFET turns on at each falling edge of the clock.

In the case of buck operation (Figure 1), during each high-side MOSFET?s on-time, the associated inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off and forward biases the Schottky rectifier. During this time, the SOURCE voltage is clamped to 0.4V (V_D) below ground. The inductor releases the stored energy as its current ramps down, and provides current to the output. The bootstrap capacitor is also recharged from the inductance energy when the MOSFET turns off. The circuit goes in discontinuous conduction mode operation at light load, when the inductor current completely discharges before the next cycle commences. Under overload conditions, when the inductor current exceeds the peak current limit of the respective switch, the high-side MOSFET turns off quickly and waits until the next clock cycle.

In the case of boost operation, the MOSFET is a low-side switch (Figure 8). During each on-time, the inductor current ramps up. During the second half of the switching cycle, the low-side switch turns off and forward biases the Schottky diode. During this time, the DRAIN voltage is clamped to 0.4V (V_D) above $V_{OUT\_}$ and the inductor provides energy to the output as well as replenishes the output capacitor charge.

Internal Oscillator/Out-of-Phase Operation

The internal oscillator generates the 180° out-of-phase clock signal required by each regulator. The internal oscillator frequency is programmable from 400kHz to 4.4MHz using a single 1% resistor at R_{OSC}. Use the following equation to calculate R_{OSC}:

$$R_{OSC} = \frac{25 \times 10^9}{f_{OSC}}$$

where f_{OSC} is the internal oscillator frequency in hertz and R_{OSC} in ohms.

The two independent regulators in the MAX5073 switch 180° out-of-phase to reduce input filtering requirements, to reduce electromagnetic interference (EMI), and to improve efficiency. This effectively lowers component cost and saves board space, making the MAX5073 ideal for cost-sensitive applications.

With dual synchronized out-of-phase operation, the MAX5073's high-side MOSFETs turn on 180° out-of-phase. The instantaneous input current peaks of both regulators do not overlap, resulting in reduced RMS ripple current and input voltage ripple. This reduces the required input capacitor ripple current rating, allows for fewer or less expensive capacitors, and reduces shielding requirements for EMI. The out-of-phase waveforms in the *Typical Operating Characteristics* demonstrate synchronized 180° out-of-phase operation.

Synchronization (SYNC)/ Clock Output (CLKOUT)

The main oscillator can be synchronized to the system clock by applying an external clock (f_{SYNC}) at SYNC. The f_{SYNC} frequency must be twice the required operating frequency of an individual converter. Use a TTL logic signal for the external clock with at least a 100ns pulse width. R_{OSC} is still required when using external synchronization. Program the internal oscillator frequency so $0.2f_{SYNC} < f_{OSC} < 1.2f_{SYNC}$. The rising edge of f_{SYNC} synchronizes the turn-on edge of the internal MOSFET (see Figure 3).

$$R_{OSC} = \frac{25 \times 10^9}{f_{OSC}}$$

where f_{OSC} is the internal oscillator frequency in hertz and R_{OSC} in ohms, $f_{OSC} = 2 \times f_{SW}$.

Two MAX5073s can be connected in the master-slave configuration for four ripple-phase operation. The MAX5073 provides a clock output (CLKOUT) that is 45° phase-shifted with respect to the internal switch turn-on edge. Feed the CLKOUT of the master to the SYNC input of the slave. The effective input ripple switching frequency shall be four times the individual converter's switching frequency. When driving the master converter using external clock at SYNC, set the clock duty cycle to 50% for a 90° phase-shifted operation.

Input Voltage (V+)/Internal Linear Regulator (VL)

All internal control circuitry operates from an internally regulated nominal voltage of 5.2V (VL). At higher input voltages (V+) of 5.5V to 23V, VL is regulated to 5.2V. At 5.5V or below, the internal linear regulator operates in dropout mode, where VL follows V+. Depending on the load on VL, the dropout voltage can be high enough to reduce VL below the undervoltage lockout (UVLO) threshold.

For input voltages of less than 5.5V, connect V+ and VL together. The load on VL is proportional to the switching frequency of converter 1 and converter 2. See the Dropout Voltage vs. Switching Frequency graph in the *Typical Operating Characteristics*. For input voltage ranges higher than 5.5V, use the internal regulator.

Bypass V+ to SGND with a low-ESR, 0.1µF or greater ceramic capacitor placed close to the MAX5073. Current spikes from VL may disturb internal circuitry powered by VL. Bypass VL with a low-ESR, ceramic 0.1µF capacitor to PGND and 4.7µF capacitor to SGND.

Undervoltage Lockout/Soft-Start

The MAX5073 includes an undervoltage lockout with hysteresis and a power-on-reset circuit for converter turn-on and monotonic rise of the output voltage. The rising UVLO threshold is internally set to 4.3V with a 175mV hysteresis. Hysteresis at UVLO eliminates "chattering" during startup. When VL drops below UVLO, the internal switches are turned off.

Digital soft-start is provided internally to reduce input surge currents and glitches at the input during turn-on. When UVLO is cleared and EN_ is high, digital soft-start slowly ramps up the internal reference voltage in 64 steps. The total soft-start period is 2048 switching cycles of the internal oscillator.

To calculate the soft-start period, use the following equation:

$$t_{SS} = \frac{2048}{f_{OSC}}$$

where f_{OSC} is the internal oscillator frequency in hertz, which is twice the switching frequency of each converter.

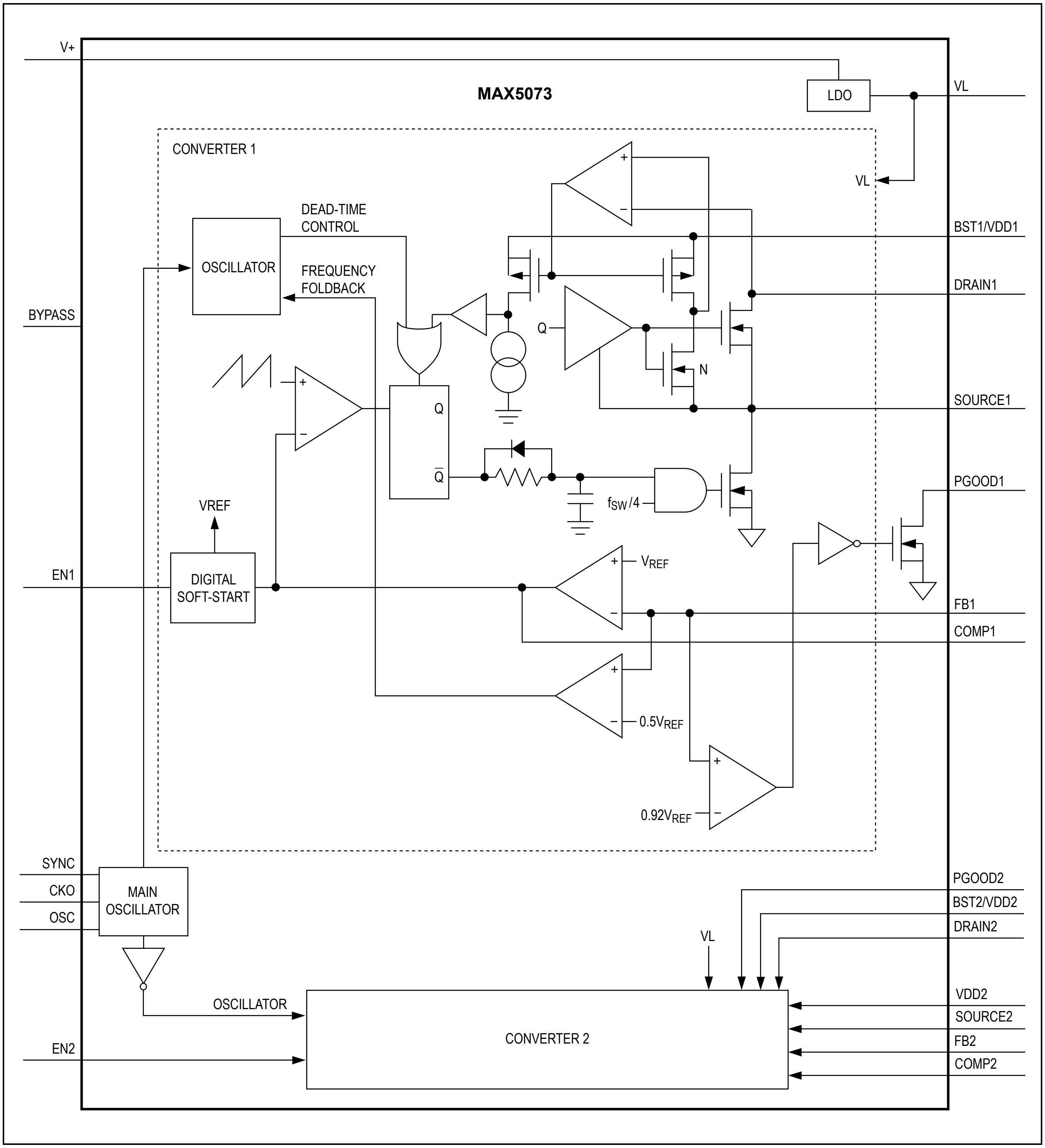


Figure 2. Functional Diagram

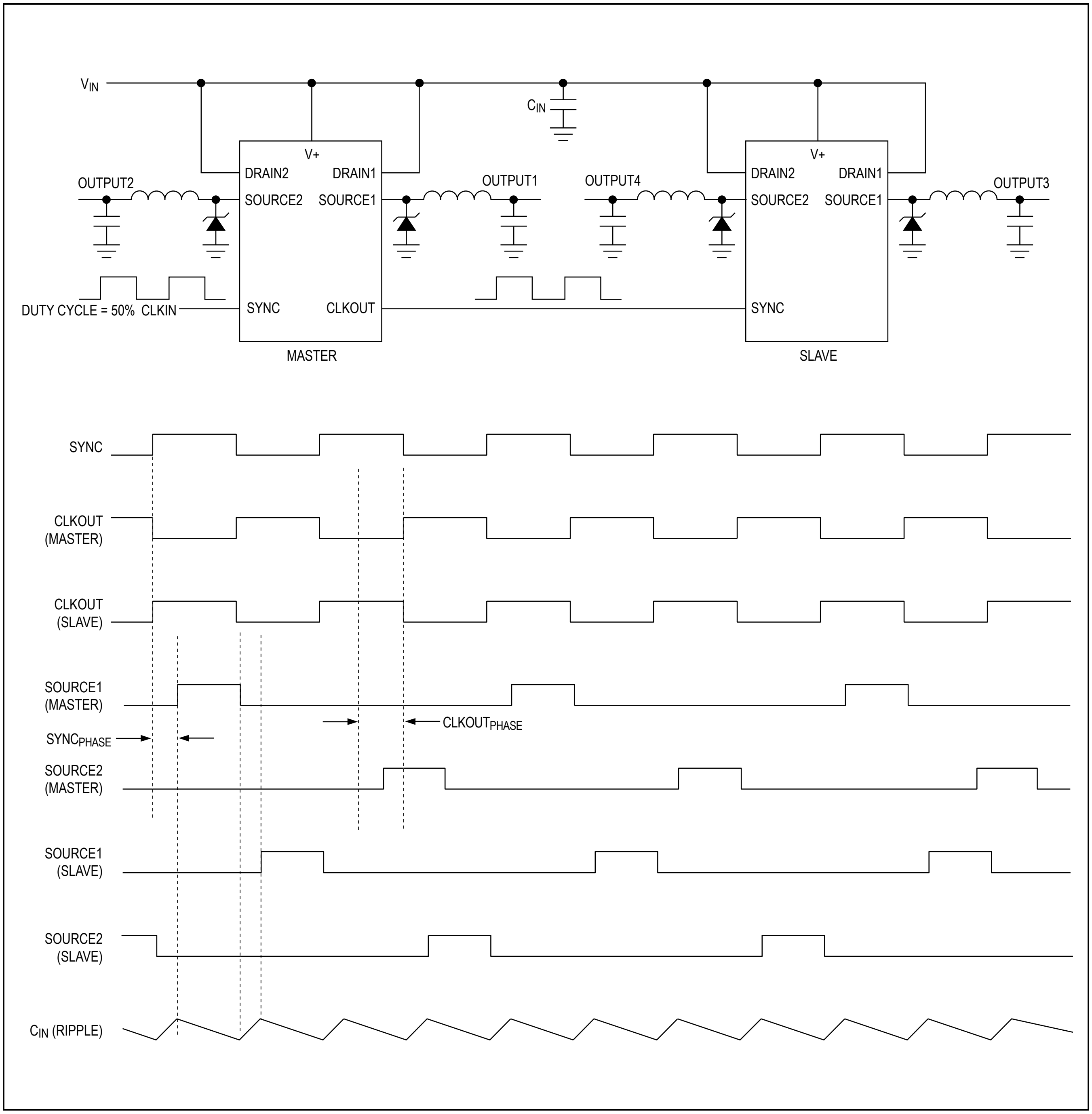


Figure 3. Synchronized Controllers

Enable

The MAX5073 dual converter provides separate enable inputs EN1 and EN2 to individually control or sequence the output voltages. These active-high enable inputs are TTL compatible. Pulling EN_ high ramps up the reference slowly, which provides soft-start at the outputs. Forcing the EN_ low externally disables the individual output and generates a PGOOD_ signal. Use EN1, EN2, and PGOOD1 for sequencing (see Figure 4). Connect PGOOD1 to EN2 to make sure converter 1's output is within regulation before converter 2 starts. Add an RC network from VL to EN1 and EN2 to delay the individual converter. A larger RC time constant means a more delayed output. Sequencing reduces input inrush current and possible chattering. Connect the EN_ to VL for always-on operation.

PGOOD_

Converter 1 and converter 2 includes a power-good flag, PGOOD1 and PGOOD2, respectively. Since PGOOD is an open-drain output and can sink 3mA while providing the TTL logic-low signal, pull PGOOD to a logic voltage to provide a logic-level output. PGOOD goes low when converter 1's output drops to 92.5% of its nominal regulated voltage. Connect PGOOD to SGND or leave unconnected if not used.

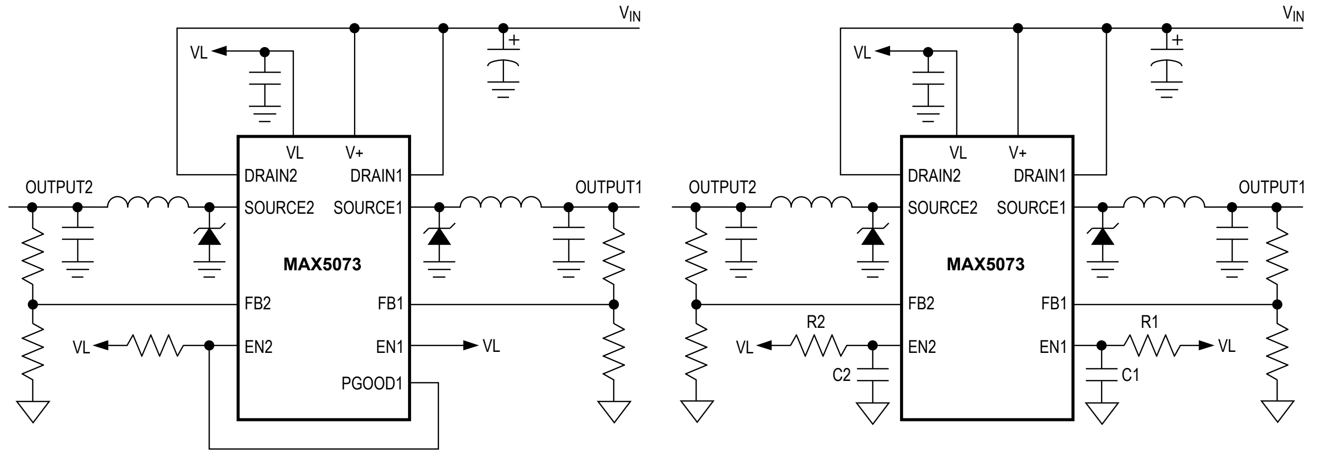
Current Limit

The internal switch current of each converter is sensed using an internal current mirror. Converter 1 and converter 2 have 2A and 1A internal switches. When the peak switch current crosses the current-limit threshold of 3A (typ) and 1.8A (typ) for converter 1 and converter 2, respectively, the on cycle is terminated immediately and the inductor is allowed to discharge. The next cycle resumes at the next clock pulse.

In deep overload or short-circuit conditions when the FB voltage drops below 0.4V, the switching frequency is reduced to 1/4 x f_{SW} to provide sufficient time for the inductor to discharge. During overload conditions, if the voltage across the inductor is not high enough to allow for the inductor current to properly discharge, current runaway may occur. Current runaway can destroy the device in spite of internal thermal-overload protection. Reducing the switching frequency during overload conditions prevents current runaway.

Thermal-Overload Protection

During continuous short circuit or overload at the output, the power dissipation in the IC can exceed its limit. Internal thermal shutdown is provided to avoid irreversible damage to the device. When the die temperature or junction temperature exceeds +150°C, an on-chip thermal sensor shuts down the device, forcing the internal switches to turn off, allowing the IC to cool. The thermal sensor turns the part on again after the junction temperature cools by +30°C. During thermal shutdown, both regulators shut down, PGOOD_ go low, and soft-start resets.



SEQUENCING—OUTPUT 2 DELAYED WITH RESPECT TO OUTPUT 1.

R1/C1 AND R2/C2 ARE SIZED FOR REQUIRED SEQUENCING.

Figure 4. Power-Supply Sequencing Configurations

Applications Information

Setting the Switching Frequency

The controller generates the clock signal by dividing down the internal oscillator or the SYNC input signal when driven by an external oscillator. The switching frequency equals half the oscillator frequency ($f_{SW} = f_{OSC}/2$). The internal oscillator frequency is set by a resistor (R_{OSC}) connected from OSC to SGND. The relationship between f_{SW} and R_{OSC} is:

$$R_{OSC} = \frac{12.5 \times 10^9}{f_{SW}}$$

where f_{SW} and f_{OSC} are in hertz, and R_{OSC} is in ohms. For example, a 1250kHz switching frequency is set with R_{OSC} = 10kΩ. Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

A rising clock edge on SYNC is interpreted as a synchronization input. If the SYNC signal is lost, the internal oscillator takes control of the switching rate, returning the switching frequency to that set by R_{OSC}. This maintains output regulation even with intermittent SYNC signals. When an external synchronization signal is used, R_{OSC} should be set for the oscillator frequency to be lower than or equal to the SYNC rate (f_{SYNC}).

Buck Converter

Effective Input Voltage Range

Although the MAX5073 converters can operate from input supplies ranging from 5.5V to 23V, the input voltage range can be effectively limited by the MAX5073 duty-cycle limitations for a given output voltage. The maximum input voltage is limited by the minimum on-time ($t_{ON(MIN)}$):

$$V_{IN(MAX)} \le \frac{V_{OUT}}{t_{ON(MIN)} \times f_{SW}}$$

where $t_{ON(MIN)}$ is 100ns. The minimum input voltage is limited by the maximum duty cycle (DMAX = 88):

$$V_{IN(MIN)} = \left[\frac{V_{OUT} + V_{DROP1}}{0.88}\right] + V_{DROP2} - V_{DROP1}$$

where V_{DROP1} is the total parasitic voltage drops in the inductor discharge path, which includes the forward voltage drop (V_D) of the rectifier, the series resistance of the inductor, and the PC board resistance. V_{DROP2} is the total resistance in the charging path, which includes the on-resistance of the high-side switch, the series resistance of the inductor, and the PC board resistance.

Setting the Output Voltage

For 0.8V or greater output voltages, connect a voltage-divider from OUT_ to FB_ to SGND (Figure 5). Select R_B (FB_ to SGND resistor) to between 1kΩ and 10kΩ. Calculate R_A (OUT_ to FB_ resistor) with the following equation:

$$R_A = R_B\left[\left(\frac{V_{OUT}}{V_{FB}}\right) - 1\right]$$

where $V_{FB\_}$ = 0.8V (see the *Electrical Characteristics* table) and $V_{OUT\_}$ can range from $V_{FB\_}$ to 28V (boost operation).

For output voltages below 0.8V, set the MAX5073 output voltage by connecting a voltage-divider from the output to FB_ to BYPASS (Figure 5). Select R_C (FB to BYPASS resistor) higher than a 50kΩ range. Calculate R_A with the following equation:

$$R_A = R_C\left[\frac{V_{FB} - V_{OUT}}{V_{BYPASS} - V_{FB}}\right]$$

where V_{FB} = 0.8V, V_{BYPASS} = 2V (see the *Electrical Characteristics* table), and $V_{OUT\_}$ can range from 0V to $V_{FB\_}$.

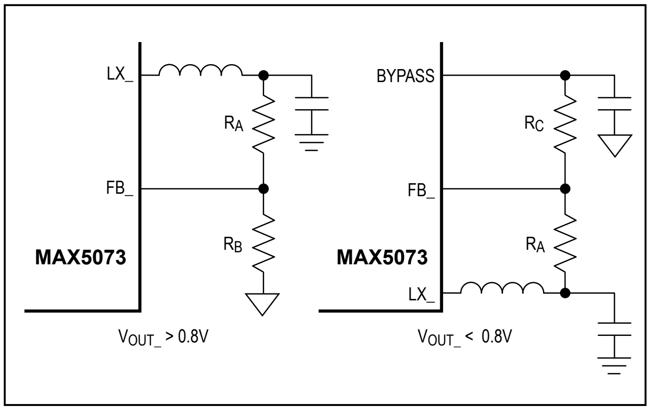


Figure 5. Adjustable Output Voltage

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX5073: inductance value (L), peak inductor current (I_L), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential and the peak-to-peak inductor current (ΔI_L). Higher ΔI_L allows for a lower inductor value while a lower ΔI_L requires a higher inductor value. A lower inductor value minimizes size and cost, improves large-signal transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output ripple voltage for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. However, resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels, especially when the inductance is increased without also allowing for larger inductor dimensions. A good compromise is to choose ΔI_L equal to 30% of the full load current. To calculate the inductance use the following equation:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

where V_{IN} and V_{OUT} are typical values (so that efficiency is optimum for typical conditions). The switching frequency is set by R_{OSC} (see the *Setting the Switching Frequency* section). The peak-to-peak inductor current, which reflects the peak-to-peak output ripple, is worse at the maximum input voltage. See the *Output Capacitor Selection* section to verify that the worst-case output ripple is acceptable. The inductor saturating current is also important to avoid runaway current during output overload and continuous short circuit. Select the I_{SAT} to be higher than the maximum peak current limits of 4.5A and 2.2A for converter 1 and converter 2.

Input Capacitors

The discontinuous input current waveform of the buck converter causes large ripple currents at the input. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple dictate the input capacitance requirement. Increasing the switching frequency or the inductor value lowers the peak to average current ratio, yielding a lower input capacitance requirement. Note that two converters of MAX5073 run 180° out-of-phase, thereby effectively doubling the switching frequency at the input.

The input ripple waveform would be unsymmetrical due to the difference in load current and duty cycle between converter 1 and converter 2. The input ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). A higher load converter dictates the ESR requirement, while the capacitance requirement is a function of the loading mismatch between the two converters. The worst-case mismatch is when one converter is at full load while the other is at no load or in shutdown. Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{\left(I_{OUT} + \frac{\Delta I_L}{2}\right)}$$

where

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times f_{SW}}$$

where

$$D = \frac{V_{OUT}}{V_{IN}}$$

where I_{OUT} is the maximum output current from either converter 1 or converter 2, and D is the duty cycle for that converter. f_{SW} is the frequency of each individual converter. For example, at V_{IN} = 12V, V_{OUT} = 3.3V at I_{OUT} = 2A, and with L = 3.3µH, the ESR and input capacitance are calculated for a peak-to-peak input ripple of 100mV or less, yielding an ESR and capacitance value of 20mΩ and 6.8µF for 1.25MHz frequency. Use a 100µF capacitor at low input voltages to avoid possible undershoot below the undervoltage lockout threshold during power-on and transient loading.

Output Capacitors

The allowable output ripple voltage and the maximum deviation of the output voltage during step load currents determines the output capacitance and its ESR.

The output ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use the ESR_{OUT} equation to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output ripple voltage from the ESR and the capacitor discharge are equal. Calculate the output capacitance and ESR required for a specified ripple using the following equations:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{\Delta I_L}$$

$$C_{OUT} = \frac{\Delta I_L}{8 \times \Delta V_Q \times f_{SW}}$$

where

$$\Delta V_{O\_RIPPLE} \cong \Delta V_{ESR} + \Delta V_Q$$

where ΔI_L is the peak-to-peak inductor current as calculated above and f_{SW} is the individual converter's switching frequency.

The allowable deviation of the output voltage during fast transient loads also determines the output capacitance and its ESR. The output capacitor supplies the step load current until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter. The high switching frequency of MAX5073 allows for higher closed-loop bandwidth, reducing $t_{RESPONSE}$ and the output capacitance requirement. The resistive drop across the output capacitor ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient load and ripple/noise performance. Keep the maximum output voltage deviation above the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume 80% and 20% contribution from the output capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

where I_{STEP} is the load step and $t_{RESPONSE}$ is the response time of the controller. Controller response time depends on the control-loop bandwidth.

Boost Converter

The MAX5073 can be configured for step-up conversion since the internal MOSFET can be used as a low-side switch. Use the following equations to calculate the inductor (L_{MIN}), input capacitor (C_{IN}), and output capacitor (C_{OUT}) when using the converter in boost operation.

Inductor

Choose the minimum inductor value so the converter remains in continuous mode operation at minimum output curt (I_{OMIN})

$$L_{MIN} = \frac{V^2{}_{IN} \times D \times \eta}{2 \times f_{SW} \times V_O \times I_{OMIN}}$$

where

$$\frac{V_O + V_D - V_{IN}}{V_O + V_D - V_{DS}}$$

and $I_{OMIN} = 0.25 \times I_O$

The V_D is the forward voltage drop of the external Schottky diode, D is the duty cycle, and V_{DS} is the voltage drop across the internal switch. Select the inductor with low DC resistance and with a saturation current (I_{SAT}) rating higher than the peak switch current limit of 4.5A and 2.2A of converter 1 and converter 2, respectively.

Input Capacitor

The input current for the boost converter is continuous and the RMS ripple current at the input is low. Calculate the capacitor value and ESR of the input capacitor using the following equations.

$$\mathrm{IN} \quad \frac{\Delta I \quad \times D}{4 \times f_{SW} \times \Delta V_Q}$$

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$

where

$$\Delta I_L = \frac{(V_{IN} - V_{DS}) \times D}{L \times f_{SW}}$$

where V_{DS} is the total voltage drop across the internal MOSFET plus the voltage drop across the inductor ESR. ΔI_L is the peak-to-peak inductor ripple current as calculated above. ΔV_Q is the portion of input ripple due to the capacitor discharge and ΔV_{ESR} is the contribution due to ESR of the capacitor.

Output Capacitor

For the boost converter, the output capacitor supplies the load current when the main switch is ON. The required output capacitance is high, especially at higher duty cycles. Also, the output capacitor ESR needs to be low enough to minimize the voltage drop due to the ESR while supporting the load current. Use the following equation to calculate the output capacitor for a specified output ripple tolerance.

$$ESR = \frac{\Delta V_{ESR}}{I_O}$$

$$C_{OUT} = \frac{I_O \times D_{MAX}}{\Delta V_Q \times f_{SW}}$$

I_O is the load current, ΔV_Q is the portion of the ripple due to the capacitor discharge and ΔV_{ESR} is the contribution due to the ESR of the capacitor. D_{MAX} is the maximum duty cycle at minimum input voltage.

Power Dissipation

The MAX5073 includes a high-frequency, low R_{DS_ON} switching MOSFET. At +85°C, the R_{DS_ON} of the internal switch for converter 1 and converter 2 are 290mΩ and 630mΩ, respectively. The DC loss is a function of the RMS current in the switch while the switching loss is a function of switching frequency and input voltage. Use the following equations to calculate the RMS current, DC loss, and switching loss of each converter. The MAX5073 device is available in a thermally enhanced package and can dissipate up to 2.7W at +70°C ambient temperature. The total power dissipation in the package must be limited so the junction temperature does not exceed its absolute maximum rating of +150°C at maximum ambient temperature.

For the buck converter:

$$I_{RMS} = \sqrt{(I^2_{DC} + I^2_{PK} + (I_{DC} \times I_{PK})) \times \frac{D_{MAX}}{3}}$$

$$P_{DC} = I^2_{RMS} \times R_{DS(ON)MAX}$$

where

$$I_{DC} = I_O - \frac{\Delta I_L}{2}$$

$$I_{PK} = I_O + \frac{\Delta I_L}{2}$$

See the *Electrical Characteristics* table for the $R_{DS(ON)MAX}$ value.

$$P_{SW} = \frac{V_{INMAX} \times I_O \times (t_R + t_F) \times f_{SW}}{4}$$

For the boost converter:

$$I_{RMS} = \sqrt{(I^2_{DC} + I^2_{PK} + (I_{DC} \times I_{PK})) \times \frac{D_{MAX}}{3}}$$

$$I_{IN} = \frac{V_O \times I_O}{V_{IN} \times \eta}$$

$$\Delta I_L = \frac{(V_{IN} - V_{DS}) \times D}{L \times f_{SW}}$$

$$I_{DC} = I_{IN} - \frac{\Delta I_L}{2}$$

$$I_{PK} = I_{IN} + \frac{\Delta I_L}{2}$$

$$P_{DC} = I^2_{RMS} \times R_{DS(ON)MAX}$$

where V_{DS} is the drop across the internal MOSFET. See the *Electrical Characteristics* for the $R_{DS(ON)MAX}$ value.

$$P_{SW} = \frac{V_O \times I_{IN} \times (t_R + t_F) \times f_{SW}}{4}$$

where t_R and t_F are rise and fall times of the internal MOSFET. The t_R and t_F are typically 20ns, and can be measured in the actual application.

The supply current in the MAX5073 is dependent on the switching frequency. See the *Typical Operating Characteristics* to find the supply current of the MAX5073 at a given operating frequency. The power dissipation (P_S) in the device due to supply current (I_S) is calculated using fowing equation.

$$P_S = V_{INMAX} \times I_{SUPPLY}$$

The total power dissipation P_T in the device is:

$$P_T = P_{DC1} + P_{DC2} + P_{SW1} + P_{SW2} + P_S$$

where P_{DC1} and P_{DC2} are DC losses in converter 1 and converter 2, respectively. P_{SW1} and P_{SW2} are switching losses in converter 1 and converter 2.

Calculate the temperature rise of the die using the following equation:

$$T_J = T_C + (P_T \text{ x } \theta_{JC})$$

where, θ_{JC} is the junction-to-case thermal impedance of the package equal to +2°C/W. Solder the exposed pad of the package to a large copper area to minimize the case-to-ambient thermal impedance. Measure the temperature of the copper area near the device at a worst-case condition of power dissipation and use +2°C/W as θ_{JC} thermal impedance. The case-to-ambient thermal impedance ($\theta_{C\text{-}A}$) is dependent on how well the heat is transferred from the PC board to the ambient. Use a large copper area to keep the PC board temperature low. The $\theta_{C\text{-}A}$ is usually in the +20°C/W to +40°C/W range .

Compensation

The MAX5073 provides an internal transconductance amplifier with its inverting input and its output available to the user for external frequency compensation. The flexibility of external compensation for each converter offers wide selection of output filtering components, especially the output capacitor. For cost-sensitive applications, use high-ESR aluminum electrolytic capacitors; for component size-sensitive applications, use low-ESR tantalum or ceramic capacitors at the output. The high switching frequency of MAX5073 allows use of ceramic capacitors at the output.

Choose all the passive power components that meet the output ripple, component size, and component cost requirements. Choose the small-signal components for the error amplifier to achieve the desired closed-loop bandwidth and phase margin. Use a simple pole-zero pair (Type II) compensation if the output capacitor ESR zero frequency is below the unity-gain crossover frequency (f_C). Type III compensation is necessary when the ESR zero frequency is higher than f_C or when compensating for a continuous mode boost converter that has a right-half-plane zero.

Use the following procedure 1 to calculate the compensation network components when $f_{ZERO,ESR} < f_C$.

Buck Converter Compensation

Procedure 1 (See Figure 6)

1) Calculate the $f_{ZERO,ESR}$ and LC double pole:

$$f_{ZERO,ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

2) Calculate the unity-gain crossover frequency as:

$$f_C = \frac{f_{SW}}{20}$$

If the $f_{ZERO,ESR}$ is lower than f_C and close to f_{LC}, use a Type II compensation network where R_FC_F provides a midband zero fmid,zero, and R_{FCCF} provides a high-frequency pole.

3) Calculate modulator gain GM at the croser frequency.

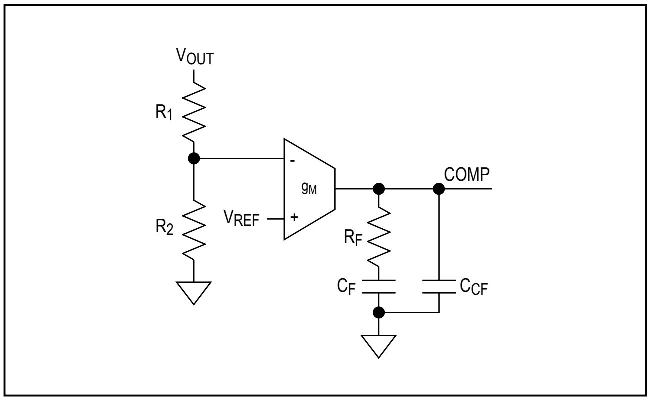


Figure 6. Type II Compensation Network

$$G_M=\frac{V_{IN}}{V_{OSC}}\times\frac{ESR}{ESR+(2\pi\times f_C\times L_{OUT})}\times\frac{0.8}{V_{OUT}}$$

where V_{OSC} is a peak-to-peak ramp amplitude equal to 1V.

The transconductance error amplifier gain is:

$$G_{E/A}=g_m\times R_F$$

The total loop gain at f_C sho be equal to 1

$$G_M\times G_{E/A}=1$$

or

$$R_F=\frac{V_{OSC}(ESR+2\pi\times f_C\times L_{OUT})V_{OUT}}{0.8\times V_{IN}\times g_m\times ESR}$$

4) Place a zero at or below the LC double pole:

$$C_F=\frac{1}{2\pi\times R_F\times f_{LC}}$$

5) Place a high-frequency pole at $f_P = 0.5 \times f_{SW}$.

Procedure 2 (see Figure 7)

If the output capacitor used is a low-ESR ceramic type, the ESR frequency is usually far away from the targeted unity crossover frequency (f_C). In this case, Type III compensation is recommended. Type III compensation provides two-pole zero pairs. The locations of the zero and poles should be such that the phase marginaks at f_C.

The $\frac{f_C}{f_Z}=\frac{f_P}{f_C}=5$ is a good number to get about 60° phase margin at f_C. However, it is important to place the two zeros at or below the double pole to avoid the conditional stability issue.

1) Select a crossover frequency:

$$f_C\le\frac{f_{SW}}{20}$$

2) Calculate the LC double-pole frequency, f_{LC}:

$$f_{LC}=\frac{1}{2\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$

3) Place a zero

$$f_Z=\frac{1}{2\pi\times R_F\times C_F}\text{ at }0.75\times f_{LC}$$

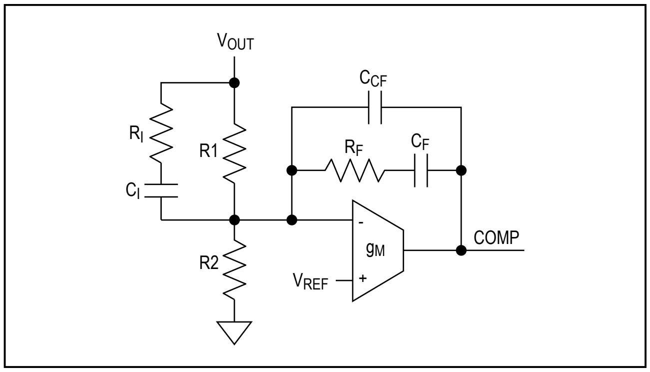


Figure 7. Type III Compensation Network

where:

$$C_F=\frac{1}{2\pi\times0.75\times f_{LC}\times R_F}$$

and $R_F \ge 10k\Omega$.

4) Calculate C_I for a target unity crossoverequency, f_C:

$$C_I=\frac{2\pi\times f_C\times L_{OUT}\times C_{OUT}\times V_{OSC}}{V_{IN}\times R_F}$$

5) Place a pole $\left(f_{P1}=\frac{1}{2\pi\times R_I\times C_I}\right)$ at $f_{ZERO,ESR}$.

$$R_I=\frac{1}{2\pi\times f_{ZERO,ESR}\times C_I}$$

6) Place a second zero, f_{Z2}, at $0.2 \times f_C$ or at f_{LC}, whichever is lower.

$$R1=\frac{1}{2\pi\times f_{Z2}\times C_I}-R_I$$

7) Placece a second pole $\left(f_{P2}=\frac{1}{2\pi\times R_F\times C_{CF}}\right)$ at 1/2 the swiing frequency.

$$C_{CF}=\frac{C_F}{(2\pi\times0.5\times f_{SW}\times R_F\times C_F)-1}$$

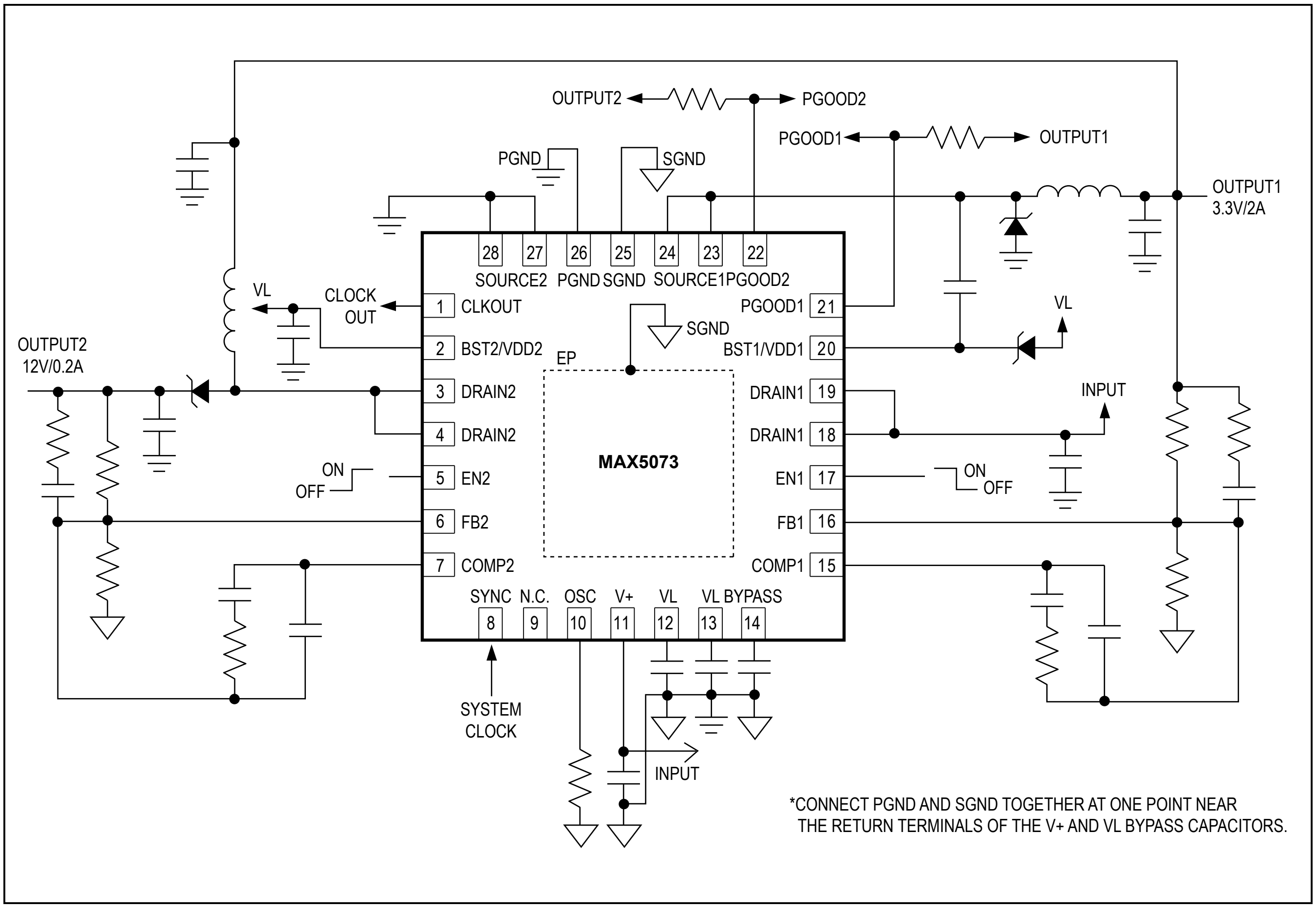


Figure 8. Buck-Boost Application

Boost Converter Compensation

The boost converter compensation gets complicated due to the presence of a right-half-plane zero $f_{ZERO,RHP}$. The right-half-plane zero causes a drop in-phase while adding positive (+1) slope to the gain curve. It is important to drop the gain significantly below unity before the RHP frequency. Use the following procedure to calculate the compensation components.

1) Calculate the LC double-pole frequency, F_{LC}, and the right half plane zero frequency.

$$f_{LC}=\frac{1-D}{2\pi\times\sqrt{L_{OUT}C_{OUT}}}$$

$$f_{ZERO,RHP}=\frac{(1-D)^2R_{(MIN)}}{2\pi\times L_{OUT}}$$

where:

$$D=1-\frac{V_{IN}}{V_{OUT}}$$

$$R_{(MIN)}=\frac{V_{OUT}}{I_{OUT(MAX)}}$$

Target the unity-gain crossovfrequency for:

$$f_C\le\frac{f_{ZERO,RHP}}{5}$$

2) Place a zero $\left(f_{Z1}=\frac{1}{2\pi\times R_F\times C_F}\right)$ at 0.75 x f_{LC}.

$$C_F=\frac{1}{2\pi\times0.75\times f_{LC}\times R_F}$$

where $R_F \ge 10k\Omega$.

3) Calculate C_I for a target crossoverequency, f_C:

$$C_I = \frac{V_{OSC}\left[(1-D)^2 + \omega_C{}^2 L_O C_O\right]}{\omega_C R_F V_{IN}}$$

where $\omega C = 2\pi\ f_C$

4) Place a pole $\left(f_{P1} = \frac{1}{2\pi \times R_I \times C_I}\right)$ at $f_{ZERO,RHP}$.

$$R_I = \frac{1}{2\pi \times f_{ZERO}{,}R_{HP} \times C_I}$$

5) Place the second zero $\left(f_{Z2} = \frac{1}{2\pi \times R1 \times C_I}\right)$ at f_{LC}.

$$R1 = \frac{1}{2\pi \times f_{LC} \times C_I} - R_I$$

6) Place the second pole $\left(f_{P2} = \frac{1}{2\pi \times R_F \times C_{CF}}\right)$ at 1/2 the swhing frequency.

$$C_{CF} = \frac{C_F}{(2\pi \times 0.5 \times f_{SW} \times R_F \times C_{F)-1}}$$

Improving Noise Immunity

In applications where the MAX5073 are subject to noisy environments, adjust the controller's compensation to improve the system's noise immunity. In particular, high-frequency noise coupled into the feedback loop causes jittery duty cycles. One solution is to lower the crossover frequency (see the *Compensation section*).

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. This is especially true for dual converters where one channel can affect the other. Refer to the MAX5073 EV kit data sheet for a specific layout example. Use a multilayer board whenever possible for better noise immunity. Follow these guidelines for good PC board layout:

1) For SGND, use a large copper plane under the IC and solder it to the exposed paddle. To effectively use this copper area as a heat exchanger between the PC board and ambient, expose this copper area on the top and bottom side of the PC board. Do not make a direct connection from the exposed pad copper plane to SGND (pin 25) underneath the IC.
2) Isolate the power components and high-current path from the sensitive analog circuitry.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
4) Connect SGND and PGND together close to the IC at the ground terminals of VL and V+ bypass capacitors. Do not connect them together anywhere else.
5) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PC boards (2oz vs. 1oz) to enhance full-load efficiency.
6) Ensure that the feedback connection to C_{OUT} is short and direct.
7) Route high-speed switching nodes (BST_/VDD_, SOURCE_) away from the sensitive analog areas (BYPASS, COMP_, and FB_). Use the internal PC board layer for SGND as EMI shields to keep radiated noise away from the IC, feedback dividers, and analog bypass capacitors.

Layout Procedure

1) Place the power components first, with ground terminals adjacent (inductor, $C_{IN\_}$, and $C_{OUT\_}$). Make all these connections on the top layer with wide, copper-filled areas (2oz copper recommended).
2) Group the gate-drive components (bootstrap diodes and capacitors, and VL bypass capacitor) together near the controller IC.
3) Make the DC-DC controller ground connections as follows:
    a) Create a small-signal ground plane underneath the IC.
    b) Connect this plane to SGND and use this plane for the ground connection for the reference (BYPASS), enable, compensation components, feedback dividers, and OSC resistor.
    c) Connect SGND and PGND together near the input bypass capacitors and the IC (this is the only connection between SGND and PGND).

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE
MAX5073ETI	-40°C to +125°C	28 Thin QFN-EP* (5mm x 5mm)	T2855-6
MAX5073ETI+	-40°C to +125°C	28 Thin QFN-EP* (5mm x 5mm)	T2855-6

**EP = Exposed pad.*

+Denotes lead-free package.

Chip Information

TRANSISTOR COUNT: 5994

PROCESS: BiCMOS

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
5	5/14	Removed automotive reference under *Applications* section on Page 1	1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.