International
IOR Rectifier

Data Sheet No. PD60230 revC

IR1150(S)(PbF)
IR1150I(S)(PbF)

µPFC ONE CYCLE CONTROL PFC IC

Features

- PFC with IR proprietary “One Cycle Control”
- Continuous conduction mode (CCM) boost type PFC
- No line voltage sense required
- Programmable switching frequency (50kHz-200kHz)
- Programmable output overvoltage protection
- Brownout and output undervoltage protection
- Cycle-by-cycle peak current limit
- Soft start
- User initiated micropower “Sleep Mode”
- Open loop protection
- Maximum duty cycle limit of 98%
- User programmable fixed frequency operation
- Min. off time of 150-350ns over freq range
- V_{CC} under voltage lockout
- Internally clamped 13V gate drive
- Fast 1.5A peak gate drive
- Micropower startup (<200 µA)
- Latch immunity and ESD protection
- Parts also available Lead-Free

Description

The µPFC IR1150 is a power factor correction (PFC) control IC designed to operate in continuous conduction mode (CCM) over a wide range input line voltages. The IR1150 is based on IR's proprietary "One Cycle Control" (OCC) technique providing a cost effective solution for PFC.

The proprietary control method allows major reductions in component count, PCB area and design time while delivering the same high system performance as traditional solutions.

The IC is fully protected and eliminates the often noise sensitive line voltage sensing requirements of existing solutions.

The IR1150 features include programmable switching frequency, programmable dedicated over voltage protection, soft start, cycle-by-cycle peak current limit, brownout, open loop, UVLO and micropower startup current.

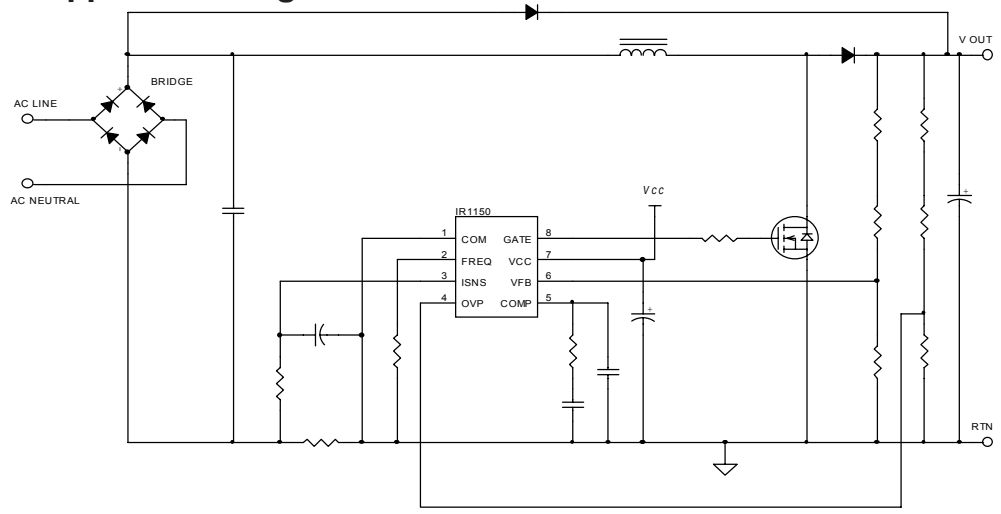
In addition, for low standby power requirements (Energy Star, 1W Standby, Blue Angel, etc.), the IC can be driven into sleep mode with total current consumption below 200µA, by pulling the OVP pin below 0.62V.

Packages


8-Lead SOIC


8-Lead PDIP

IR1150 Application Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltages are absolute voltages referenced to COM. Thermal resistance and power dissipation are measured under board mounted and still air conditions.

Parameters	Symbols	Min.	Max.	Units	Remarks
V_{CC} voltage	V_{CC}	-0.3	22	V	Not internally clamped
Freq. voltage	$V_{FREQ.}$	-0.3	10.5	V	
I_{SNS} voltage	V_{ISNS}	-10	3	V	
V_{FB} voltage	V_{FB}	-0.3	10.5	V	
COMP voltage	V_{COMP}	-0.3	10	V	
Gate voltage	V_{GATE}	-0.3	18	V	
Continuous gate current	I_{GATE}	-5	5	mA	
Max peak gate current	I_{GATEPK}	-1.5	1.5	A	
Junction temperature	T_J	-40	150	°C	
Storage temperature	T_S	-55	150	°C	
Thermal resistance	$R_{\theta JA}$	—	128	°C/W	SOIC-8
		—	84	°C/W	PDIP-8
Package power dissipation	P_D	—	675	mW	SOIC-8 T_{AMB} = 25°C
		—	1000	mW	PDIP-8 T_{AMB} = 25°C
ESD protection	V_{ESD}	—	2	kV	Human body model*

Recommended Operating Conditions

Recommended operating conditions for reliable operation with margin

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Supply voltage	V_{CC}	15	18	20	V	
Junction temperature	T_J	-25	—	125	℃	
Ambient temperature	T_A	0	—	70	℃	IR1150(S)
Ambient temperature	T_A	-25	—	85	℃	IR1150I(S)
Switching frequency	F_{SW}	50	—	200	kHz	

Electrical Characteristics

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from – 25 ° C to 125°C. Typical values represent the median values, which are related to 25°C. **If not otherwise stated, a supply voltage of V_{CC} =15V is assumed for test condition**

Supply Section

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
V_{CC} turn-on threshold	$V_{CC\ ON}$	12.2	12.7	13.2	V	
V_{CC} turn-off threshold (under voltage lock out)	$V_{CC\ UVLO}$	10.2	10.7	11.2	V	

*Per EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5KΩ series resistor)

Electrical Characteristics cont.

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from – 25° C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} =15V is assumed for test condition.

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
V_{CC} turn-off hysteresis	$V_{CC\ HYST}$	1.8	—	2.2	V	
Operating current	I_{CC}	—	18	22	mA	C_{LOAD}=1nF f_{SW}=200kHZ
		—	36	40	mA	C_{LOAD}=10nF f_{SW}=200kHZ
		—	8	10	mA	Standby mode - inactive gate Internal oscillator running
Startup current	$I_{CCSTART}$	—	—	175	uA	V_{CC}=$V_{CC\ ON}$ -0.1V
Sleep current	I_{SLEEP}	—	125	200	uA	V_{OVP}<0.5V (typ),V_{CC} =15V

Oscillator Section

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Switching frequency	f_{SW}	50	—	200	kHz	R_{SET} = 165kΩ -37kΩ approx.
Initial accuracy	$f_{SW\ ACC}$	—	—	5	%	T_A = 25°C
Voltage stability	V_{STAB}	—	0.2	3	%	13V <V_{CC} <20V
Temperature stability	T_{STAB}	—	2	—	%	-25°C ≤T_J≤125°C
Total variation	f_{VT}	—	10	—	%	Line & temperature
Long term stability	F_{STABLT}	—	0.1	0.5	%	T_{AMB} = 125°C, 1000Hrs
Maximum duty cycle	D_{MAX}	93	—	98	%	f_{SW}=200kHz
Minimum duty cycle	D_{MIN}	—	—	0	%	
Minimum off time	T_{offmin}	200	300	400	ns	f_{SW}=50kHz to 200kHz

Protection Section

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Open loop protection (OLP) Vfb threshold	V_{OLP}	17	19	21	%V_{REF}	
Output under voltage protection (OUV)	V_{OUV}	49	51	53	%V_{REF}	Brown out protection
Output over voltage protection (OVP)	V_{OVP}	104	105.5	107	%V_{REF}	
OVP hysteresis	—	350	450	550	mV	
Peak current limit protection (I_{PKLMT}) I_{SNS} voltage threshold	V_{ISNS}	-1.11	-1.04	-0.96	V	

Internal Voltage Reference Section

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Reference voltage	V_{REF}	6.9	7.0	7.1	V	$T_A = 25^oC$
Line regulation	R_{REG}	—	12	25	mV	$13.5V < V_{CC} < 20V$
Temp stability	T_{STAB}	—	0.4	—	%	$-25^oC \leq T_{AMB} \leq 125^oC$
Total variation	ΔV_{TOT}	6.8	—	7.1	V	Over V_{CC} and T_j ranges

Voltage Error Amplifier Section

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Transconductance	g_m	30	40	55	µS	$-25^oC \leq T_{AMB} \leq 125^oC$
Source/sink current		30	40	65	µA	$T_{AMB} = 25^oC$
	I_{OVEA}	20	45	90	µA	$-25^oC \leq T_{AMB} \leq 125^oC$
Soft start delay time (calculated)	t_{ss}	—	40	—	ms	R_{GAIN}=1kΩ, C_{ZERO}=0.33µF C_{POLE}=0.01µF, f_{XO}=28Hz
V_{COMP} voltage (fault)	$V_{COMP\ FLT}$	—	1.2	1.5	V	@ 1mA (max) initial
				0.2	V	@ 25µA steady state
Effective V_{COMP} voltage	$V_{COMP\ EFF}$		6.05		V	
Input bias current	I_{IB}	—	-0.2	-0.5	µA	V_{FB}=0V, $-25^oC \leq T_{AMB} \leq 125^oC$
Open loop bandwidth	BW	—	1	—	MHz	
Input offset voltage temp coefficient	TC_{IOV}	—	—	10	µV/°C	Note 1
Common mode rejection ratio	CMRR	—	100	—	dB	
Output low voltage	V_{OL}	—	—	0.5	V	
Output high voltage	V_{OH}	5.71	6.15	6.8	V	
V_{COMP} start voltage	$V_{COMP\ START}$	300	500	700	mV	

Current Amplifier Section

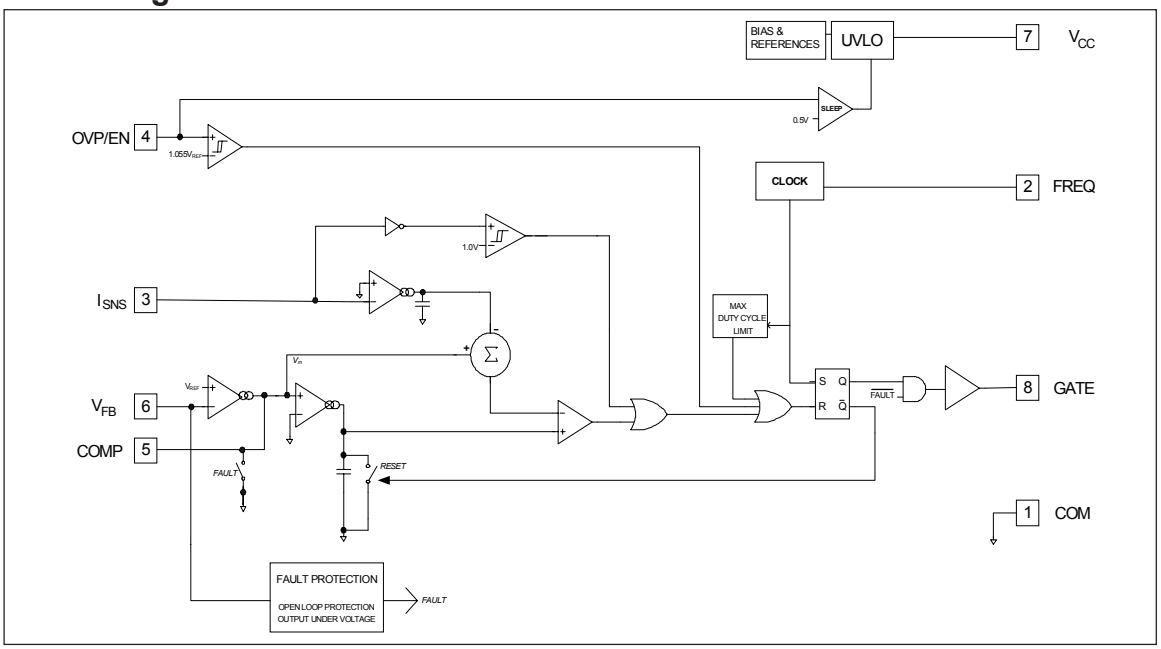
Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
DC gain	g_{DC}	—	2.5	—	V/V	
Corner frequency	f_C	200	—	280	kHz	Note 1
Input offset voltage	V_{IO}	—	1	4	mV	Note 1
I_{SNS} bias current	I_{IB}	—	200	300	µA	V_{FB}=0V,$-25^oC \leq T_{AMB} \leq 125^oC$
Input offset voltage temp coefficient	TC_{IOV}	—	—	10	µV/°C	Note 1
Common mode rejection ratio	CMRR	—	100	—	dB	
Blanking time	T_{BLANK}	230	350	450	ns	$T_{AMB} = 25^oC$
		150		600	ns	$-25^oC \leq T_{AMB} \leq 125^oC$

Gate Driver Section

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Gate low voltage	V_{GLO}	—	1.2	1.5	V	I_{GATE}=200mA
Gate high voltage	V_{GTH}	—	13	18	V	V_{CC}=20V
Gate high voltage	V_{GTH}	9.5	—	—	V	V_{CC} =11.5V
Rise time	t_r	—	20	—	ns	C_{LOAD} = 1nF, V_{CC}=16V
		—	70	—	ns	C_{LOAD} = 10nF, V_{CC}=16V
Fall time	t_f	—	20	—	ns	C_{LOAD} = 1nF, V_{CC}=16V
		—	70	—	ns	C_{LOAD} = 10nF, V_{CC}=16V
Out peak current	I_{OPK}	1.5	—	—	A	C_{LOAD} = 10nF, V_{CC}=16V
Gate voltage @ fault	$V_{G\ fault}$	—	—	1.8	V	I_{GATE}=20mA

Note 1: Guaranteed by design, but not tested in production.

Block Diagram



Lead Assignments & Definitions

Lead Assignment	Pin#	Symbol	Description
IR1150 COM 1 — 8 GATE FREQ 2 — 7 V_{CC} I_{SNS} 3 — 6 V_{FB} OVP/EN 4 — 5 COMP	1	COM	Ground
	2	FREQ	Frequency Set
	3	I_{SNS}	Current Sense
	4	OVP/EN	Overvoltage Fault Detect / Enable
	5	COMP	Voltage Loop Compensation
	6	V_{FB}	Output Voltage Sense
	7	V_{CC}	IC Supply Voltage
	8	GATE	Gate Drive Output

General Description

The μPFC IR1150 is intended for boost converters for power factor correction operating at a fixed frequency in continuous conduction mode. The IC operates with two loops; an inner current loop and an outer voltage loop. The inner current loop is fast, reliable and does not require sensing of the input voltage in order to create a current reference.

This inner current loop sustains the sinusoidal profile of the average input current based on the dependency of the pulse width modulator duty cycle on the input line voltage in order to determine the analogous input line current. Thus, the current loop uses the embedded input voltage signal to control the average input current to follow the input voltage.

The IR1150 enables excellent THD performance. In light load conditions, a small distortion occurs at zero-crossing due to the finite boost inductance but this is negligible and well within EN61000-3-2 Class D specifications.

The outer voltage loop controls the DC bus voltage. This voltage is fed into the voltage error amplifier to control the slope of the integrator ramp and sets the amplitude of the average input current.

The two loops combine to control the amplitude, phase and shape of the input current, with respect to the input voltage, giving near-unity power factor.

The IC is designed for robust operation and provides protection from system level over current, over voltage, under voltage, and brownout conditions.

IC Supply

The UVLO circuit monitors the V_{CC} pin and maintains the gate drive signal inactive until the V_{CC} pin voltage reaches the UVLO turn on threshold, ($V_{CC\ ON}$). As soon as the V_{CC} voltage exceeds this threshold, provided that the V_{FB} pin voltage is greater than 20%V_{REF}, the gate drive will begin switching (under Soft Start) and increase the pulse width to its maximum value as demanded by the output voltage error amplifier. If the voltage on the V_{CC} pin falls below the UVLO turn off threshold, ($V_{CC\ UVLO}$), the IC turns off, gate drive is terminated, and the turn on threshold must again be exceeded in order to re-start the process and move into Soft Start mode.

Soft Start

Soft Start controls the rate of rise of the output voltage error amplifier in order to obtain a linear control of the increasing duty cycle as a function of time. The Soft Start time is controlled by voltage error amplifier compensation components selected, and is user programmable based on desired loop crossover frequency.

Frequency Select

The switching frequency of the IC is programmable by an external resistor at the FREQ pin. The design incorporates min/max restrictions such that the minimum and maximum operating frequency fall within the range of 50-200kHz.

Gate Drive

The gate drive is a totem pole driver with 1.5A capability. If higher currents are required, additional external drivers can be used.

Detailed Pin Description

COM: Ground
This is the ground potential pin of the integrated control circuit. All internal devices are referenced to this point.

V_{FB}: Output Voltage Feedback
The output voltage of the boost converter is sensed via a resistive divider and fed into this pin, which is the inverting input of the output voltage error amplifier. The impedance of the divider string must be low enough so as to not introduce substantial error due to the input bias currents of the amplifier, yet high enough so as to minimize power dissipation. A typical value of external divider impedance is 1MΩ.
The error amplifier is a transconductance type which yields high output impedance, thus increasing the noise immunity of the error amplifier output. This also eliminates input divider string interaction with compensation feedback capacitors and reducing the loading of divider string due to a low impedance output of the amplifier.

COMP: Voltage Loop Compensation
External circuitry from this pin to ground compensates the system voltage loop and soft start time. This is the output of the voltage error amplifier. This pin will be discharged via internal resistance when a fault mode occurs.

GATE: Gate Drive Output
This is the gate drive output of the IC. Drive voltage is internally limited and provides ±1.5A peak with matched rise and fall times.

FREQ: Frequency Set
This is the user programmable frequency pin. An external resistor from this pin to the COM pin programs the frequency. The operational switching frequency range for the device is 50kHz – 200kHz.

I_{SNS}: Current Sense input
This pin is the inverting Current Sense Input & Peak Current Limit. The voltage at this pin is the negative voltage drop, sensed across the system current sense resistor, representing the inductor current.
This voltage is fed into the Peak Current Limit protection comparator with threshold arond -1V. This protection circuit incorporates a leading edge blanking circuit following the comparator to improve noise immunity of the protection process.
The current sense signal is also fed into the current sense amplifier. The signal is amplified, filtered of high frequency noise and then injected into a summing node where it is subtracted from the compensation voltage V_{COMP}.
The signal on this pin must be previously filtered with an RC cell to provide additional noise immunity. The input impedance of this pin is 5kΩ.

V_{CC}: Supply Voltage
This is the supply voltage pin of the IC and it is monitored by the under voltage lockout circuit. It is possible to turn off the IC by pulling this pin below the minimum turn off threshold voltage, without damage to the IC.
To prevent noise problems, a bypass ceramic capacitor connected to V_{CC} and COM should be placed as close as possible to the IR1150.
This pin is not internally clamped, therefore damage will occur if the maximum voltage is exceeded.

OVP/EN: Over Voltage Protection / Enable
This pin is the input to the over voltage protection comparator the threshold of which is internally programmed to 105.5% of V_{REF}.
A resistive divider feeds this pin from the output voltage to COM and inhibits the gate drive whenever the threshold is exceeded. Normal operation resumes when the voltage level on this pin decreases to below the pin threshold.
This pin is also used to activate “sleep” mode by pulling the voltage level below 0.62V (typ).

Operating States

UVLO Mode

The IC remains in the UVLO condition until the voltage on the V_{CC} pin exceeds the V_{CC} turn on threshold voltage, $V_{CC\ ON}$.

During the time the IC remains in the UVLO state, the gate drive circuit is inactive and the IC draws a quiescent current of $I_{CC\ START}$. The UVLO mode is accessible from any other state of operation whenever the IC supply voltage condition of $V_{CC} < V_{CC\ UVLO}$ occurs.

Standby Mode

The IC is in this state if the supply voltage has exceeded $V_{CC\ ON}$ and the V_{FB} pin voltage is less than 20% of V_{REF} . The oscillator is running and all internal circuitry is biased in this state but the gate is inactive. This state is accessible from any other state of operation except OVP. The IC enters this state whenever the V_{FB} pin voltage has decreased to 50% of V_{REF} when operating in normal mode or during a peak current limit fault condition, or 20% V_{REF} when operating in soft start mode.

Soft Start Mode

This state is activated once the V_{CC} voltage has exceeded V_{CCON} and the V_{FB} pin voltage has exceeded 20% of V_{REF}.

The soft start time, which is defined as the time required for the duty cycle to linearly increase from zero to maximum, is dependent upon the values selected for compensation of the voltage loop pin COMP to pin COM. Throughout the soft start cycle, the output of the voltage error amplifier (pin COMP) charges through the compensation network. This forces a linear rise of the voltage at this node which in turn forces a linear increase in the gate drive duty cycle from 0. This controlled duty cycle reduces system component stress during start up conditions as the input current amplitude is increasing linearly.

Normal Mode

The IC enters normal operating mode once the soft start transition has been completed. At this point the gate drive is switching and the IC draws a maximum of I_{CC} from the supply voltage source. The device will initiate another soft start sequence in the event of a shutdown due to a fault, which activates the protection circuitry, or if the supply voltage drops below the UVLO turn off threshold of $V_{CC\ UVLO}$.

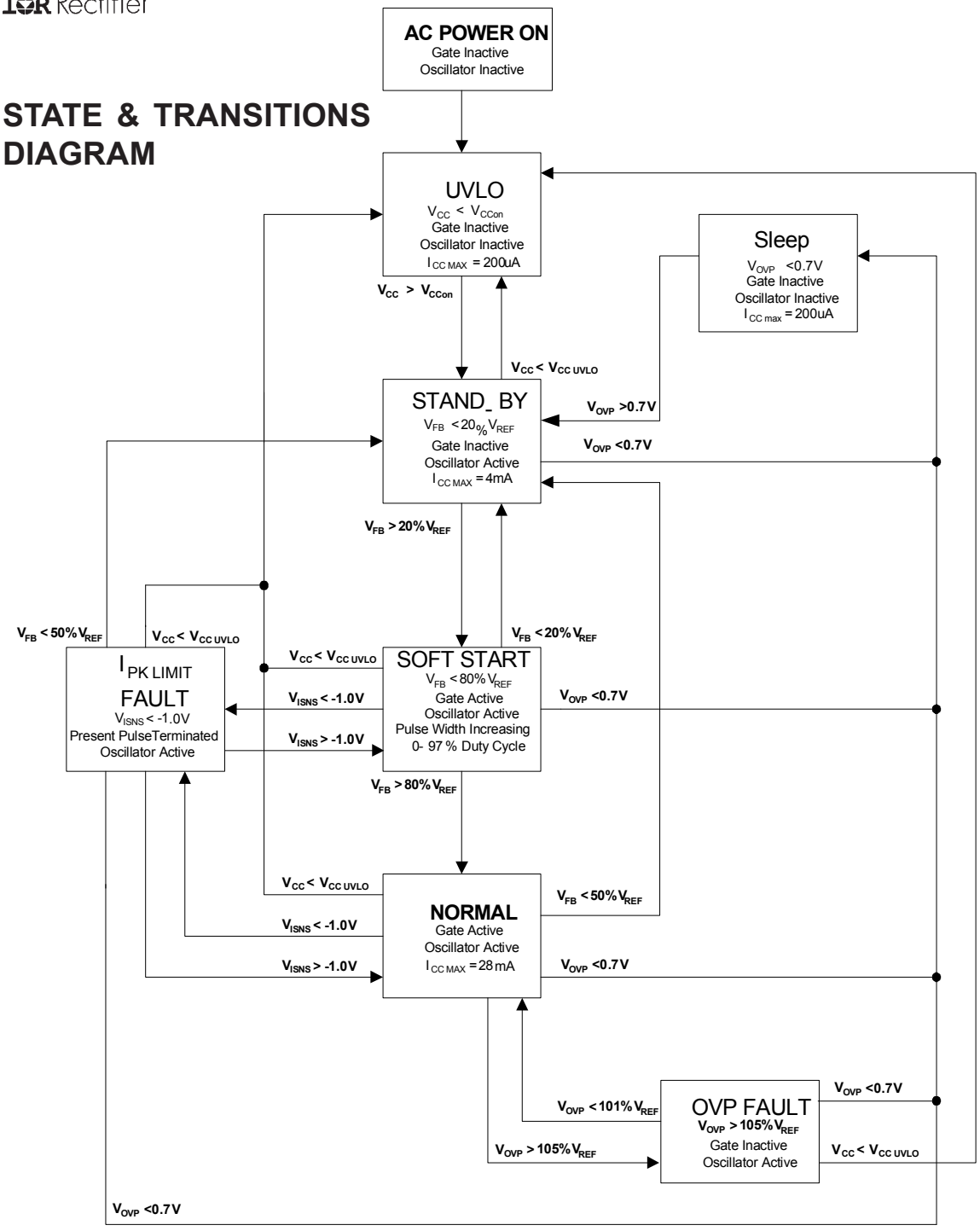
Fault Protection Mode

The fault mode will be activated when any of the protection circuits are activated. The IC protection circuits include Supply Voltage Under Voltage Lockout (UVLO), Output Over Voltage Protection (OVP), Open Loop Protection (OLP), Output Undervoltage Protection (OUV), and Peak Current Limit Protection ($I_{PK\ LIMIT}$).

Sleep Mode

The sleep mode is initiated by pulling the OVP pin below 0.62V (typ). In this mode the IC draws a very low quiescent supply current.

STATE & TRANSITIONS DIAGRAM



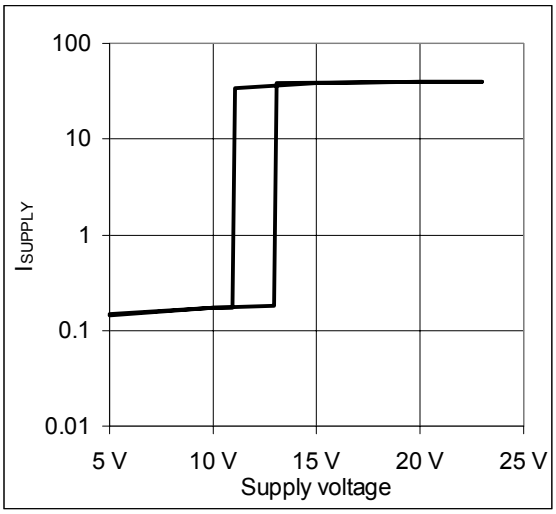


Fig.1 - Supply Current

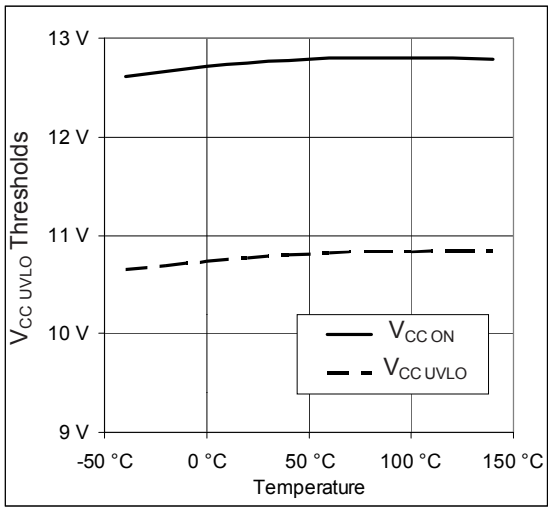


Fig. 2 - Under Voltage Lockout vs. Temperature

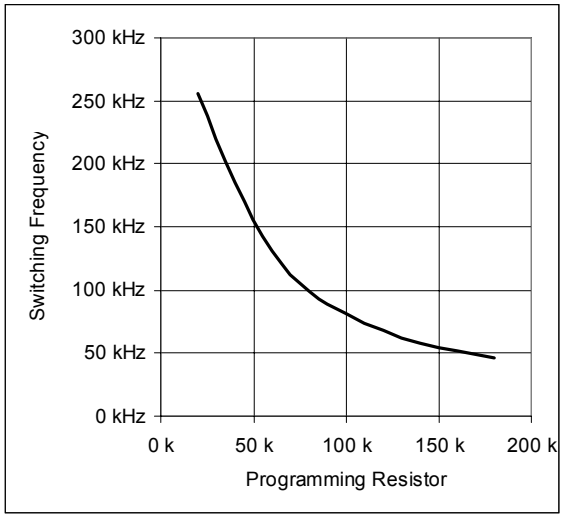


Fig. 3 - Oscillator Frequency vs. Programming Resistor

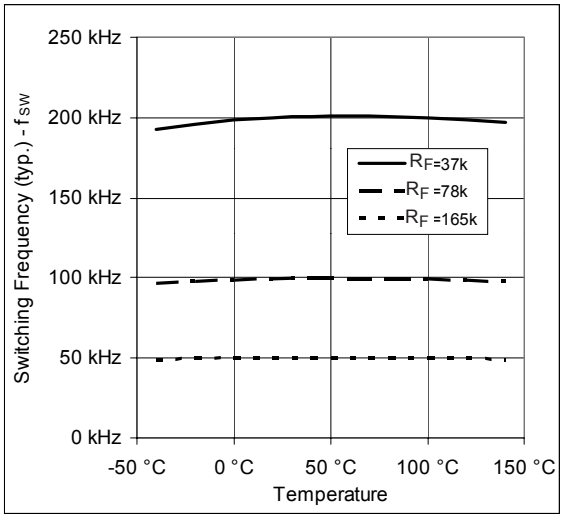


Fig. 4 - Oscillator Frequency vs. Temperature

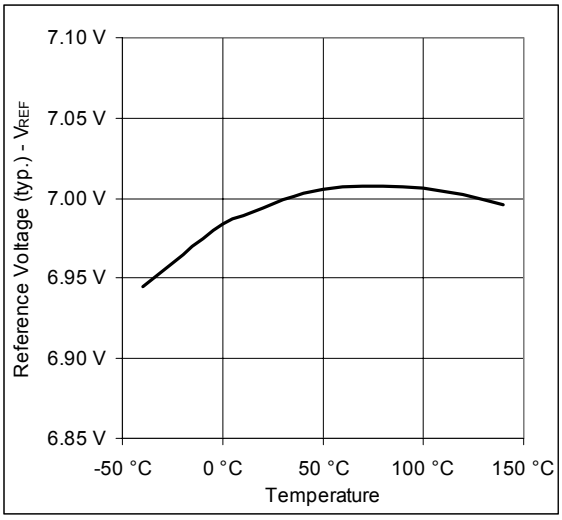


Fig. 5 - Reference Voltage

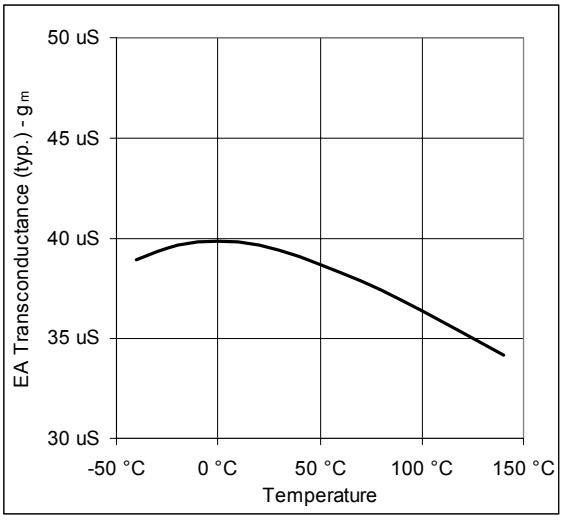


Fig. 6 - Voltage Error Amplifier Transconductance

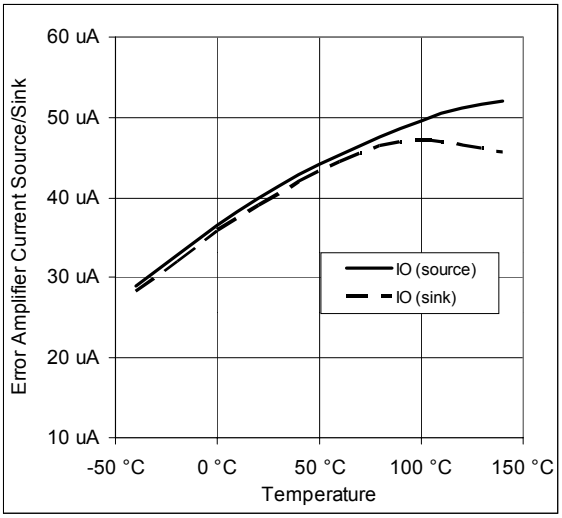


Fig.7 - Voltage Error Amplifier Source/Sink Current

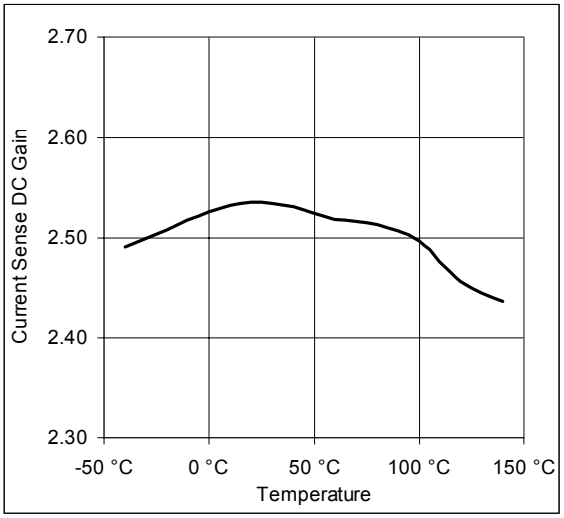
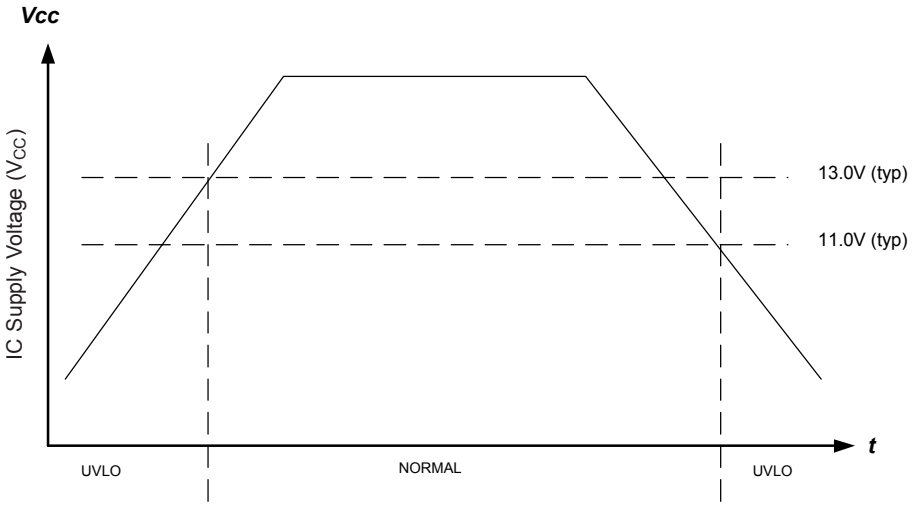
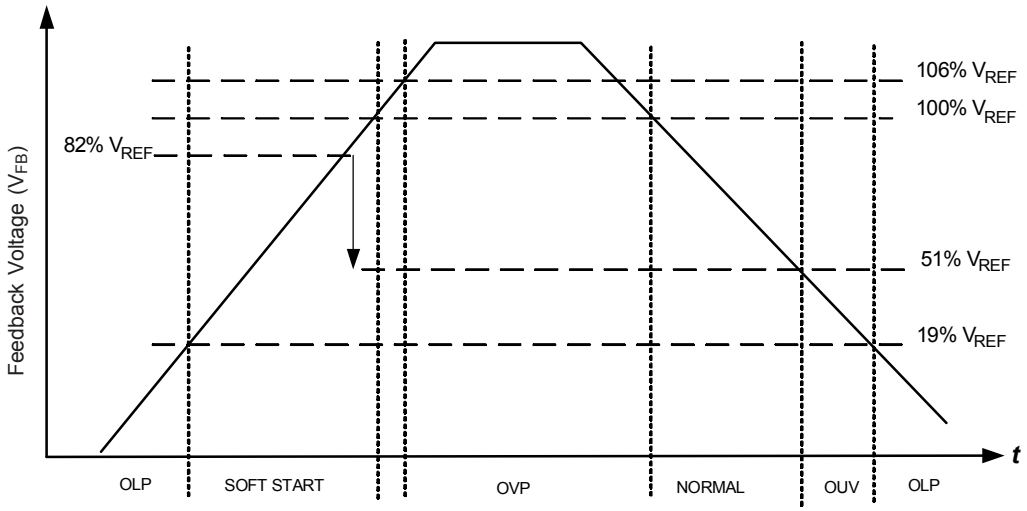


Fig. 8 - Current Sense Amplifier DC Gain

IR1150 Timing Diagrams

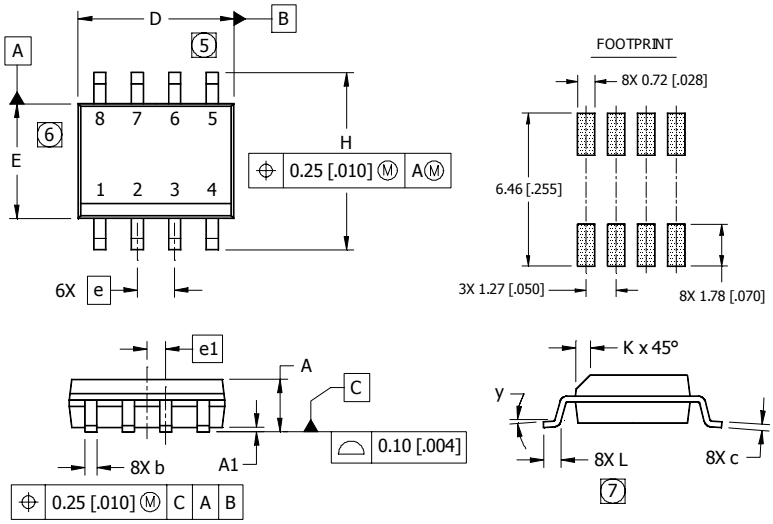


V_{cc} Under Voltage Lockout



Output Protection

Case outline



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

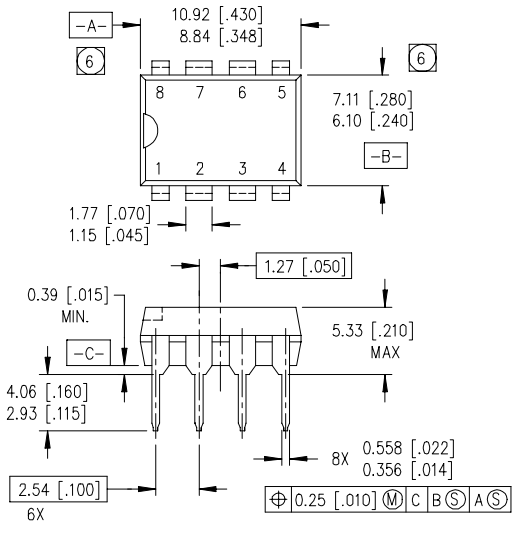
5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

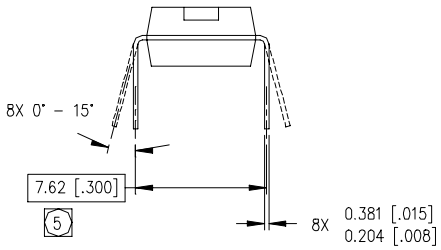
8-Lead SOIC



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.

5 MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

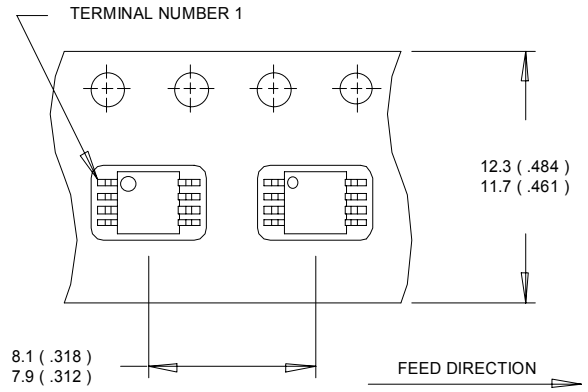


01-6014
01-3003 01 (MS-001AB)

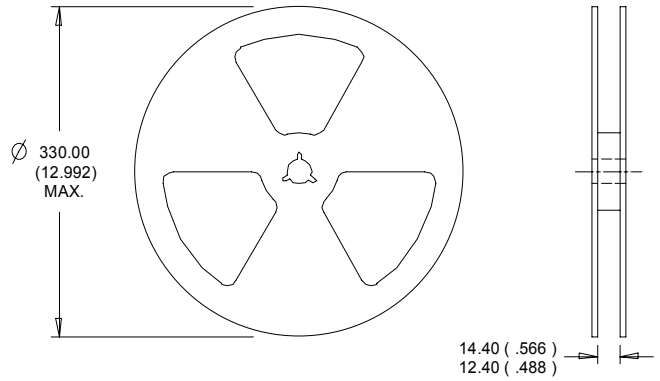
8-Lead PDIP

Tape & Reel Information (SOIC 8-Lead only)

Dimensions are shown in millimeters (inches)



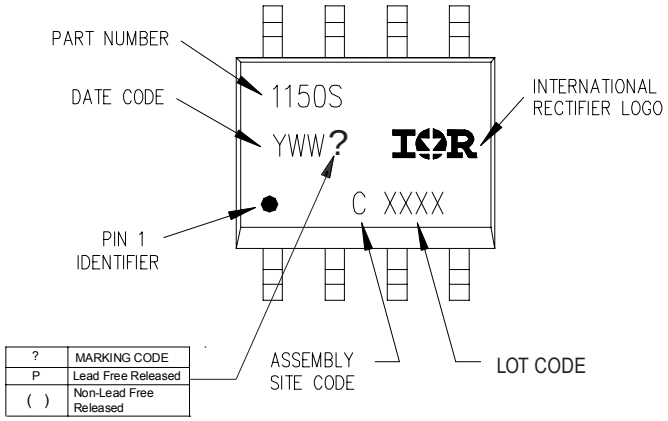
NOTES:
1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. CONTROLLING DIMENSION : MILLIMETER.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

PART MARKING INFORMATION

TOP MARKING (LASER)



ORDER INFORMATION

Basic Part

8-Lead SOIC IR1150STR order IR1150STR
8-Lead SOIC IR1150ISTR order IR1150ISTR

Lead-free Part

8-Lead SOIC IR1150S order IR1150STRPbF
8-Lead SOIC IR1150ISTR order IR1150ISTRPbF
8-Lead PDIP IR1150 order IR1150PbF
8-Lead PDIP IR1150I order IR1150IPbF

International
IOR Rectifier

The IR1150(S)(PbF) has been designed and qualified for the Consumer Market
The IR1150I(S)(PbF) has been designed and qualified for the Industrial Market
Qualification Standards can be found on IR's Web site.

WORLD HEADQUARTERS: 233 Kansas Street, El Segundo, California 90245 Tel: (310) 252-7105
http://www.irf.com/ Data and specifications subject to change without notice. 2/5/2007