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TUTORIAL 872

LVDS Splitter Simplifies High-Speed Signal Distribution

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Abstract: The ANSI EIA/TIA-644 standard for low voltage differential signaling (LVDS) offers lower power and lower noise emission than the more traditional ECL, PECL, and CML standards for high-speed signal distribution. This application note compares some of the characteristics of these communication standards and discusses some of the advantages of the LVDS standard.

Introduction

As the clock frequencies of microprocessors, DSPs and digital ASICs increase, so does the speed of backplane signals. Faster clock rates strain the limits of single-ended TTL-based signaling. This strain, in turn, brings increased power dissipation; ringing, which leads to bit errors; high levels of radiated emission; transmission-line effects such as impedance mismatch and crosstalk; difficulties decoupling the power supply and other problems. Despite reports that speeds greater than 50MHz can be maintained with this technology, other signaling techniques are worth considering.

One way to increase overall bus and/or backplane bandwidth is to increase the bus width. However, this approach complicates PC-board layout and requires high-pin-count connectors, which are expensive and unwieldy. Serial data streams are attractive when distances exceed a few centimeters. High-speed data-communication systems that can benefit from serial data streams include third-generation basestations, routers, add-drop multiplexers, and other equipment.

Low-voltage differential signaling (LVDS) can replace TTL and enable backplane communication with low error rates, reduced crosstalk, and low radiated emission.

Characteristics of LVDS, ECL, PECL, and CML

LVDS is seeing increased use in high-speed systems where signal integrity, low-jitter (jitter can be defined as the deviation in a signal's output transitions from their ideal positions in time) and good common-mode performance are required. LVDS is among the signaling techniques used for high-speed serial interfaces.

Other signaling techniques (ranked in approximate order of speed from slowest to fastest) are ECL (emitter-coupled logic), PECL (positive ECL), and CML (current-mode logic). Note that every one of these signaling techniques is differential.

ECL is the traditional high-speed logic technology, originally based on bipolar transistor differential pairs. In its initial form it uses a negative bias supply. PECL is a form of ECL that is referenced to the positive supply. The latest generation of ECL devices exhibit propagation delays in the region of 200ps and toggle frequencies over 3GHz.

Of all the interfaces available today, CML operates at the highest speed and is used in applications requiring gigabit data rates. CML has an additional advantage over the other techniques: it includes an integrated 50Ω termination, which considerably simplifies the task of ensuring good matching all the way to the silicon. Some external coupling components are needed, however, if each end of the link operates at a different supply voltage.

This article focuses on the characteristics of LVDS and its possible applications. **Table 1** lists some of those characteristics and compares them with those found in ECL, PECL, and CML systems. As specified in the EIA/TIA-644 LVDS and IEEE® 1596.3 standards, LVDS uses differential signals of an amplitude ranging from 250mV to 400mV at an offset of 1.2V.

Table 1. Comparison of High-Speed Signaling Systems*

	LVDS	ECL	PECL	CML
Differential Voltage Swing	250mV to 400mV	~0.8V	~0.8V	0.4V
DC Offset	1.2V	-1.3V	V_{CC} - 1.3V	V_{CC} - 0.2V
Propagation Delay	~1ns	200ps	200ps	Technology dependent

*ECL and PECL transmitter-output signal swings are higher than those of LVDS transmitters. The higher signal swings and the shorter propagation delays exhibited by ECL and PECL devices come at the cost of higher power dissipation.

Advantages of LVDS

Many of the advantages of LVDS derive from its differential nature: it is immune to common-mode noise and, in theory, emits no noise itself. (This assumes completely symmetrical differential signals, i.e., no skew between the positive and negative outputs.) LVDS can be implemented in CMOS, which simplifies its integration with other circuits.

Since LVDS is differential, the magnitude of current spikes drawn from its power supplies is lower and can be handled easier with suitably placed decoupling capacitors of reasonable value. Also, LVDS generally dissipates less power than ECL and CML, although this depends to some extent on the termination techniques used.

Applications of LVDS

Among the many applications for which LVDS is well-suited are clock distribution and multiple point-to-point signal distribution. Clock distribution is of great importance in digital systems where different subsystems are required to work with the same clock reference. For example, the DSP section of a basestation must, in most cases, be synchronized to the radio-frequency signal processing section, which is where phase-locked loops (PLLs) produce the required local oscillator frequencies and where ADCs are locked to the central clock reference. Also, when working with applications that include radio receivers, the clock (and the signals) must be distributed with the lowest possible emission levels to avoid interfering with low-level signal paths.

When distributing high-speed signals to different destinations, various strategies can be employed. Two approaches represent the extremes within which you find the range of strategies: one, drive all destinations from a single source/driver (called multidrop distribution); two, use a separate driver for each destination (called multiple point-to-point distribution). **Figure 1** shows the difference between these two types of distribution schemes with two typical techniques. In multidrop distribution, a driver of sufficient drive capability drives all receivers and the intervening media (cable, connectors(s), backplane). The bus is usually terminated in its characteristic impedance at the final receiver. Efforts must be made to keep all "stubs" or branches from the bus as short as possible to avoid possible signal-integrity problems. On the high-density printed circuit boards of today, controlling stub length is not always simple.
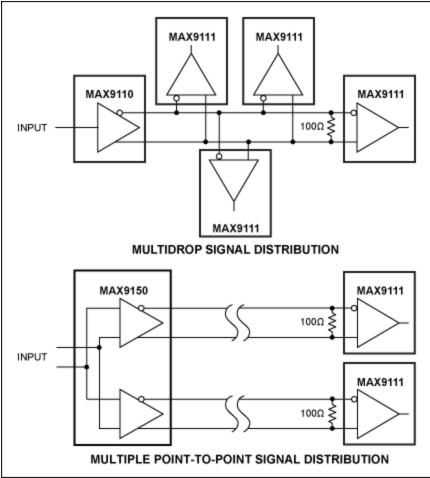

Figure 1. Multidrop signal distribution permits communication between one transmitter and multiple receivers. Multiple point-to-point signal distribution, which does not require tuning stubs, eliminates the disturbances that those stubs can potentially create.

A multiple point-to-point strategy employs multiple drivers, which need only be specified for point-to-point operation, as each driver communicates with a single locally terminated receiver. With this scheme, the problems of signal integrity are reduced to ensuring that the impedance of the medium is as uniform as possible. The disturbance that stubs could potentially cause is eliminated.

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Related Parts		
MAX9110	Single/Dual LVDS Line Driver with Ultra-Low Differential Skew in SOT23	Free Samples
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