16-Lane 4-Port
Gen2 PCI Express® Switch

89HPES16T4AG2
Product Brief

Device Overview

The 89HPES16T4AG2 is a member of IDT's PRECISE™ family of PCI Express® switching solutions. The PES16T4AG2 is a 16-lane, 4-port Gen2 peripheral chip that performs PCI Express Base switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides connectivity and switching functions between a PCI Express upstream port and up to three downstream ports and supports switching between downstream ports.

Features

- – *Sixteen 5 Gbps Gen2 PCI Express lanes*
- – *Four switch ports*
  - • *One x8 or x4 upstream port*
  - • *Up to three x4 downstream ports*
- – *Low latency cut-through switch architecture*
- – *Support for Max Payload Size up to 2048 bytes*
- – *One virtual channel*
- – *Eight traffic classes*
- – *PCI Express Base Specification Revision 2.0 compliant*
- ◆ **Flexible Architecture with Numerous Configuration Options**
- – *Automatic per port link width negotiation to x8, x4, x2 or x1*
- – *Automatic lane reversal on all ports*
- – *Automatic polarity inversion*
- – *Ability to load device configuration from serial EEPROM*

- ◆ **Legacy Support**
- – *PCI compatible INTx emulation*
- – *Bus locking*
- ◆ **Highly Integrated Solution**
- – *Incorporates on-chip internal memory for packet buffering and queueing*
- – *Integrates sixteen 5 Gbps embedded SerDes with 8b/10b encoder/decoder (no separate transceivers needed)*
  - • *Receive equalization (RxEQ)*
- ◆ **Reliability, Availability, and Serviceability (RAS) Features**
- – *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
- – *Supports ECRC and Advanced Error Reporting*
- – *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
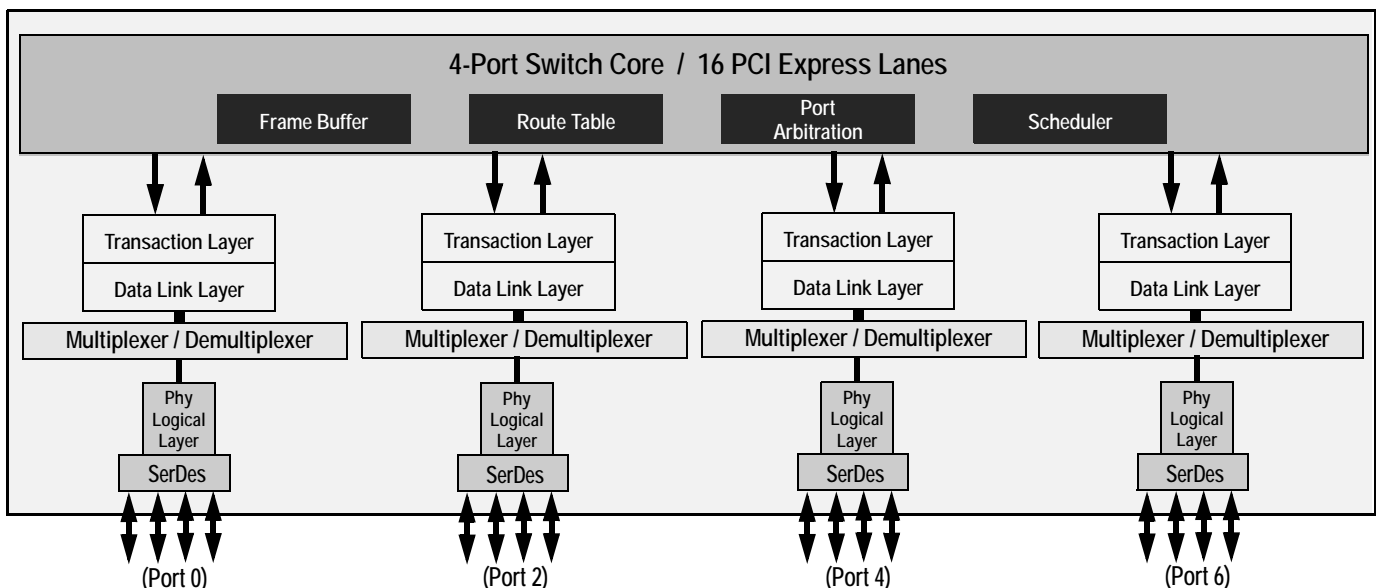- – *Compatible with Hot-Plug I/O expanders used on PC motherboards*
- – *Supports Hot-Swap*

Block Diagram

Figure 1 Internal Block Diagram

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- ◆ Power Management
  - – *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - – *Support PCI Express Power Management Interface specification (PCI-PM 2.0)*
  - – *Unused SerDes are disabled.*
  - – *Supports Advanced Configuration and Power Interface Specification, Revision 2.0 (ACPI) supporting active link state*
- ◆ Testability and Debug Features
  - – *Built in Pseudo-Random Bit Stream (PRBS) generator*
  - – *Numerous SerDes test modes*
  - – *Ability to read and write any internal register via the SMBus*
  - – *Ability to bypass link training and force any link into any mode*
  - – *Provides statistics and performance counters*
- ◆ Sixteen General Purpose Input/Output Pins
  - – *Each pin may be individually configured as an input or output*
  - – *Each pin may be individually configured as an interrupt input*
  - – *Some pins have selectable alternate functions*
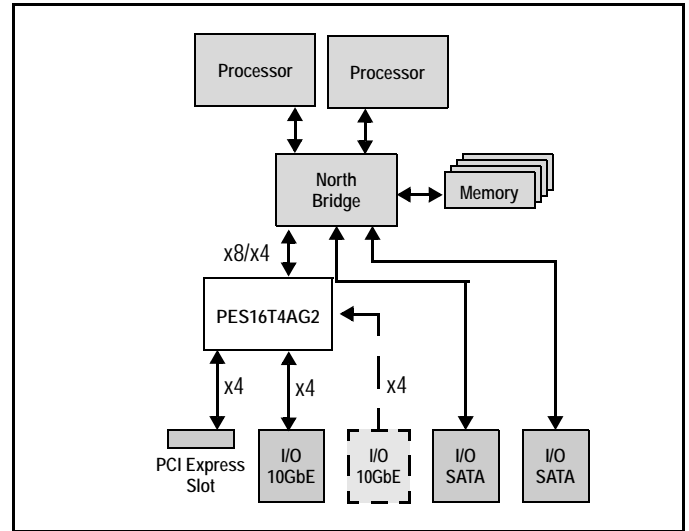- ◆ Packaged in a 19mm x 19mm, 324-ball Flip Chip BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES16T4AG2 provides the most efficient fan-out solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 16 GBps (128 Gbps) of aggregated, full-duplex switching capacity through 16 integrated serial lanes, using proven and robust IDT technology. Each lane provides 5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 2.0.

The PES16T4AG2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES16T4AG2 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

Figure 2 I/O Expansion Application

IDT

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
email: ssdhelp@idt.com
phone: 408-284-8208