Dual Channel 0.47Gbps to 6.25Gbps Multi-Rate Transceiver

Check for Samples: TLK6002

1 Introduction

1.1 Transceiver Features

- **Dual Channel 470Mbps to 6.25Gbps Continuous/Multi-Rate Transceiver**
- **Supports all CPRI and OBSAI Data Rates**
- **Integrated Latency Measurement Function, Accuracy of ±814 ps**
- **CPRI/OBSAI Automated Rate Sense (ARS) Function**
- **Supports SERDES Operation, 8B/10B Data Modes (20-bit and 16-bit + Controls)**
- **20-bit HSTL Single-Ended Parallel Data Interface (Integrated Source and End Termination)**
- **Shared or Independent Reference Clock per Channel**
- **Latency/Depth Configurable Transmit and Receive FIFOs.**
- **Loopback Capability (Serial and Parallel Side), OBSAI Compliant**
- **Supports Serial Retime Operation**
- **Supports PRBS (2^7–1), (2^{23} – 1) and (2^{31}–1) and CRPAT Long/Short Generation and Verification**
- **Dual Power Supply: 1.0V Core, and 1.5V/1.8V I/O Nominal Supply**
- **Serial Side Three Tap Transmit De-emphasis and Receive Adaptive Equalization to Allow Extended Backplane Reach**
- **Programmable Output Swing on Serial Output**
- **Minimum Receiver Differential Input Thresholds of 100mV_{dfpp}**
- **Loss of Signal (LOS) detection (≤75 mV_{dfpp})**
- **Interface to Back Plane, Copper Cables, or Optical Modules**
- **Hot Plug Protection**
- **JTAG; IEEE 1149.1 /1149.6 Test Interface**
- **MDIO; IEEE 802.3 Clause-22 Support**
- **65nm Advanced CMOS Technology**
- **Industrial Ambient Operating Temp (–40°C to 85°C) at Full Rate**
- **Device Package; 324 PBGA**

1.2 Applications

- **WI Infrastructure**
- **CPRI and OBSAI Links**
- **Proprietary Links**
- **Backplane**
- **High Speed Point- to-Point Transmission Systems**

1.3 Overview

1.3.1 Device Description

The TLK6002 is a member of a portfolio of multi-gigabit transceivers, intended for use in ultra-high-speed bi-directional point-to-point data transmission systems. It is specifically intended for base station RRH (Remote Radio Head) application, but may also be used in other high speed applications. The TLK6002 supports a serial interface speed of 0.470 Gbps to 6.25 Gbps. Rate support includes all the CPRI and OBSAI rates (0.6144/0.768/1.2288/1.536/2.4576/3.072/4.9152/6.144 Gbps) using a single fixed reference clock frequency (either 122.88 MHz or 153.6 MHz).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TLK6002 20-bit parallel interface operates in 1.5V or 1.8V HSTL single-ended format. The 20-bit interface allows low speed signals on the parallel side and therefore enabling the use of low cost FPGA in the system design. The parallel interface can be programmed to be in SDR (Single Data Rate) or DDR (Double Data Rate) modes. The line rate may be set to full (≤6.25Gbps), half (≤3.75Gbps), quarter (≤1.88Gbps) or eighth (≤0.94Gbps). The line rate can be set using either device inputs or software control registers.

The TLK6002 performs data conversion parallel-to-serial, serial-to-parallel and clock extraction as a physical layer interface device. The serial transceiver interface operates at a maximum serial data rate of 6.25 Gbps.

TLK6002 accepts single-ended HSTL signals at its parallel transmit and receive data buses. If the internal 8B/10B coding and decoding are enabled, TDA/B_[19:0] are latched by TXCLK_A/B and sent to the internal 8b/10b encoder, where the resulting encoded words are serialized and transmitted differentially using a line clock derived from the SERDES reference clock at the desired line rate. If the internal coding and decoding are disabled, TDA/B_[19:0] are defined as 20-bits of data being serialized and transmitted unmodified according to the desired line rate.

The receive direction performs the serial-to-parallel conversion on the input serial data synchronizing the resulting 20-bit parallel data to the recovered byte clock (RXCLK_A/B). The optionally decoded receive data is available on the RDA/B_[19:0] output signals.

The serial transmitter and receiver are implemented using differential Current Mode Logic (CML) with integrated termination resistors.

The TLK6002 provides two local (parallel side) and two remote (serial side) loopback modes for self-test and system diagnostic purposes.

The TLK6002 has an integrated loss of signal (LOS) detection function, which is asserted in conditions where the serial input signal does not have sufficient voltage amplitude (≤75 mV_{dfpp}). Note that the input signal must be ≥150 mV_{dfpp} when loss of signal replacement of the receive datapath data is enabled (register bit 6.6).

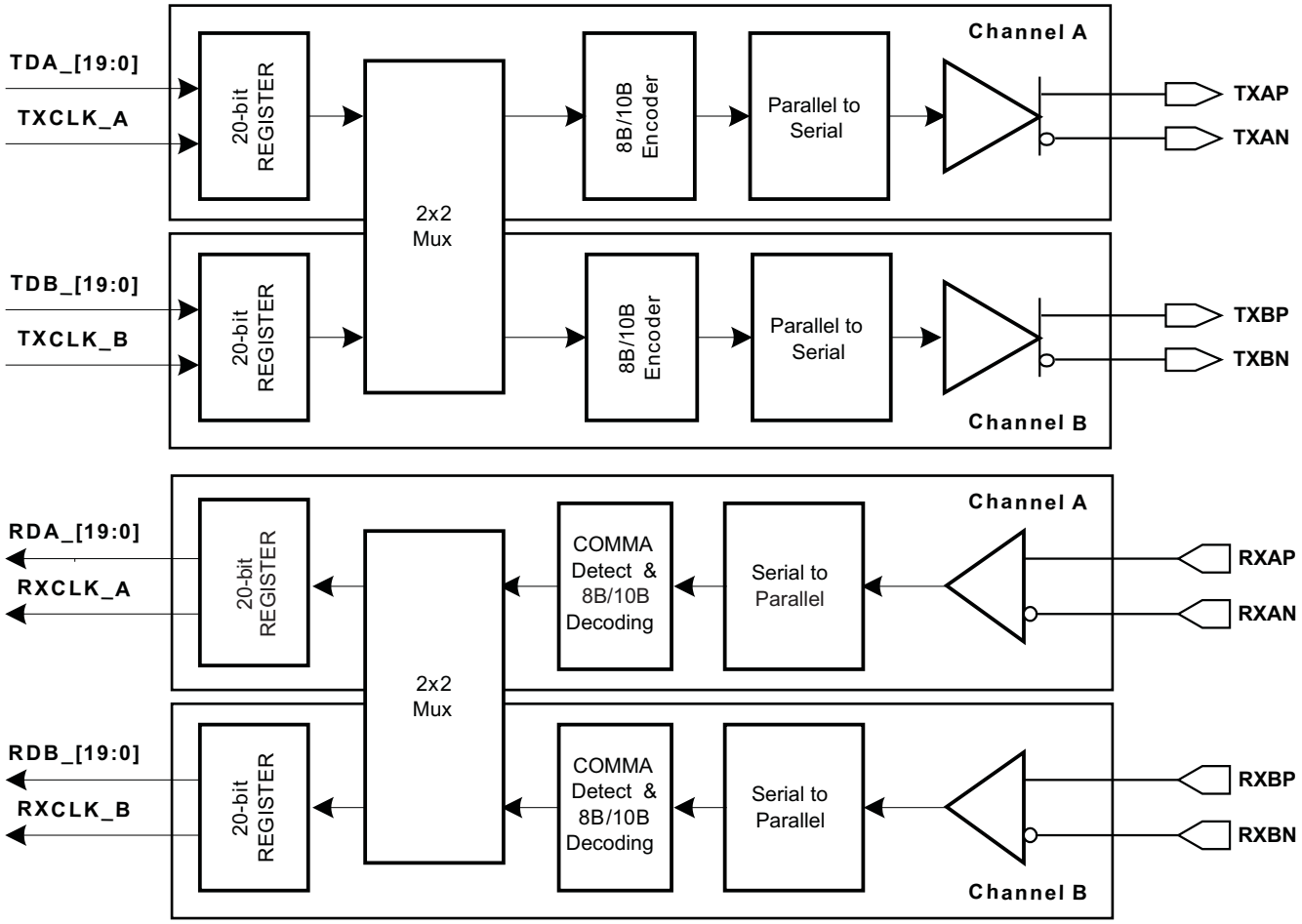


Figure 1-1. TLK6002 Block Diagram

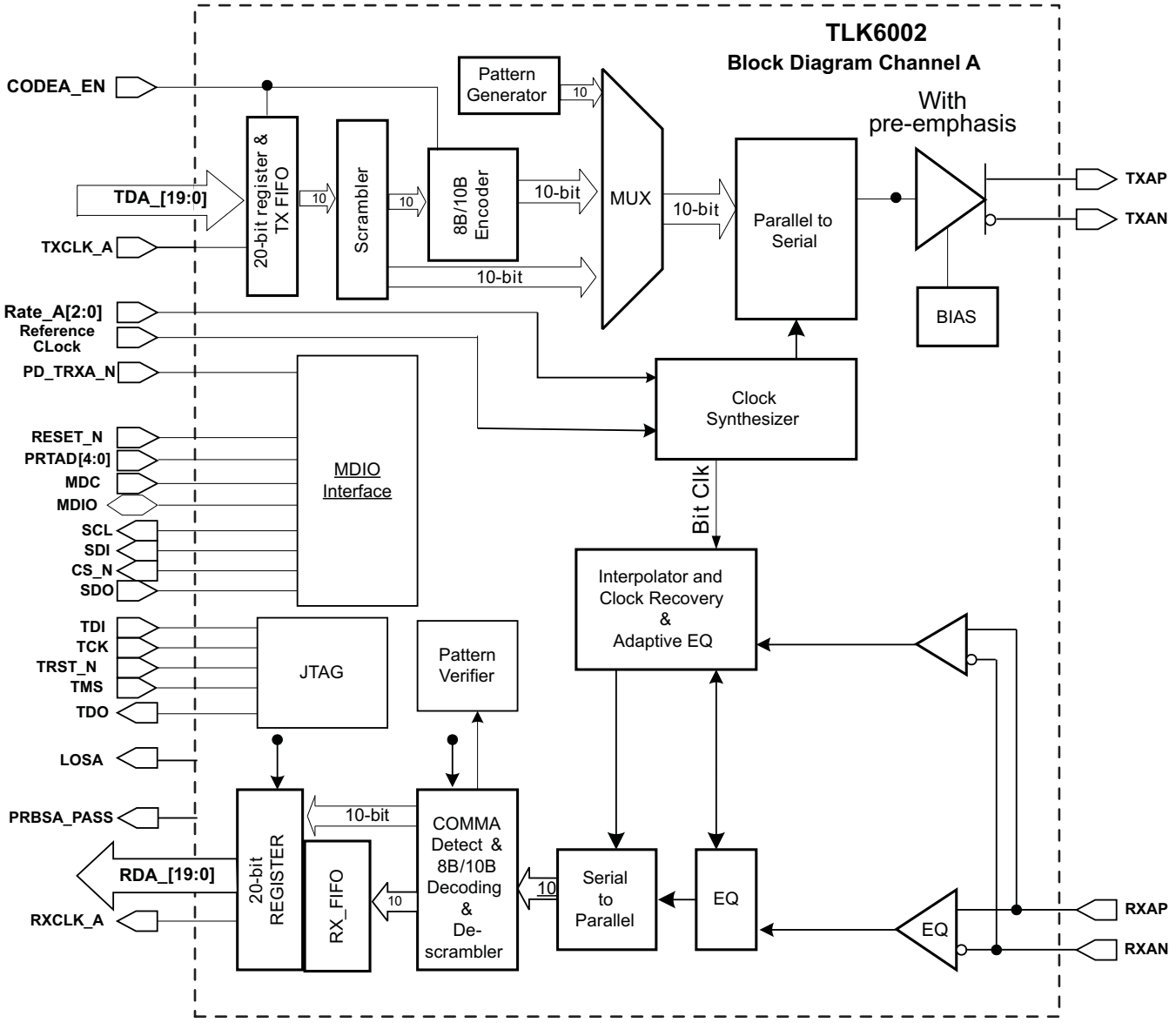


Figure 1-2. TLK6002 Detail Block Diagram (Channel A)

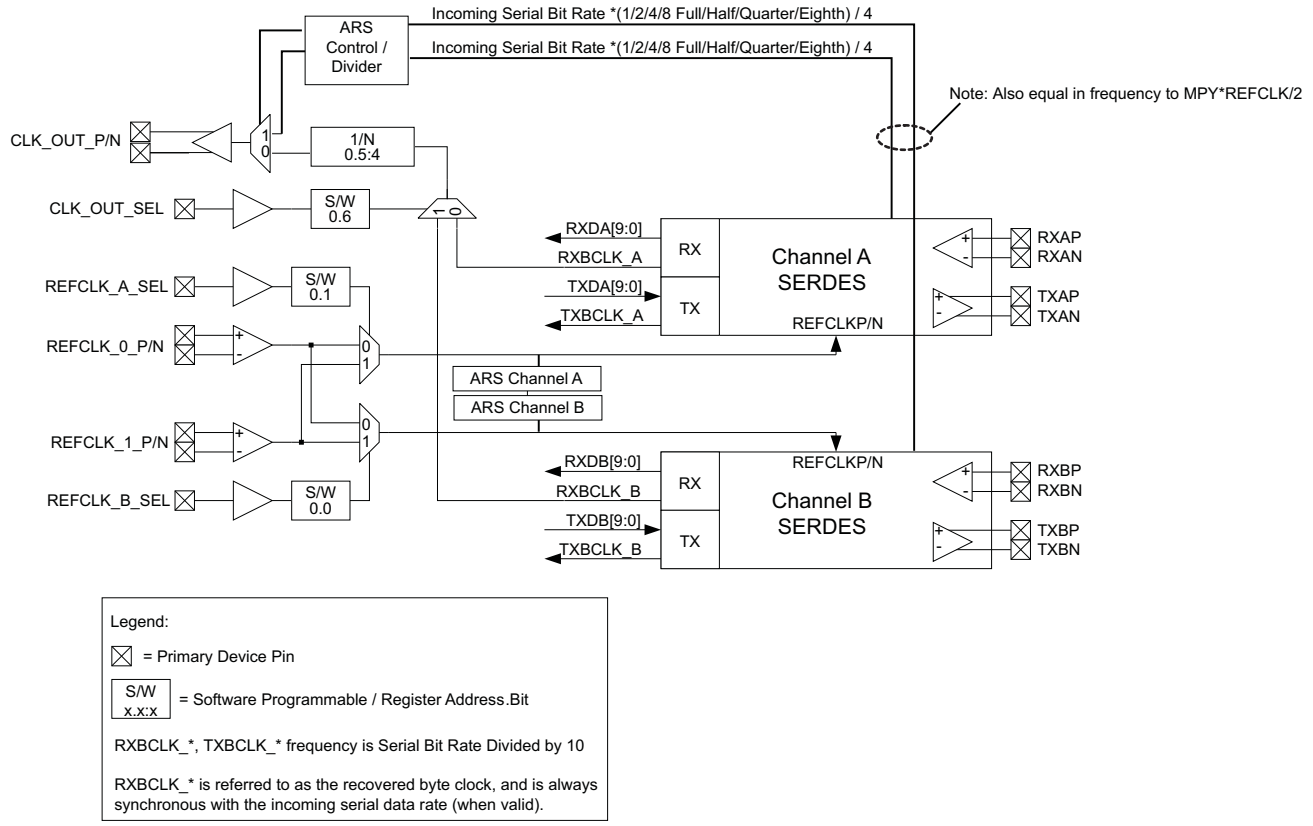


Figure 1-3. TLK6002 Reference Clock/Output Clock Architecture

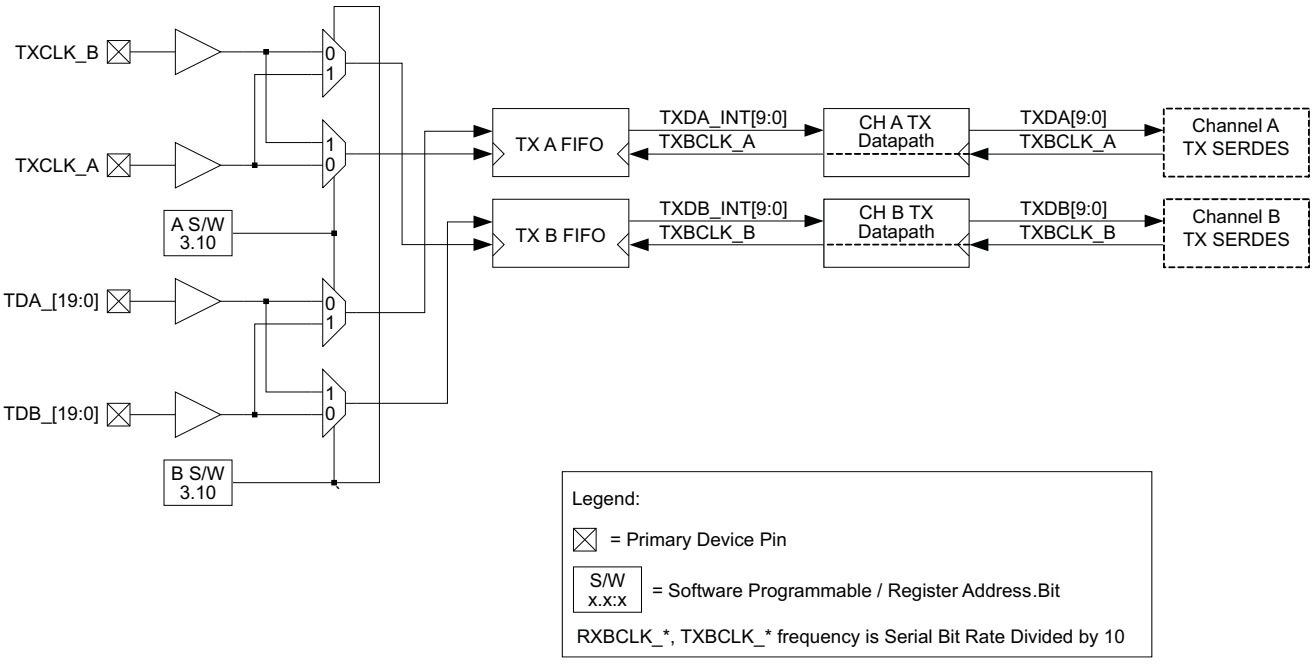


Figure 1-4. TLK6002 Transmit Clock Architecture

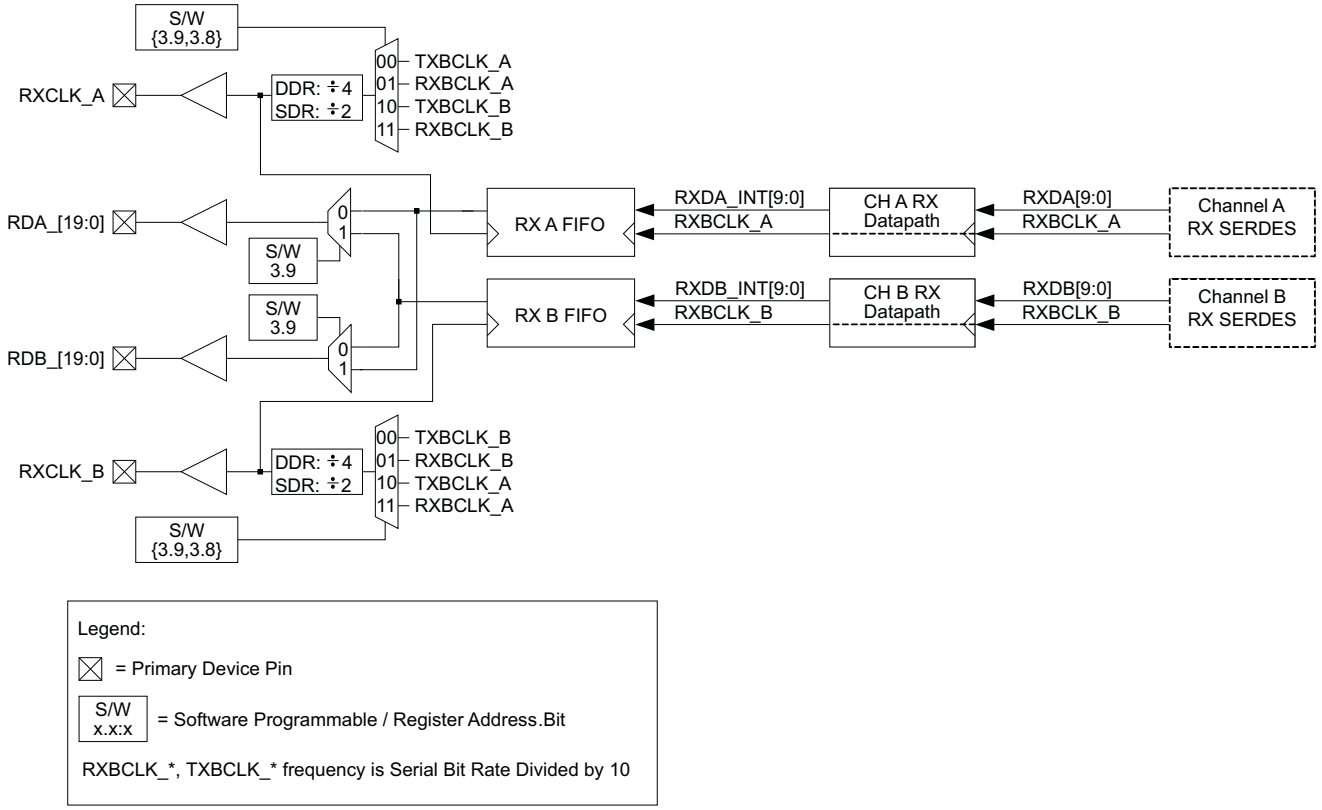


Figure 1-5. TLK6002 Receive Clock Architecture

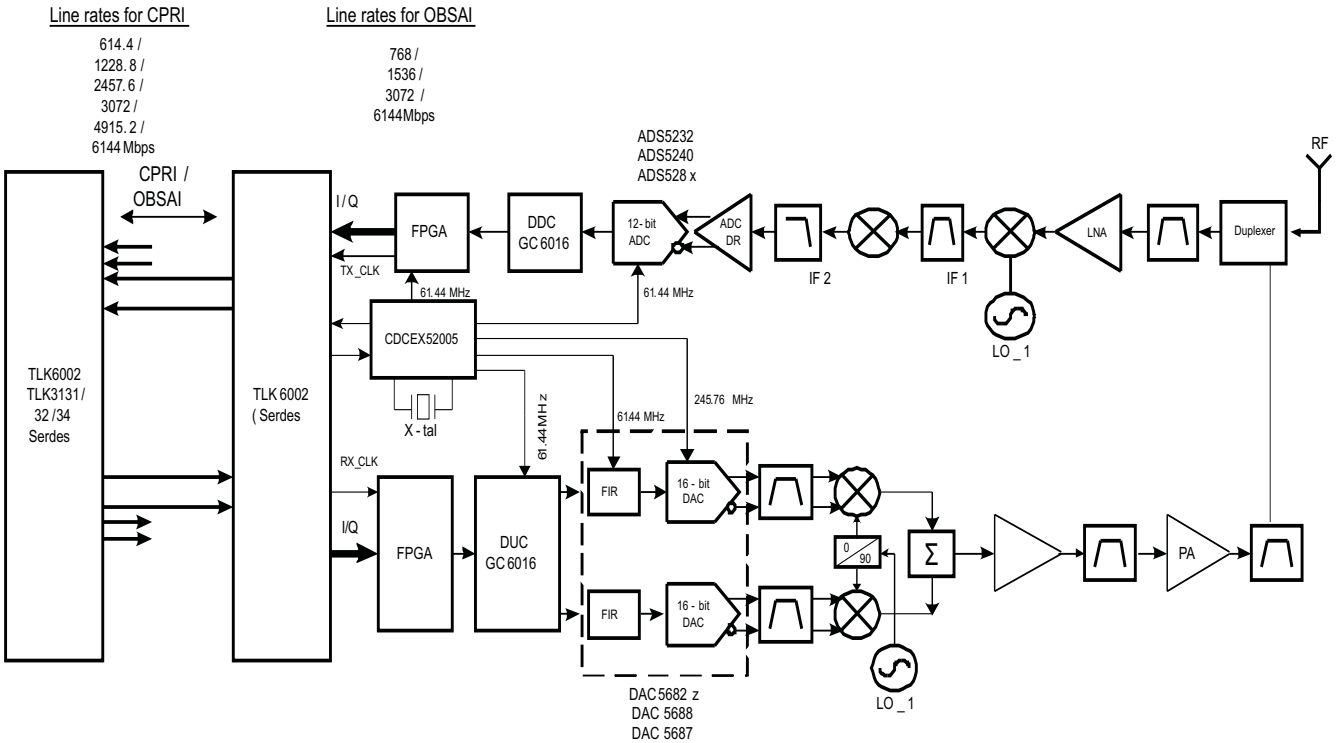


Figure 1-6. TLK6002 Application Diagram

2 Description

2.1 Pin Descriptions

Table 2-1. Pin Description – Signal Pins

Terminal		Direction Type Supply	Description
Signal	**BGA**		
Channel A:			
TXAP TXAN	V7 V6	Output CML AVDD	**Serial Transmit Channel A Output.** TXAP and TXAN comprise the transmit direction Channel A differential serial high speed output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC coupled. During pin based power down (PD_TRXA_N asserted low), these pins are floating.During register based power down (1.15 asserted high), these pins are floating.
RXAP RXAN	U9 U8	Input CML AVDD	**Serial Receive Channel A Input.** RXAP and RXAN comprise the receive direction Channel A differential high speed serial input signal. These signals must be AC coupled.
TXCLK_A	P1	Input HSTL 1.5V/1.8V VDDQA	**Transmit Input Channel A Clock.** TXCLK_A is used to sample Channel A input parallel data (TDA_[19:0]). This input must be synchronous (0 ppm) to the SERDES reference clock. In SDR mode, this signal is equal in frequency to serial bit rate / 20. In DDR mode, this signal is equal in frequency to serial bit rate / 40. If unused in the application, this input must be grounded.
TDA_[19:0]	H1 J3 H2 K4 J2 J1 K5 L3 L5 M3 M4 K3 M5 N3 M2 P2 P4 N5 R2 P5	Input HSTL 1.5V/1.8V VDDQA	**Parallel Input Channel A Transmit Data Bus.** These data signals are synchronous to and sampled by TXCLK_A. Two data modes are supported, SDR (Single Data Rate), and DDR (Double Data Rate). SDR has two valid symbols per TXCLK_A cycle, and DDR has four valid symbols per TXCLK_A cycle. When input data is in 8b/10b encoded format (a.k.a. 20-bit data mode), TDA_[19:10] and TDA_[9:0] each carry a symbol. When input data is encoded internal to TLK6002 (8b/10b encoder enabled, a.k.a. 16-bit data mode), two symbols are input at a time, defined as follows: One Symbol – TDA_[8] contains the control bit (k-character indication) of data byte TDA_[7:0], and TDA_[9] is unused and should be grounded. Other Symbol – TDA_[18] contains the control bit (k-character indication) of data byte TDA_[17:10], and TDA_[19] is unused and should be grounded. Unused parallel input pins must be grounded. See the following figures for more detail: Figure 2-1 20-bit SDR Parallel Interface Mode. Figure 2-2 16-bit SDR Parallel Interface Mode. Figure 2-3 20-bit DDR Parallel Interface Mode
RDA_[19:0]	D1 B3 B1 C2 E2 F2 F3 A2 C3 D3 C1 F4 D4 E4 G4 G3 H4 E5 H5 G5	Output HSTL 1.5V/1.8V VDDQA	**Parallel Channel A Receive Data Bus.** These output receive data signals are synchronous to RXCLK_A. Two data modes are supported, SDR (Single Data Rate), and DDR (Double Data Rate). SDR has two valid symbols per RXCLK_A cycle, and DDR has four valid symbols per RXCLK_A cycle. When output data is in 8b/10b encoded format (a.k.a. 20-bit data mode), RDA_[19:10] and RDA_[9:0] each carry a symbol. When output data is decoded internal to TLK6002 (8b/10b decoder enabled, a.k.a. 16-bit data mode), two symbols are output at a time, defined as follows: One Symbol – RDA_[8] contains the control bit (k-character indication) of data byte RDA_[7:0], and RDA_[9] indicates whether a 8b/10b disparity error was detected or an invalid code was received coincident with that particular symbol Other Symbol – RDA_[18] contains the control bit (k-character indication) of data byte RDA_[17:10], and RDA_[19] indicates whether a 8b/10b disparity error was detected or an invalid code was received coincident with that particular symbol. During device reset (RESET_N asserted low) these pins are driven low.During pin based power down (PD_TRXA_N asserted low), these pins are floating.During register based power down (1.15 asserted high), these pins are floating. See the following figures for more detail: Figure 2-1 20-bit SDR Parallel Interface Mode. Figure 2-2 16-bit SDR Parallel Interface Mode. Figure 2-3 20-bit DDR Parallel Interface Mode.

Table 2-1. Pin Description – Signal Pins (continued)

Terminal		Direction Type Supply	Description
Signal	BGA		
RATE_A[2:0]	V2 T4 U3	Input LVCMOS 1.5V/1.8V VDDO3	**Channel A Rate select pins.** These pins put channel A into one of the four supported (full/half/quarter/eighth) channel operation rates, enable software control, or enable Auto Rate Sense (ARS): **000 – Full Rate mode** **001 – Half Rate mode** **010 – Quarter rate mode** **011 – Eighth rate mode** **100 – Software Selectable Rate** (Recommended default board configuration) **101 – Channel A Auto Rate Sense (ARS) Function Enabled** Channel A SERDES settings are determined by Channel A ARS machine. CLK_OUT_P/N selected by CLK_OUT_SEL See Table 2-9 for additional details on CLK_OUT_P/N. **110 – Channel A Auto Rate Sense (ARS) Function Enabled** Channel A SERDES settings are determined by Channel A ARS machine. CLK_OUT_P/N is not selected by CLK_OUT_SEL Channel B may not be simultaneously configured with RATE_B=110 With respect to CLK_OUT_P/N, this setting has the highest priority. See Table 2-9 for additional details on CLK_OUT_P/N. **111 – Channel A Auto Rate Sense (ARS) Function Enabled – Slave Mode** *If Channel B ARS is enabled (RATE_B=101 or 110 only):* Channel A SERDES settings are determined by Channel B ARS machine. CLK_OUT_P/N is not selected by CLK_OUT_SEL See Table 2-9 for additional details on CLK_OUT_P/N. *If Channel B ARS is not enabled (RATE_B=000/001/010/011/111):* Channel A SERDES settings are determined by Channel A MDIO registers. CLK_OUT_P/N selected by CLK_OUT_SEL See Table 2-9 for additional details on CLK_OUT_P/N. Channel A and B should not be in slave mode simultaneously. Both directions of Channel A are controlled by these input signals. The RATE_A[2] pin should be routed to an uninstalled header so that it could be driven externally in the event that device debug is required. In application mode, it should be biased with a pull up or pull down resistor, and not connected directly to a power or ground plane.
RXCLK_A	F1	Output HSTL 1.5V/1.8V VDDQA	**Receive Output Channel A Clock.** RXCLK_A is synchronous to RDA_[19:0], and may be used externally to sample Channel A output parallel data. In SDR mode, this signal is equal in frequency to serial bit rate / 20. In DDR mode, this signal is equal in frequency to serial bit rate / 40. During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PD_TRXA_N asserted low), this pin is floating. During register based power down (1.15 asserted high), these pins are floating.
PRBSA_PASS	V3	Output LVCMOS 1.5V/1.8V VDDO3 40Ω Driver	**Receive PRBS Channel A Error Free (Pass) Indicator** When PRBS test is enabled (PRBS_EN=1): PRBSA_PASS=1 indicates that PRBS pattern reception is error free. PRBSA_PASS=0 indicates that a PRBS error is detected. During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PD_TRXA_N asserted low), this pin is floating. During register based power down (1.15 asserted high), this pin is floating. It is highly recommended that PRBSA_PASS be brought to easily accessible point on the application board (header), in the event that debug is required.
CODEA_EN	V4	Input LVCMOS 1.5V/1.8V VDDO3	**Encoder/Decoder Channel A Enable:** When this pin is asserted high, the internal 8b/10b encoder/decoder is enabled. This signal is OR'd with MDIO register bits, and should be pulled low through a resistor if software control is desired. This pin should be routed to an uninstalled header so that it could be driven externally in the event that device debug is required. In application mode, it should be biased with a pull up or pull down resistor, and not connected directly to a power or ground plane.
LOSA	U4	Output LVCMOS 1.5V/1.8V VDDO3 40Ω Driver	**Channel A Receive Loss Of Signal (LOS) Indicator.** LOSA = 0, signal detected. LOSA = 1, Loss of signal (6.10 enabled). Loss of signal detection is based on the input signal level. When RXAP/N has an input signal of ≤75 mVdfpp, LOSA will be asserted (if enabled). The input signal should be ≥ 150 mVdfpp for this function to operate reliably. Other functions can be observed on LOSA realtime, configured via MDIO. During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PD_TRXA_N asserted low), this pin is floating. During register based power down (1.15 asserted high), this pin is floating. It is highly recommended that LOSA be brought to easily accessible point on the application board (header), in the event that debug is required.

Table 2-1. Pin Description – Signal Pins (continued)

Terminal		Direction Type Supply	Description
Signal	**BGA**		
PD_TRXA_N	T6	Input LVCMOS 1.5V/1.8V VDDO3	**Transceiver Power down.** When this pin is held low (asserted), Channel A is placed in power down mode. When deasserted , Channel A operates normally. After deassertion, a software datapath reset should be issued through the MDIO interface.
Channel B:			
TXBP TXBN	U12 U13	Output CML AVDD	**Serial Transmit Channel B Output.** TXBP and TXBN comprise the transmit direction Channel B differential high speed serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC coupled. During pin based power down (PD_TRXB_N asserted low), these pins are floating. During register based power down (1.15 asserted high), these pins are floating.
RXBP RXBN	V10 V11	Input CML AVDD	**Serial Receive Channel B Input.** RXBP and RXBN comprise the receive direction Channel B differential high speed serial input signal. These signals must be AC coupled.
RATE_B[2:0]	U16 U17 U18	Input LVCMOS 1.5V/1.8V VDDO2	**Channel B Rate select pins.** These pins put channel B into one of the four supported (full/half/quarter/eighth) channel operation rates, enable software control, or enable Auto Rate Sense (ARS): **000 – Full Rate mode** **001 – Half Rate mode** **010 – Quarter rate mode** **011 – Eighth rate mode** **100 – Software Selectable Rate** (Recommended if ARS not used) **101 – Channel B Auto Rate Sense (ARS) Function Enabled** Channel B SERDES settings are determined by Channel B ARS machine. CLK_OUT_P/N selected by CLK_OUT_SEL See Table 2-9 for additional details on CLK_OUT_P/N. **110 – Channel B Auto Rate Sense (ARS) Function Enabled** Channel B SERDES settings are determined by Channel B ARS machine. CLK_OUT_P/N is not selected by CLK_OUT_SEL Channel A may not be simultaneously configured with RATE_A=110 With respect to CLK_OUT_P/N, this setting has the highest priority. See Table 2-9 for additional details on CLK_OUT_P/N. **111 – Channel B Auto Rate Sense (ARS) Function Enabled – Slave Mode** *If Channel A ARS is enabled (RATE_A=101 or 110 only):* Channel B SERDES settings are determined by Channel A ARS machine. CLK_OUT_P/N is not selected by CLK_OUT_SEL See Table 2-9 for additional details on CLK_OUT_P/N. *If Channel A ARS is not enabled (RATE_A=000/001/010/011/111):* Channel B SERDES settings are determined by Channel B MDIO registers. CLK_OUT_P/N selected by CLK_OUT_SEL See Table 2-9 for additional details on CLK_OUT_P/N. Channel A and B should not be in slave mode simultaneously. Both directions of Channel B are controlled by these input signals. The RATE_B[2] pin should be routed to an uninstalled header so that it could be driven externally in the event that device debug is required. In application mode, it should be biased with a pull up or pull down resistor, and not connected directly to a power or ground plane.
TXCLK_B	T18	Input HSTL 1.5V/1.8V VDDQB	**Transmit Input Channel B Clock.** TXCLK_B is used to sample Channel B input parallel data (TDB_[19:0]). This input must be synchronous (0 ppm) to the SERDES reference clock. In SDR mode, this signal is equal in frequency to serial bit rate / 20. In DDR mode, this signal is equal in frequency to serial bit rate / 40. If unused in the application, this input must be grounded.

Table 2-1. Pin Description – Signal Pins (continued)

Terminal		Direction Type Supply	Description
Signal	BGA		
TDB_[19:0]	J17 H17 J16 H18 K15 K16 L14 L16 M14 M16 M15 P17 N14 N16 J18 M17 R17 P15 P14 P18	Input HSTL 1.5V/1.8V VDDQB	**Parallel Input Channel B Transmit Data Bus.** These data signals are synchronous to and sampled by TXCLK_B. Two data modes are supported, SDR (Single Data Rate), and DDR (Double Data Rate). SDR has two valid symbols per TXCLK_B cycle, and DDR has four valid symbols per TXCLK_B cycle. When input data is in 8b/10b encoded format (a.k.a. 20-bit data mode), TDB_[19:10] and TDB_[9:0] each carry a symbol. When input data is encoded internal to TLK6002 (8b/10b encoder enabled, a.k.a. 16-bit data mode), two symbols are input at a time, defined as follows: One Symbol – TDB_[8] contains the control bit (k-character indication) of data byte TDB_[7:0], and TDB_[9] is unused and should be grounded. Other Symbol – TDB_[18] contains the control bit (k-character indication) of data byte TDB_[17:10], and TDB_[19] is unused and should be grounded. Unused parallel input pins must be grounded. See the following figures for more detail: Figure 2-1 20-bit SDR Parallel Interface Mode Figure 2-2 16-bit SDR Parallel Interface Mode Figure 2-3 20-bit DDR Parallel Interface Mode
RDB_[19:0]	D18 E17 B18 C17 F16 F17 A17 B16 C16 D16 C18 F15 A16 B15 D15 E15 G16 H15 G15 G14	Output HSTL 1.5V/1.8V VDDQB	**Parallel Channel B Receive Data Bus.**These output receive data signals are synchronous to RXCLK_B. Two data modes are supported, SDR (Single Data Rate), and DDR (Double Data Rate). SDR has two valid symbols per RXCLK_B cycle, and DDR has four valid symbols per RXCLK_B cycle. When output data is in 8b/10b encoded format (a.k.a. 20-bit data mode), RDB_[19:10] and RDB_[9:0] each carry a symbol. When output data is decoded internal to TLK6002 (8b/10b decoder enabled, a.k.a. 16-bit data mode), two symbols are output at a time, defined as follows: One Symbol - RDB_[8] contains the control bit (k-character indication) of data byte RDB_[7:0], and RDB_[9] indicates whether a 8b/10b disparity error was detected or an invalid code was received coincident with that particular symbol Other Symbol - RDB_[18] contains the control bit (k-character indication) of data byte RDB_[17:10], and RDB_[19] indicates whether a 8b/10b disparity error was detected or an invalid code was received coincident with that particular symbol. During device reset (RESET_N asserted low) these pins are driven low. During pin based power down (PD_TRXB_N asserted low), these pins are floating. During register based power down (1.15 asserted high), these pins are floating. See the following figures for more detail: Figure 2-1 20-bit SDR Parallel Interface Mode Figure 2-2 16-bit SDR Parallel Interface Mode Figure 2-3 20-bit DDR Parallel Interface Mode
RXCLK_B	F18	Output HSTL 1.5V/1.8V VDDQB	**Receive Output Channel B Clock.** RXCLK_B is synchronous to RDB_[19:0], and may be used externally to sample Channel B output parallel data. In SDR mode, this signal is equal in frequency to serial bit rate / 20. In DDR mode, this signal is equal in frequency to serial bit rate / 40. During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PD_TRXB_N asserted low), this pin is floating. During register based power down (1.15 asserted high), these pins are floating.
PRBSB_PASS	V18	Output LVCMOS 1.5V/1.8V VDDO2 40Ω Driver	**Receive PRBS Channel B Error Free (Pass) Indicator** When PRBS test is enabled (PRBS_EN=1): PRBSB_PASS=1 indicates that PRBS pattern reception is error free. PRBSB_PASS=0 indicates that a PRBS error is detected. During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PD_TRXB_N asserted low), this pin is floating. During register based power down (1.15 asserted high), this pin is floating. It is highly recommended that PRBSB_PASS be brought to easily accessible point on the application board (header), in the event that debug is required.
CODEB_EN	V16	Input LVCMOS 1.5V/1.8V VDDO2	**Encoder/Decoder Channel B Enable:** When this pin is asserted high, the internal 8b/10b encoder/decoder is enabled. This signal is OR'd with MDIO register bits, and should be tied low if software control is desired.

Table 2-1. Pin Description – Signal Pins (continued)

Terminal		Direction Type Supply	Description
Signal	**BGA**		
LOSB	V17	Output LVCMOS 1.5V/1.8V VDDO2 40Ω Driver	**Channel B Receive Loss Of Signal (LOS) Indicator.** LOSB=0, signal detected. LOSB=1, Loss of signal (6.10 enabled). Loss of signal detection is based on the input signal level. When RXBP/N has an input signal of ≤75 mVdfpp, LOSB will be asserted (if enabled). The input signal should be ≥ 150 mVdfpp for this function to operate reliably. Other functions can be observed on LOSB realtime, configured via MDIO. During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PD_TRXB_N asserted low), this pin is floating. During register based power down (1.15 asserted high), this pin is floating. It is highly recommended that LOSB be brought to easily accessible point on the application board (header), in the event that debug is required.
PD_TRXB_N	U15	Input LVCMOS 1.5V/1.8V VDDO2	**Transceiver Power down.** When this pin is held low (asserted), Channel B is placed in power down mode. When deasserted , Channel B operates normally. After deassertion, a software datapath reset should be issued through the MDIO interface.
Signals common to Channels A and B:			
REFCLK_0_P/N	B5 A5	Input LVDS/ LVPECL DVDD	**Reference Clock Input Zero.** This differential input is a clock signal used as a reference to either or both of the bidirectional SERDES macros. It can be routed internally to either SERDES macro using device pins (REFCLK_A_SEL and REFCLK_B_SEL) or through software registers. This input signal must be AC coupled. See Figure 1-3. TLK6002 Reference Clock / Output Clock Architecture for more detail. If unused, REFCLK_0_P/N should be pulled down to DGND through a shared 100Ω resistor.
REFCLK_1_P/N	C6 D6	Input LVDS/ LVPECL DVDD	**Reference Clock Input One.** This differential input is a clock signal used as a reference to either or both of the bidirectional SERDES macros. It can be routed internally to either SERDES macro using device pins (REFCLK_A_SEL and REFCLK_B_SEL) or through software registers. This input signal must be AC coupled. See Figure 1-3. TLK6002 Reference Clock / Output Clock Architecture for more detail. If unused, REFCLK_1_P/N should be pulled down to DGND through a shared 100Ω resistor
REFCLK_A_SEL	R6	Input LVCMOS 1.5V/1.8V VDDO3	**Reference Clock Select Channel A.** This input, when low, selects REFCLK_0_P/N as the clock reference to Channel A SERDES macro. When high, REFCLK_1_P/N is selected as the clock reference to Channel A SERDES macro. If software control is desired (register bit 0.1), this input signal should be tied low. See Figure 1-3. TLK6002 Reference Clock / Output Clock Architecture for more detail.
REFCLK_B_SEL	T2	Input LVCMOS 1.5V/1.8V VDDO3	**Reference Clock Select Channel B.** This input, when low, selects REFCLK_0_P/N as the clock reference to Channel B SERDES macro. When high, REFCLK_1_P/N is selected as the clock reference to Channel B SERDES macro. If software control is desired (register bit 0.0), this input signal should be tied low. See Figure 1-3. TLK6002 Reference Clock/Output Clock Architecture for more detail.
PRBS_EN	R16	Input LVCMOS 1.5V/1.8V VDDO2	**Enable PRBS:** When this pin is asserted high, the internal PRBS generator and verifier circuits are enabled on both transmit and receive data paths of both channels. This signal is logically OR'd with an mdio register bit. PRBS 2^{31}-1 is selected by default, and can be changed in MDIO register 7.10:8. **Note that PRBS is not possible in eighth rate mode.** The PRBS_EN pin should be routed to an uninstalled header so that it could be driven externally in the event that device debug is required. In application mode, it should be biased with a pull up or pull down resistor (or allow for an isolation mechanism from the on board driver), and not connected directly to a power or ground plane.
CLK_OUT_P/N	J6 J7	Output CML DVDD	**Recovered Byte Clock.** If ARS is not enabled, and CLK_OUT_SEL is low, an optionally divided version of Channel A recovered byte clock is output onto CLK_OUT_P/N. If ARS is not enabled, and CLK_OUT_SEL is high, an optionally divided version of Channel B recovered byte clock is output onto CLK_OUT_P/N. The recovered byte clock is synchronous to the incoming serial data rate for the selected channel. See Figure 1-3. TLK6002 Reference Clock/Output Clock Architecture for more detail. The recovered byte clock can be divided by one, two, four, or eight as selected in an mdio register. If ARS is enabled, the CLK_OUT_P/N output is selected via **Table 2-9.** This CML output must be AC coupled. During device reset (RESET_N asserted low) this pin is driven differential zero. During pin based power down (PD_TRXA_N and PD_TRXB_N asserted low), these pins are floating. During register based power down (1.15 asserted high both channels), these pins are floating.
CLK_OUT_SEL	T15	Input LVCMOS 1.5V/1.8V VDDO2	**Output Clock Selection.** If ARS is not enabled and CLK_OUT_SEL is low, Channel A recovered byte clock is output onto CLK_OUT_P/N. If ARS is not enabled and CLK_OUT_SEL is high, Channel B recovered byte clock is output onto CLK_OUT_P/N. If software control is desired (register bit 0.6), this input signal should be tied low. See Figure 1-3. TLK6002 Reference Clock / Output Clock Architecture for more detail. If ARS is enabled, the function of CLK_OUT_SEL is shown in **Table 2-9.**

Table 2-1. Pin Description – Signal Pins (continued)

Terminal		Direction Type Supply	Description
Signal	BGA		
PRTAD[4:0]	V15 M8 K12 K11 L11	Input LVCMOS 1.5V/1.8V VDDO2/ VDDO1/ VDDO1/ VDDO1/ VDDO1	**Port Address.** Used to select the Port ID. PRTAD[4:1] selects the device port address. TLK6002 has two different PHY addresses (ports). Selecting a unique PRTAD[4:1] per TLK6002 device allows 16 TLK6002 devices per MDIO bus. Each channel can be accessed by setting the appropriate port address field within the serial interface protocol transaction. TLK6002 will respond if the 4 MSB's of the inband PHY address field on MDIO protocol (PA[4:1]) matches PRTAD[4:1]. The LSB of PHY address field (PA[0]) will determine which channel/port within TLK6002 to respond to. PRTAD[0] is not used functionally, but is present for device testability and compatibility with other devices in the family of products. Channel A responds to port address 0 within the block of two port addresses. Channel B responds to port address 1 within the block of two port addresses. PRTAD[0] should be grounded on the application board. The PRTAD[3] pin in application mode should be biased with a pull up or pull down resistor (or allow for an isolation mechanism from the on board driver), and not connected directly to a power or ground plane. The application board should allow the flexibility of easily reworking the PRTAD[3] signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO1).
RESET_N	V1	Input LVCMOS 1.5V/1.8V VDDO3	**Low True Device Reset.** When asserted (low logic level), this signal resets the entire TLK6002 device. RESET_N must be held asserted for at least 10 µS after device power stabilization.
MDC	T1	Input LVCMOS w/Hysteresi s 1.5V/1.8V VDDO3	**MDIO clock input.** Clock input for the Clause 22 MDIO interface. Note that an external pullup is generally not required on MDC.
MDIO	U2	Input/ Output LVCMOS 1.5V/1.8V VDDO3 25Ω Driver	**MDIO data I/O.** MDIO interface data input/output signal for the Clause 22 MDIO interface. **This signal must be externally pulled up to VDDO3, using a 2 kΩ resistor.** During device reset (RESET_N asserted low) this pin is floating. During software initiated power down the management interface remains active for control register writes and reads. Certain status bits are not deterministic as their generating clock source may be disabled as a result of asserting either power down input signal. During pin based power down (PD_TRXA_N and PD_TRXB_N asserted low), this pin is floating. During register based power down (1.15 asserted high both channels), this pin is driven normally.
SCL	H13	Input/ Output LVCMOS 1.5V/1.8V VDDO1 25Ω Driver	**SPI Clock (SPI_CLK).** Defaults to Output, Driven Low. Can be used as a SPI interface or a generic customer controllable I/O interface. When used as part of the SPI interface, this signal is the SPI clock to be used with external TI Jitter cleaner or clock Distribution device. Three register bits (15.14:12) control this I/O signal. See the detailed register bit description for operational detail. If unused in the application, this signal can be left floating. Careful programming is required to prevent accidental contention with simultaneous external drivers. During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PD_TRXA_N and PD_TRXB_N asserted low), this pin is floating. During register based power down (1.15 asserted high both channels), these pins are driven per register setting
SDO	K13	Input/ Output LVCMOS 1.5V/1.8V VDDO1 25Ω Driver	**SPI Data. Defaults to Input.** Can be used as a SPI interface or a generic customer controllable I/O interface. When used as part of the SPI interface, this signal is the SPI data from the external TI Jitter cleaner or clock Distribution device to the TLK6002. Three register bits (15.10:8) control this I/O signal. See the detailed register bit description for operational detail. If unused in the application, this signal should be pulled to ground. Careful programming is required to prevent accidental contention with simultaneous external drivers. During device reset (RESET_N asserted low) this pin is floating. During pin based power down (PD_TRXA_N and PD_TRXB_N asserted low), this pin is floating. During register based power down (1.15 asserted high both channels), these pins are driven per register setting.
SDI	E14	Input/ Output LVCMOS 1.5V/1.8V VDDO1 25Ω Driver	**SPI Data. Defaults to Output, driven low.** Can be used as a SPI interface or a generic customer controllable I/O interface. When used as part of the SPI interface, this signal is the SPI data from TLK6002 to the external TI Jitter cleaner or clock Distribution device. Three register bits (15.6:4) control this I/O signal. See the detailed register bit description for operational detail. If unused in the application, this signal can be left floating. Careful programming is required to prevent accidental contention with simultaneous external drivers. During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PD_TRXA_N and PD_TRXB_N asserted low), this pin is floating. During register based power down (1.15 asserted high both channels), these pins are driven per register setting.
CS_N	D14	Input/ Output LVCMOS 1.5V/1.8V VDDO1 25Ω Driver	**SPI Chip Select. Defaults to Output, Driven High.** Can be used as a SPI interface or a generic customer controllable I/O interface. When used as part of the SPI interface, this signal is the chip select for the external TI Jitter cleaner or clock Distribution device. Low=Select Device. High=Device Not Selected. Three register bits (15.2:0) control this I/O signal. See the detailed register bit description for operational detail. If unused in the application, this signal can be left floating. Careful programming is required to prevent accidental contention with simultaneous external drivers. During device reset (RESET_N asserted low) this pin is driven high. During pin based power down (PD_TRXA_N and PD_TRXB_N asserted low), this pin is floating. During register based power down (1.15 asserted high both channels), these pins are driven per register setting.

Table 2-1. Pin Description – Signal Pins (continued)

Terminal		Direction Type Supply	Description
Signal	BGA		
TDI	R15	Input LVCMOS 1.5V/1.8V VDDO2 (Internal Pullup)	**JTAG Input Data.** TDI is used to serially shift test data and test instructions into the device during the operation of the test port. In system applications where JTAG is not implemented, this input signal may be left floating. During pin based power down (PD_TRXA_N and PD_TRXB_N asserted low), this pin is not pulled up. During register based power down (1.15 asserted high both channels), this pin is pulled up normally.
TDO	R14	Output LVCMOS 1.5V/1.8V VDDO2 50Ω Driver	**JTAG Output Data.** TDO is used to serially shift test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high impedance state. During device reset (RESET_N asserted low) this pin is floating. During pin based power down (PD_TRXA_N and PD_TRXB_N asserted low), this pin is floating. During register based power down (1.15 asserted high both channels), this pin is floating.
TMS	R3	Input LVCMOS 1.5V/1.8V VDDO3 (Internal Pullup)	**JTAG Mode Select.** TMS is used to control the state of the internal test-port controller. In system applications where JTAG is not implemented, this input signal can be left unconnected. During pin based power down (PD_TRXA_N **and** PD_TRXB_N asserted low), this pin is not pulled up. During register based power down (1.15 asserted high both channels), this pin is pulled up normally.
TCK	T16	Input LVCMOS w/Hysteresis 1.5V/1.8V VDDO2	**JTAG Clock.** TCK is used to clock state information and test data into and out of the device during boundary scan operation. In system applications where JTAG is not implemented, this input signal should be grounded.
TRST_N	T3	Input LVCMOS 1.5V/1.8V VDDO3 (Internal Pulldown)	**JTAG Test Reset.** TRST_N is used to reset the JTAG logic into system operational mode. This input can be left unconnected in the application and is pulled down internally, disabling the JTAG circuitry. If JTAG is implemented on the application board, this signal should be deasserted (high) during JTAG system testing, and otherwise asserted (low) during normal operation mode. During pin based power down (PD_TRXA_N and PD_TRXB_N asserted low), this pin is not pulled down. During register based power down (1.15 asserted high both channels), this pin is pulled down normally.
TESTEN	T17	Input LVCMOS 1.5V/1.8V VDDO2	**Test Enable.** This signal is used during the device manufacturing process. It should be grounded through a resistor in the device application board. The application board should allow the flexibility of easily reworking this signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO2).
GPI0	R4	Input LVCMOS 1.5V/1.8V VDDO3	**General Purpose Input Zero.** This signal is used during the device manufacturing process. It should be grounded through a resistor on the device application board. The application board should also allow the flexibility of easily reworking this signal to a high level if device debug is necessary (by including an uninstalled resistor to VDDO3).
GPI1	K10	Input LVCMOS 1.5V/1.8V VDDO1	**General Purpose Input One.** This signal can be used to logically combine an external status condition with LOSA or LOSB if enabled in an mdio register. Note that if GPI1 is low, LOSA/B will be asserted if logical combination is enabled. Similarly, if GPI1 is high, LOSA/B will be deasserted. If unused, this input should be grounded in the device application (not floating).
AMUXA	U5	Analog I/O	**SERDES Channel A Analog Testability I/O.** This signal is used during the device manufacturing process. It should be left unconnected in the device application.
AMUXB	V14	Analog I/O	**SERDES Channel B Analog Testability I/O.** This signal is used during the device manufacturing process. It should be left unconnected in the device application.
RESRA, RESTA, RESRB, RESTB	K8 M1 J14 M18	Analog Input	**HSTL Impedance Matching Resistors.** These resistors are used as a reference for internal terminations on the HSTL inputs and outputs. Each RES* pin requires it's own resistor, sharing resistors between RES* pins is not possible. A 50 ohm 0.5% tolerance resistor should be selected to guarantee device datasheet specified parallel interface timing specification.

Table 2-2. Pin Description – Power Pins

Terminal		Type	Description
Signal	BGA		
VDDD	T8 T11	Power	**SERDES Digital logic power** Provides power for digital circuitry internal to the SERDES. 1.0V nominal.
AVDD	U6 T9 T10 U11 T13 U14	Power	**SERDES Analog Power** AVDD provides supply voltage for the high-speed analog circuits. 1.0V nominal.
DVDD	L6 L9 L13 M10 M12 N6 N13 R8 R10 R12 T5	Power	**Digital Core Power** DVDD provides supply voltage to the digital core. 1.0V nominal.
VDDT	V8 V12	Power	**SERDES Analog Power** VDDT provides supply voltage for the high-speed analog circuits, termination voltage. 1.0V nominal.
VDDRA/B	T7 T12	Power	**SERDES Analog Regulator Power** VDDRA and VDDRB provide supply voltage for the internal PLL regulator. 1.5V or 1.8V nominal.
VDDQA/B	A3 B2 B17 C4 C15 E1 E18 F5 F14 G2 G17 J4 J15 K1 K18 L4 L7 L8 L12 L15 L17 M6 M13 N1 N18 P3 P6 P13 P16	Power	**HSTL I/O Power** VDDQA and VDDQB provide supply voltage for the HSTL inputs and outputs. 1.5V or 1.8V nominal.
VDDO1/2/3	L10 R13 R7	Power	**LVCMOS I/O Power** VDDO1, VDDO2, and VDDO3 provide supply voltage for the LVCMOS inputs and outputs. 1.5V or 1.8V nominal.
VPP	K9	Power	**Factory Program Voltage** Programming supply voltage for TI internal use during device manufacturing. The application must connect this power supply directly to DVDD.
AGND	R9 R11 T14 U7 U10 V5 V9 V13	Ground	**Analog Ground** Analog ground.

Table 2-2. Pin Description – Power Pins (continued)

Terminal		Type	Description
Signal	BGA		
DGND	A1 A4 A6 A15 A18 B4 B6 C5 D2 D5 D17 E3 E16 G1 G18 H3 H14 H16 J5 K2 K6 K14 K17 L2 M7 M9 M11 N2 N4 N7 N8 N10 N11 N12 N15 N17 P7 P8 P9 P10 P11 P12 R1 R5 R18 U1	Ground	**Digital Ground** Digital ground
VREFTA, VREFTB	L1 L18	Voltage Reference	**HSTL Voltage Reference** These high impedance voltage reference inputs are used as a signal comparison level for HSTL input signals. These signals should be created using a resistive voltage divider (dual 1kΩ) between VDDQA or VDDQB and DGND. These signals should be locally decoupled as close to the device pins as possible.

Table 2-2. Pin Description – Power Pins (continued)

Terminal		Type	Description
Signal	BGA		
NC	A7 A8 A9 A10 A11 A12 A13 A14 B7 B8 B9 B10 B11 B12 B13 B14 C7 C8 C9 C10 C11 C12 C13 C14 D7 D8 D9 D10 D11 D12 D13 E6 E7 E8 E9 E10 E11 E12 E13 F6 F7 F8 F9 F10 F11 F12 F13 G6 G7 G8 G9 G10 G11 G12 G13 H6 H7 H8 H9 H10 H11 H12 J8 J9 J10 J11 J12 J13 K7	No Connect	**No Connect** These BGAs can be left unconnected in the application
NC33	N9	Reserved Input	**Reserved** This input pin should be connected to DVDD through a zero ohm resistor in the device application.

2.2 Device Pinout Diagram

Table 2-3. Device Pinout Diagram – (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DGND	RDA_12	VDDQA	DGND	REFCLK_0_N	DGND									DGND	RDB_7	RDB_13	DGND
B	RDA_17	VDDQA	RDA_18	DGND	REFCLK_0_P	DGND									RDB_6	RDB_12	VDDQB	RDB_17
C	RDA_9	RDA_16	RDA_11	VDDQA	DGND	REFCLK_1_P									VDDQB	RDB_11	RDB_16	RDB_9
D	RDA_19	DGND	RDA_10	RDA_7	DGND	REFCLK_1_N								CS_N	RDB_5	RDB_10	DGND	RDB_19
E	VDDQA	RDA_15	DGND	RDA_6	RDA_2									SDI	RDB_4	DGND	RDB_18	VDDQB
F	RXCLK_A	RDA_14	RDA_13	RDA_8	VDDQA									VDDQB	RDB_8	RDB_15	RDB_14	RXCLK_B
G	DGND	VDDQA	RDA_4	RDA_5	RDA_0									RDB_0	RDB_1	RDB_3	VDDQB	DGND
H	TDA_19	TDA_17	DGND	RDA_3	RDA_1								SCL	DGND	RDB_2	DGND	TDB_18	TDB_16
J	TDA_14	TDA_15	TDA_18	VDDQA	DGND	CLK_OUT_P	CLK_OUT_N							RESRB	VDDQB	TDB_17	TDB_19	TDB_5
K	VDDQA	DGND	TDA_8	TDA_16	TDA_13	DGND		RESRA	VPP	GPI1	PRTAD1	PRTAD2	SDO	DGND	TDB_15	TDB_14	DGND	VDDQB
L	VREFTA	DGND	TDA_12	VDDQA	TDA_11	DVDD	VDDQA	VDDQA	DVDD	VDDO1	PRTAD0	VDDQB	DVDD	TDB_13	VDDQB	TDB_12	VDDQB	VREFTB
M	RESTA	TDA_5	TDA_10	TDA_9	TDA_7	VDDQA	DGND	PRTAD3	DGND	DVDD	DGND	DVDD	VDDQB	TDB_11	TDB_9	TDB_10	TDB_4	RESTB
N	VDDQA	DGND	TDA_6	DGND	TDA_2	DVDD	DGND	DGND		DGND	DGND	DGND	DVDD	TDB_7	DGND	TDB_6	DGND	VDDQB
P	TXCLK_A	TDA_4	VDDQA	TDA_3	TDA_0	VDDQA	DGND	DGND	DGND	DGND	DGND	DGND	VDDQB	TDB_1	TDB_2	VDDQB	TDB_8	TDB_0
R	DGND	TDA_1	TMS	GPI0	DGND	REFCLK_ASEL	VDDO3	DVDD	AGND	DVDD	AGND	DVDD	VDDO2	TDO	TDI	PRBS_EN	TDB_3	DGND
T	MDC	REFCLK_B_SEL	TRST_N	RATE_A1	DVDD	PD_TRXA_N	VDDRA	VDDD	AVDD	AVDD	VDDD	VDDRB	AVDD	AGND	CLK_OUT_SEL	TCK	TESTEN	TXCLK_B
U	DGND	MDIO	RATE_A0	LOSA	AMUXA	AVDD	AGND	RXAN	RXAP	AGND	AVDD	TXBP	TXBN	AVDD	PD_TRXB_N	RATE_B2	RATE_B1	RATE_B0
V	RESET_N	RATE_A2	PRBSA_PASS	CODEA_EN	AGND	TXAN	TXAP	VDDT	AGND	RXBP	RXBN	VDDT	AGND	AMUXB	PRTAD4	CODEB_EN	LOSB	PRBSB_PASS

2.3 CPRI/OBSAI Specific Operation Modes

The TLK6002 contains an internal low-jitter high quality oscillator that is used as a frequency multiplier for the serdes and other internal circuits of the device. The rate pins (and mdio registers) as well as the SERDES PLL multiplier are used to program the line rate and the REFCLK frequency for various applications. See Appendix B for more details on SERDES reference clock, rate, and multiplier selection (rates beyond the CPRI/OBSAI specific rates).

The TLK6002 is optimized for operation at a serial data rate of 470 Mbit/s through 6.25 Gbit/s. The external differential reference clock has a large operating frequency range allowing support for many different applications. The reference clock frequency must be within ±200 PPM of the incoming serial data rate (±100 PPM of nominal data rate), and have less than 40ps of jitter. Table 2-4 and Table 2-5 show a summary of frequency ranges used for the CPRI and OBSAI applications. The transmit parallel input clock must be frequency locked (0 ppm) to the supplied/selected reference clock (REFCLK_0/1_P/N) frequency.

Table 2-4. CPRI Line Rate Selection(1)

LINE RATE (Mbps)	SERDES PLL MULTIPLIER VALUE	RATE SELECT (PINS OR REGISTER VALUE)	TXCLK_A/B (MHz)	REFCLKP/N (MHz)
6144.00	20/25	Full	307.2	153.60/122.88
4915.20	16/20	Full	245.76	153.60/122.88
3072.00	20/25	Half	153.6	153.60/122.88
2457.60	16/20	Half	122.88	153.60/122.88
1228.80	16/20	Quarter	61.44	153.60/122.88
614.40	16/20	Eighth	30.72	153.60/122.88

(1) In DDR mode TX_CLK frequencies will be half the values in the table above. The table above indicate two possible REFCLK frequencies, 153.60MHz and 122.88MHz which can be used based on the application preference. The Serdes PLL Multiplier (MPY) has been given for each REFCLK frequency respectively. Note that Channel A and B are independent, and their application rates and references clocks are separate.

Table 2-5. OBSAI Line Rate Selection(1)

LINE RATE (Mbps)	SERDES PLL MULTIPLIER VALUE	RATE SELECT (PINS OR REGISTER VALUE)	TXCLK_A/B (MHz)	REFCLKP/N (MHz)
6144.00	20/25	Full	307.2	153.60/122.88
3072.00	20/25	Half	153.6	153.60/122.88
1536.00	20/25	Quarter	76.8	153.60/122.88
768.00	20/25	Eighth	38.4	153.60/122.88

(1) In DDR mode TX_CLK frequencies will be half the values in the table above. The table above indicate two possible REFCLK frequencies, 153.60MHz and 122.88MHz which can be used based on the application preference. The Serdes PLL Multiplier (MPY) has been given for each REFCLK frequency respectively. Note that Channel A and B are independent, and their application rates and references clocks are separate.

2.4 Parallel Interface Modes

2.4.1 20-bit SDR (Single Data Rate) Mode (8b/10b Encoder/Decoder Disabled)

Channel A TX: TDA_[19:0] → TXAP/N (using TXCLK_A). **RX:** RXAP/N → RDA_[19:0] (using RXCLK_A).
Channel B TX: TDB_[19:0] → TXBP/N (using TXCLK_B). **RX:** RXBP/N → RDB_[19:0] (using RXCLK_B).

20 Bits (two symbols) of already encoded (TX) or undecoded (RX) data are transferred per parallel interface clock cycle. Symbols are defined by a group of 10 parallel bits. Note that four symbols are shown in Figure 2-1: Data0[19:10], Data0[9:0], Data1[19:10], Data1[9:0].

Symbol Transmission Order:
When 3.5/3.4 = 0: Data0[19:10] is the first transmitted or received symbol. Data0[9:0] is next, then Data1[19:10].
When 3.5/3.4 = 1: Data0[9:0] is the first transmitted or received symbol. Data0[19:0] is next, then Data1[9:0].

Bit Transmission Order within a Symbol:
When 8.3/2 = 0, Data[19] or Data[9] bits are serially transmitted first or received first respectively per symbol.
When 8.3/2 = 1, Data[10] or Data[0] bits are serially transmitted first or received first respectively per symbol.

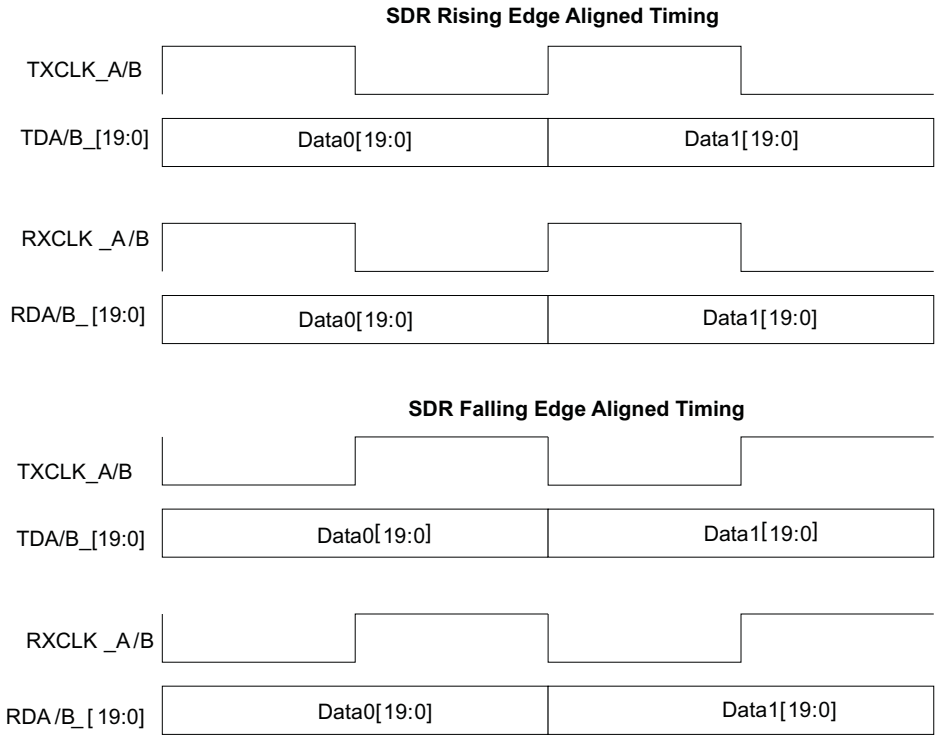


Figure 2-1. 20-bit SDR Parallel Interface Mode

2.5 16-bit SDR (Single Data Rate) Mode (8b/10b Encoder/Decoder Enabled)

Channel A TX: TDA_[18:10,8:0] → TXAP/N (Using TXCLK_A). **RX:** RXAP/N → RDA_[19:0] (Using RXCLK_A).
Channel B TX: TDB_[18:10,8:0] → TXBP/N (Using TXCLK_B). **RX:** RXBP/N → RDB_[19:0] (Using RXCLK_B).

The 16 Bits (two symbols) of unencoded (TX) or decoded (RX) data are transferred per parallel interface clock cycle. Symbols are defined by a group of 9 parallel bits comprising of a K character control bit and a byte of data (plus a high true disparity error or invalid symbol bit in RX only on RD*_[19] and RD*_[9]). Please note that four symbols are shown in Figure 2-1: Data0[18:10]={Control Bit, Data[7:0]}, Data0[8:0] ={Control Bit, Data[7:0]}, Data1[18:10] ={Control Bit, Data[7:0]}, Data1[8:0] ={Control Bit, Data[7:0]}. TXDA_[19], TXDA_[9], TXDB_[19], and TXDB_[9] are unused, and should be grounded in this application mode. See Appendix C for a full list of control characters supported in the 8b/10b encoder/decoder.

Symbol Transmission Order:
When 3.5/3.4 = 0: Data0[18:10] is the first encoded transmitted or decoded received symbol. Data0[8:0] is next, followed by Data1[18:10].
When 3.5/3.4 = 1: Data0[8:0] is the first encoded transmitted or decoded received symbol. Data0[18:10] is next, followed by Data1[8:0].

Bit Transmission Order within a Symbol:
Control Character Bits are always on TD*_[18], TD*_ [8], RD*_[18], RD*_[8]
Data bytes are always on TD*_[17:10], TD*_[7:0], RD*_[17:10], RD*_[7:0].

The most significant bit of the data byte is always on TD*_[17], TD*_[7], RD*_[17], RD*_[7], and is bit "H" in Figure 2-2.

When 8.3/8.2 = 1, The "a" bit in Figure 2-2 is serially transmitted first or received first (typical case, shown below) per symbol.

When 8.3/8.2 = 0, The "j" bit in Figure 2-2 is serially transmitted first or received first (atypical case, reverse from order Figure 2-2) per symbol.

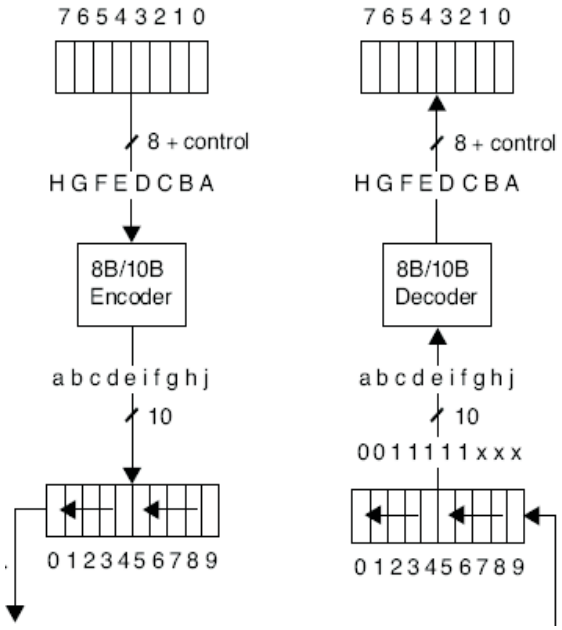


Figure 2-2. 16-bit SDR Parallel Interface Mode (Serial Bit Order)

Figure 2-1 shows the two modes of operation in SDR mode, rising edge aligned mode and falling edge aligned mode. In rising edge aligned mode, TDA_* and TDB_* inputs are sampled on the falling edges of TXCLK_A and TXCLK_B respectively. In falling edge aligned mode, TDA_* and TDB_* inputs are sampled on the rising edge of TXCLK_A and TXCLK_B respectively. In rising edge aligned mode, RDA_* and RDB_* are timed such that an external device can sample the data using the falling edge of RXCLK_A and RXCLK_B respectively. In falling edge aligned mode, RDA_* and RDB_* are timed such that an external device can sample the data using the rising edge of RXCLK_A and RXCLK_B respectively.

2.6 20-bit DDR (Double Data Rate) Mode (8b/10b Encoder/Decoder Disabled)

When DDR is enabled with the 8b/10b encoder disabled, the data format is identical to that of "20-bit SDR (Single Data Rate) Mode (8b/10b Encoder/Decoder Disabled)" mode, except that four symbols are transferred per parallel interface clock cycle instead of two. See the referenced previous section for further details. Figure 2-3 shows the two modes of operation in DDR mode, source centered and source aligned mode. In source centered mode, TDA_* and TDB_* inputs are sampled on the rising and falling edges of TXCLK_A and TXCLK_B respectively. In source aligned mode, TDA_* and TDB_* inputs arrive simultaneously with TXCLK_A and TXCLK_B respectively, and the TXCLK_A and TXCLK_B sampling window is created internal to TLK6002 by delaying the clock. In source centered mode, RDA_* and RDB_* are timed such that an external device can sample the data using RXCLK_A and RXCLK_B respectively, where the appropriate timing window for sampling is created by TLK6002. In source aligned mode, RDA_* and RDB_* are aligned with RXCLK_A and RXCLK_B respectively at the outputs of TLK6002, and the sampling window must be created external to TLK6002.

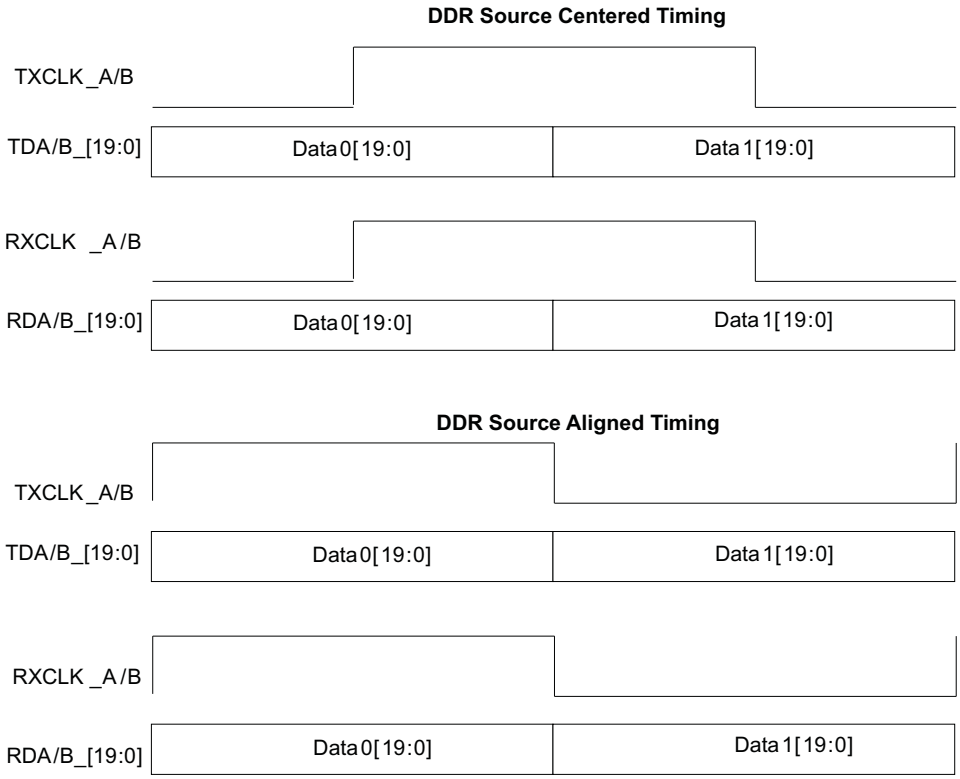


Figure 2-3. 20-bit DDR Parallel Interface Mode

2.7 16-bit DDR (Double Data Rate) Mode (8b/10b Encoder/Decoder Enabled)

When DDR is enabled with the 8b/10b encoder enabled, the data format is identical to that of "16-bit SDR (Single Data Rate) Mode (8b/10b Encoder/Decoder Enabled)" mode, except that four symbols are transferred per parallel interface clock cycle instead of two. See the referenced previous section for further details.

2.8 Parallel Interface Clocking Modes

The TLK6002 supports source centered timing and source aligned DDR timing on the parallel receive output bus. TLK6002 also supports rising edge aligned and falling edge aligned SDR timing on the parallel receive output bus. See Figure 2-4 for more details.

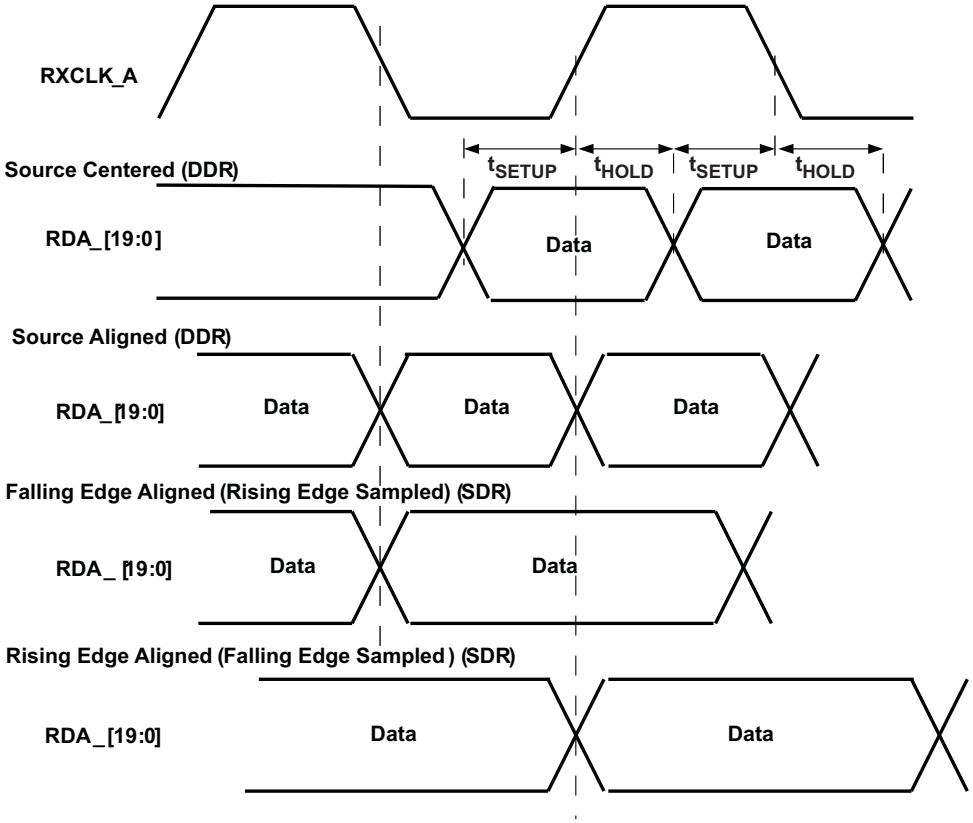


Figure 2-4. Receive Interface Timing – Source Centered/Aligned (Channel A is shown).

The transmit input timing modes are shown in Figure 2-5.

Transmit SDR/DDR input timing modes supported are similar to RX modes.

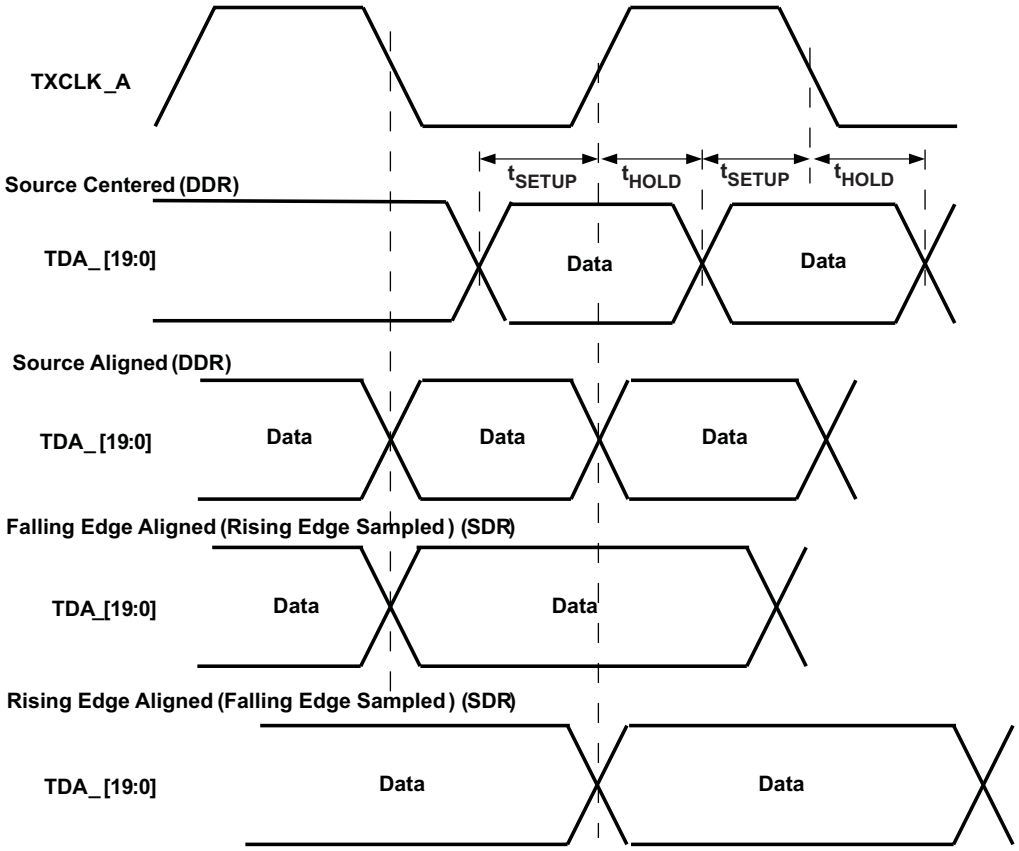


Figure 2-5. Transmit Interface Timing (Channel A is shown).

2.9 Scrambler and De-scrambler

TLK6002 incorporates a scrambling function located before the 8b/10b encoder in the transmit datapath, and a de-scrambling function located after the 8b/10b decoder in the receive datapath. The scrambler and de-scrambler can be enabled/disabled using the MDIO management serial interface.

The transmitter applies a 7-degree polynomial to data bytes (not control), and the inverse operation is performed by the receiver.

The scrambler/descrambler should be disabled if the 8b/10b encoder/decoder is disabled.

To achieve randomness between transmitting lanes, transmitters can be programmed to have differing scrambling offset. Each transmitter seed value is programmed into a register which will be used by that transmitter. The user should program unique seed values for adjacent TX links.

The receivers also have their own de-scrambling seed value registers. The receiver's de-scrambling seed value must be programmed to be the same as the corresponding transmitting end of the link. There is no training sequence for transmitting the seed values to the receiver.

The scrambler is a 7-degree polynomial, linear feedback shift register (LFSR). The polynomial is; ($X^7 + X^6 + 1$). K28.1, K28.5, or K28.7 characters reset the LFSR to the seed value. The bit pattern repeats every 127 bits.

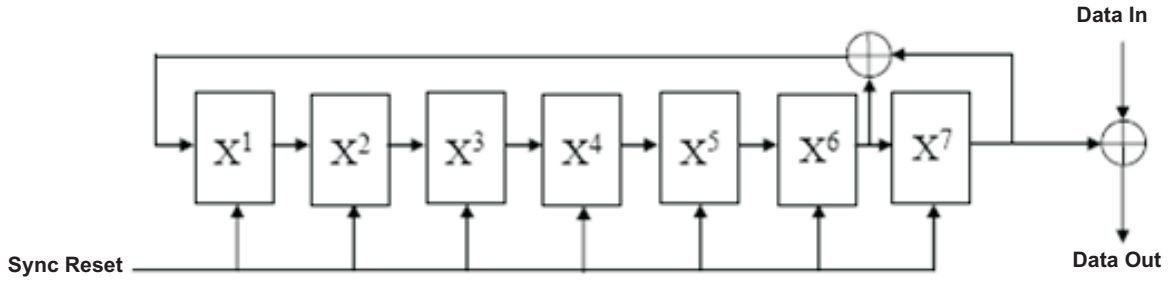


Figure 2-6. 7-Degree Polynomial Scrambler

2.10 Power Down Mode

The TLK6002 can be put in power down either through device input pins or through MDIO control register (1.15). PD_TRXA_N: Active low, powers down channel A. PD_TRXB_N: Active low, powers down channel B.

The MDIO management serial interface remains operational when in register based power down mode (1.15 asserted for both channels), but status bits may not be valid since the clocks are disabled. The serial outputs and parallel output interface signals are high impedance when in power down mode. See the detailed per pin description for behavior of each device I/O signal during pin based and register based power down.

2.11 Parallel to Serial (Transmit):

In the transmit direction, the device accepts parallel input data on the TDA_[19:0] and TDB_[19:0] input pins and converts the data into an optionally scrambled 8b/10b encoded serial stream on the TXAP/N and TXBP/N serial output pins.

2.12 Serial to Parallel (Receive)

Serial data is received on the RXAP/N and RXBP/N pins, and optionally descrambled and 8b/10b decoded and converted to parallel output data pins RDA_[19:0] and RDB_[19:0]. The interpolator and clock recovery circuit will lock to the data stream if the incoming serial rate is within ±200 PPM of the reference clock for the channel. The recovered byte clock is used to retime and deserialize the input data stream, and is always synchronous with the parallel output data.

2.13 High Speed CML Output

The high speed data output driver is implemented using Current Mode Logic (CML) with integrated pull up resistors, requiring no external components. The transmit outputs must be AC coupled.

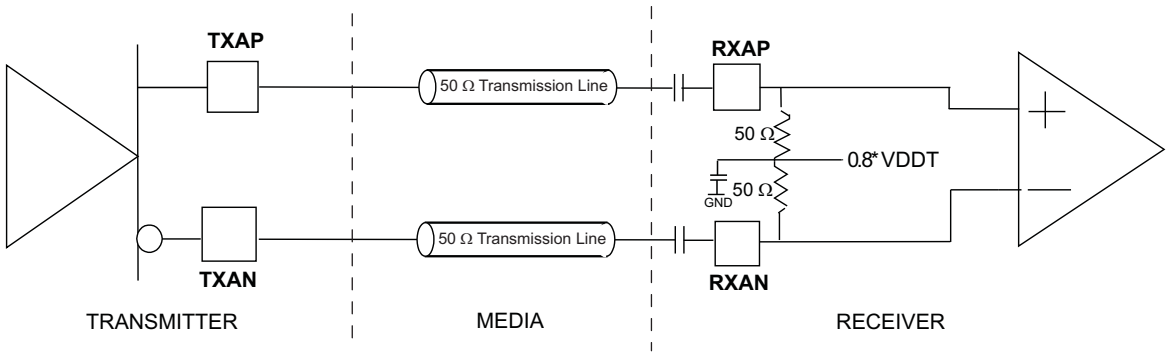


Figure 2-7. Example of High Speed I/O AC Coupled Mode (Channel A is shown).

Current Mode Logic (CML) drivers often require external components. The disadvantage of the external component is a limited edge rate due to package and line parasitic. The CML driver on TLK6002 has on-chip 50Ω termination resistors terminated to VDDT, providing optimum performance for increased speed requirements. The transmitter output driver is highly configurable allowing output amplitude and de-emphasis to be tuned to a channel's individual requirements. Software programmability allows for very flexible output amplitude control. Only AC coupled output mode is supported.

When transmitting data across long lengths of PCB trace or cable, the high frequency content of the signal is attenuated due to the skin effect of the media. This causes a "smearing" of the data eye when viewed on an oscilloscope. The net result is reduced timing margins for the receiver and clock recovery circuits. In order to provide equalization for the high frequency loss, 3-tap finite impulse response (FIR) transmit de-emphasis is implemented. A highly configurable output driver maximizes flexibility in the end system by allowing de-emphasis and output amplitude to be tuned to a channel's individual requirements. Output swing control is via MDIO.

See Figure 4-2 for output waveform flexibility. The level of de-emphasis is programmable via the MDIO interface through control registers (2.12:4) through pre-cursor and post-cursor settings. Users can control the strength of the de-emphasis to optimize for a specific system requirement.

2.14 High Speed Receiver

The high speed receiver is differential CML with internal termination resistors. The receiver requires AC coupling. The termination impedances of the receivers are configured as 100Ω with the center tap weakly tied to 0.8×VDDT with a capacitor to create an AC ground.

TLK6002 receiver incorporates an adaptive equalizer. This circuit compensates for channel insertion loss by amplifying the high frequency components of the signal, reducing inter-symbol interference. Equalization can be enabled or disabled per register settings. Both the gain and bandwidth of the equalizer are controlled by the receiver equalization logic.

2.15 Loss Of Signal Output Signal Generation (LOS)

Loss of input signal detection is based on the voltage level of each serial input signal RXAP/N and RXBP/N. Anytime the serial receive input differential signal peak to peak voltage level is ≤75 mVdfpp, LOSA or LOSB are asserted (high true) respectively for Channel A and Channel B (if enabled, disabled by default). Note that an input signal ≥ 150 mVdfpp is required for reliable operation of the loss of signal detection circuit. If the input signal is between these two ranges, the SERDES will operate properly, but the LOS indication will not be valid (or robust). The LOS indications are also directly readable through the MDIO interface in register bits (5.2). The LOS indication per channel can be enabled through register bit 6.10 (defaults to disabled).

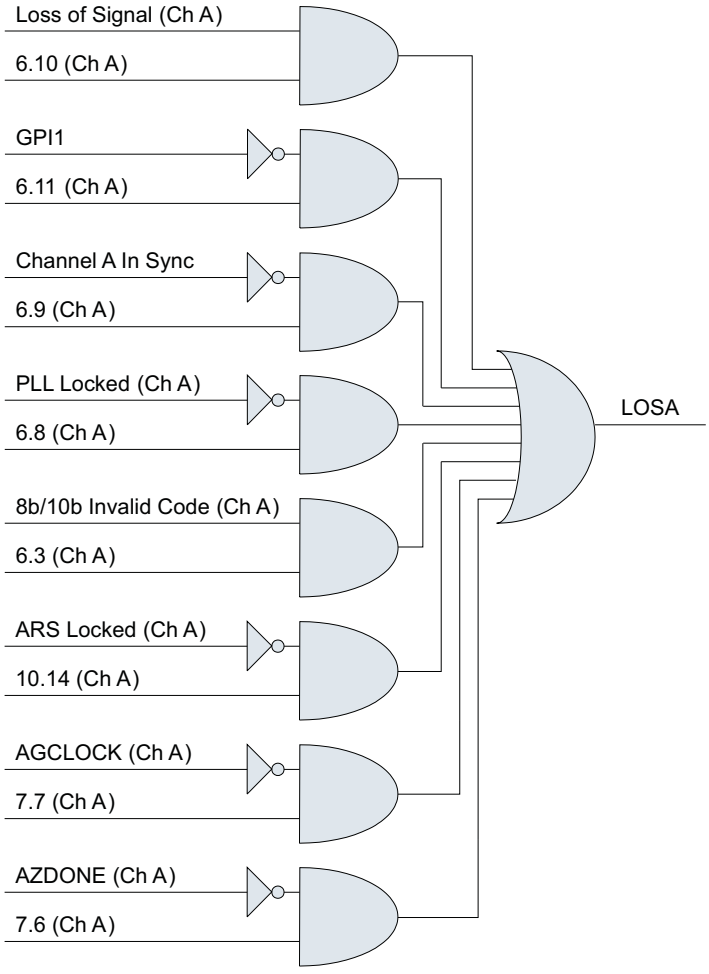
The following additional critical status conditions can be combined with the loss of signal condition enabling additional realtime status signal visibility on the LOSA and LOSB outputs per channel:

1. GPI1 – Inverted and Logically OR'd (Register 6.11 enable) with LOS condition(s) when enabled – This input signal, when enabled (disabled by default), is inverted and logically OR'd with the internally generated LOS condition (on both channels) to allow easy overlay of additional board or external device status with the other LOSA/LOSB indications.
2. Loss of Channel Synchronization Status – Logically OR'd with LOS condition(s) when enabled – (Register 6.9 enabled). Loss of channel synchronization can be optionally logically OR'd (disabled by default) with the internally generated LOS condition (per channel). In 20-bit operational mode, the comma detection circuit must be enabled to actually enable this OR function. If it is not, this function is not OR'd with the other LOS generating conditions. This bit should not be enabled unless comma detection is enabled.
3. Loss of PLL Lock Status – Logically OR'd with LOS condition(s) when enabled – (Register 6.8 enabled). The internal PLL loss of lock status bit is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
4. Receive 8b/10b Decode Error (Invalid Code Word or Running Disparity Error) – Logically OR'd with

LOS condition(s) when enabled – (Register 6.3 enabled). The occurrence of an 8b/10b decode error (invalid code word or disparity error) is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).

5. ARS_Locked (ARS State Machine Currently Locked) – Inverted and Logically OR'd with LOS condition(s) when enabled – (Register 10.14 enabled). ARS State Machine unlocked indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
6. AGCLOCK (Active Gain Control Currently Locked) – Inverted and Logically OR'd with LOS conditions(s) when enabled – (Register 7.7 enabled). RX SERDES adaptive gain control unlocked indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
7. AZDONE (Auto Zero Calibration Done) – Inverted and Logically OR'd with LOS conditions(s) when enabled – (Register 7.6 enabled). RX SERDES auto zero not done indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).

See Figure 2-8, which shows the detailed implementation of the LOSA signal.



NOTE: LOSA is asserted (driven high) during a failing condition, and deasserted (driven low) otherwise. Any combinations of status signals may be enabled onto LOSA/B based on MDIO register bits indicated above. LOSB circuit is similar.

Figure 2-8. LOSA – Logic Circuit Implementation

2.16 Receive Datapath Error Condition Operation

The receive datapath (parallel output), when the 8b/10b decoder is enabled, automatically replaces the received symbol with K30.7 (control = 1, data = 0xFE) in the case of an invalid code word or 8b/10b disparity error.

The following additional conditions optionally enable replacement of received data with K30.7 (control = 1, data = 0xFE) (when enabled through MDIO) when 8b/10b decoding is enabled, or replace the parallel output data with all zero data if the 8b/10b decoder is disabled:

1. Loss of Signal Status – (character replacement enabled through register bit 6.6, disabled by default).
2. Loss of Channel Synchronization Status – (character replacement enabled through register bit 6.5, disabled by default). This bit should not be enabled unless comma detection is enabled.

   Note: Achieving channel synchronization is not possible if register bit 6.6 is high and LOS is detected.
3. Loss of PLL Lock Status – (character replacement enabled through register bit 6.4, disabled by default)
4. GPI1 – (if GPI1=0, character replacement enabled through register bit 6.7, disabled by default)
5. AZDONE – (if AZDONE=0, character replacement enabled through register bit 7.4, disabled by default)
6. AGCLOCK – (if AGCLOCK=0, character replacement enabled through register bit 7.5, disabled by default)

2.17 Loopback Support

TLK6002 supports several loopback configurations.

Local loopback accepts parallel input data, and returns that data on the parallel output for the same channel.

Remote loopback accepts serial input data, and returns that data on the serial output for the same channel.

Shallow local loopback data traverses the entire transmit datapath except for serialization, and is returned through the entire receive datapath (except for deserialization). Data is not serialized or deserialized.

Deep local loopback data traverses the entire transmit datapath including serialization, and is returned through the entire receive datapath (including serialization). Data is both serialized and deserialized.

Deep remote loopback data traverses the entire receive datapath including the 20-bit output register, and is returned through the entire transmit datapath (excluding the parallel input buffers). Data is both deserialized and serialized.

Shallow remote loopback data traverses the entire receive datapath until just before the 20-bit output register, and is returned through the entire transmit datapath (excluding the parallel input buffers). Data is both serialized and deserialized.

Figure 2-9 and Figure 2-10 show all four loopback modes of operation.

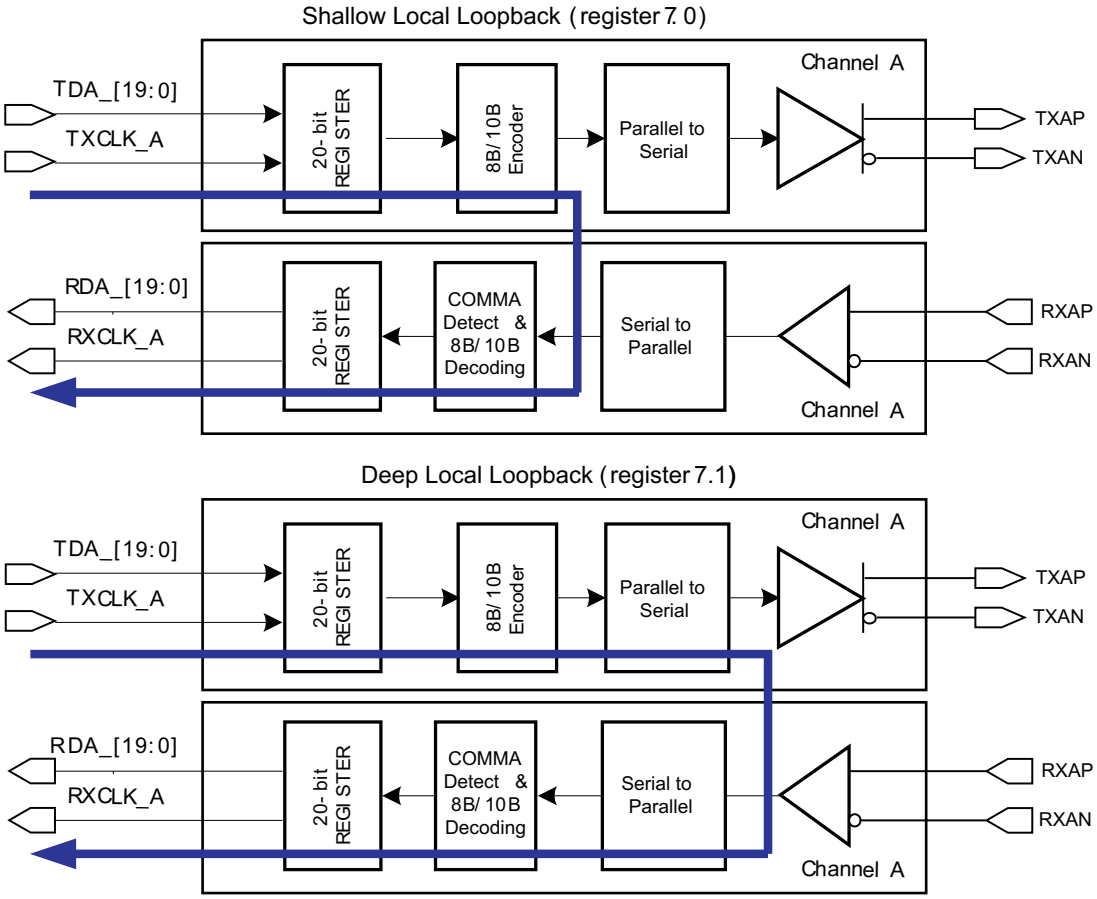


Figure 2-9. TLK6002 Shallow and Deep Local Loopback (Channel A)

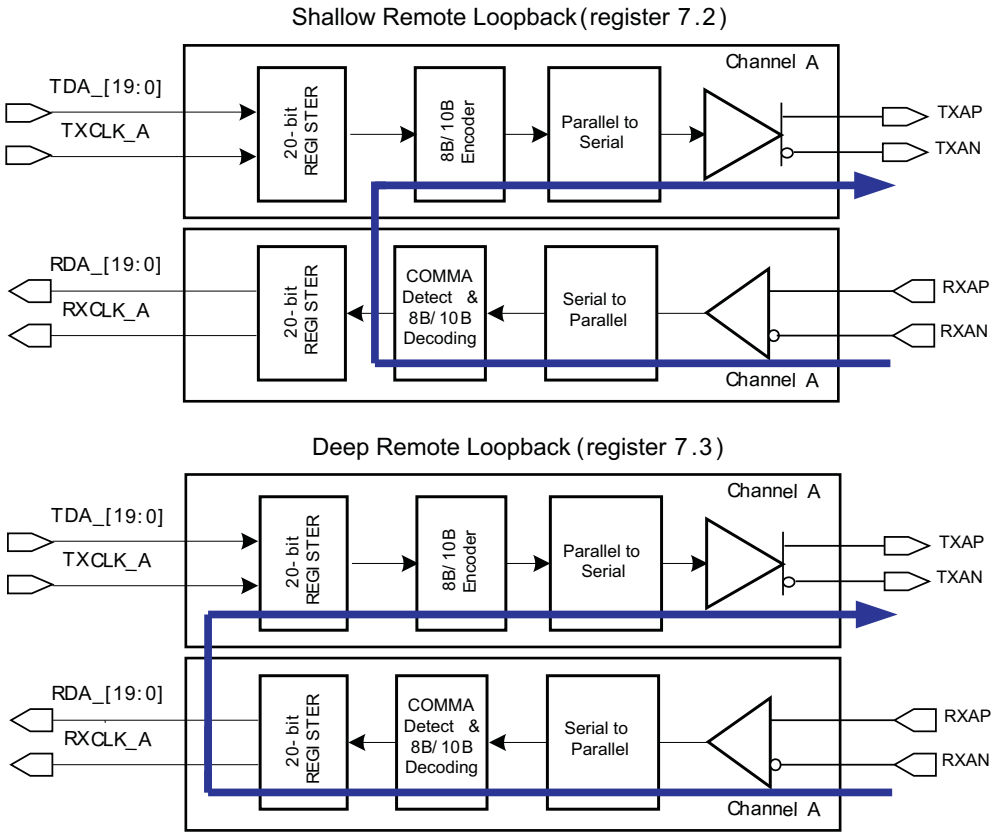


Figure 2-10. TLK6002 Shallow and Deep Remote Loopback (Channel A)

2.17.1 Link Test Functions

The TLK6002 has an extensive suite of built in test functions to support system diagnostic requirements. Each channel has an internal test pattern generator and verifier. Several patterns can be selected via the MDIO that offer extensive test coverage. The test patterns supported are: 2^7-1, 2^{23}-1, 2^{31}-1 PRBS (Pseudo Random Bit Stream), CRPAT Short/Long frequency patterns.

2.18 Serial Retime Mode

TLK6002 supports serial retime mode of operation. Serial retime mode is enabled through an mdio register bit.

In serial retime mode mode:

- Incoming serial data on RXAP/N is sent to both RDA_[19:0] parallel and TXBP/N serial outputs.
- Incoming serial data on RXBP/N is sent to both RDB_[19:0] parallel and TXAP/N serial outputs.

In serial retime mode, the incoming serial data rate on Channel A must be synchronous (0 ppm) to the reference clock supplied to Channel B SERDES. Also, the incoming serial data rate on Channel B must be synchronous (0 ppm) to the reference clock supplied to Channel A SERDES.

Note that latency measurement is not possible when in serial retime mode of operation.

Figure 2-11 shows operation of TLK6002 in serial retime mode:

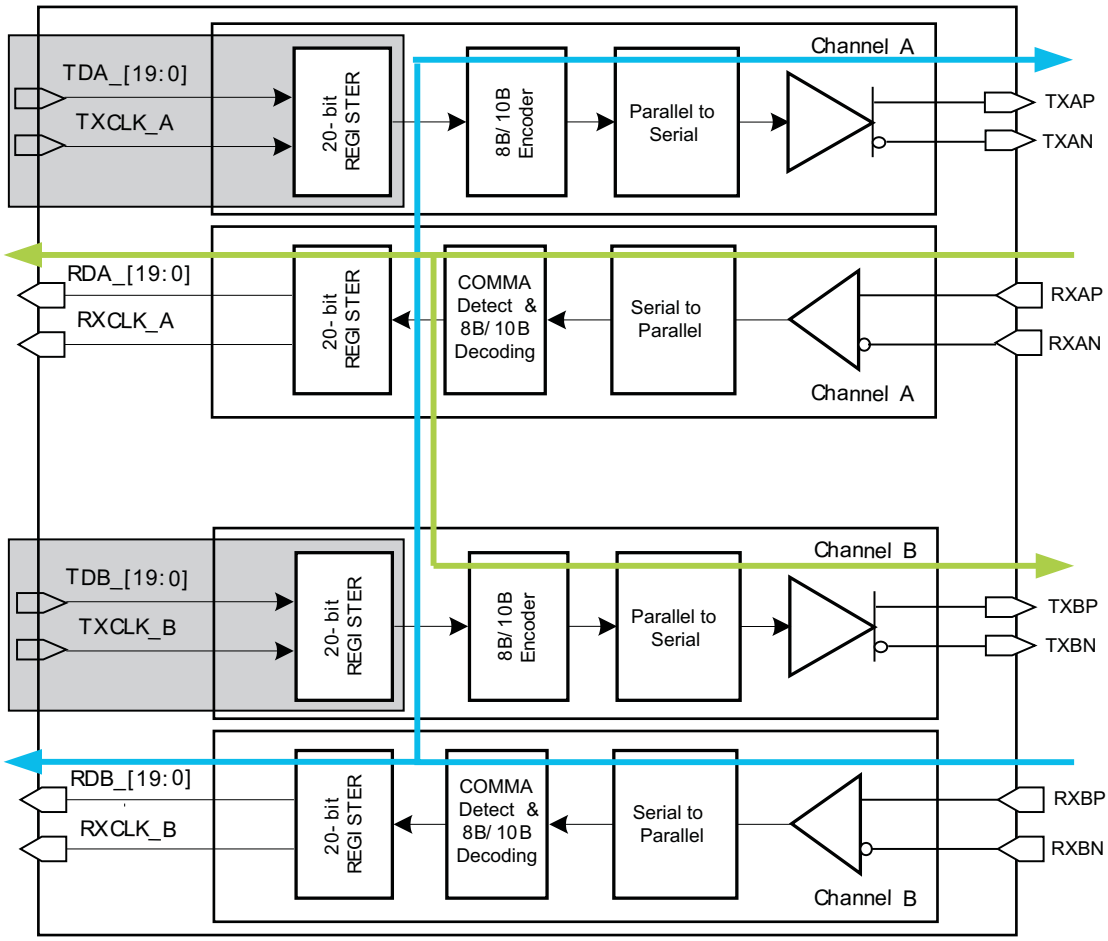


Figure 2-11. TLK6002 – Serial Retime Mode of Operation

2.19 Latency Measurement Function

The TLK6002 includes a round trip latency measurement function to support CPRI and OBSAI base station applications. The elapsed time from a comma (either encoded or unencoded) detected in the transmit direction of a particular channel to a comma detected in the receive direction of the same channel is measured and reported through the MDIO interface (TDA_[19:0] → RDA_[19:0] -or- TDB_[19:0] → RDB_[19:0]). The function operates on one channel at a time. When 8b/10b encoding/decoding is enabled, the following three control characters (containing commas) are monitored:

1. K28.1 (control = 1, data = 0x3C)
2. K28.5 (control = 1, data = 0xBC)
3. K28.7 (control = 1, data = 0xFC).

When 8b/10b encoding/decoding is disabled, the lower 7 bits of the Tx and Rx data stream are monitored for either positive (7'b0011111) or negative (7'b1100000) comma characters.

Whether 8b/10b encoding/decoding is enabled or not, comma detection in the receive datapath must be enabled (register bit 3.7).

The result of this measurement is readable through the MDIO interface through a 20-bit register. The accuracy of the measurement is a function of the serial bit rate which the channel being measured is operating at. The register will return a value of 0xFFFFF if the duration between transmit and receive comma detection exceeds the depth of the counter. Only one measurement value is stored internally until the 20-bit results counter is read. The counter will return zero in cases where a transmit comma was never detected (indicating the results counter never began counting).

In full rate mode, the latency measurement function runs off of an internal clock which is equal to the frequency of the transmit serial bit rate divided by four. In half rate mode, the latency measurement function runs off of an internal clock which is equal to the serial bit rate divided by two. In quarter rate mode, the latency measurement function runs off of an internal clock which is equal to the serial bit rate. In eighth rate mode, the latency measurement function runs off of a clock which is equal to twice the serial bit rate. The latency measurement accuracy in all cases is equal to plus or minus one latency measurement clock period. The measurement clock can be divided down if a longer duration measurement is required, in which case the accuracy of the measurement is accordingly reduced. The high speed latency measurement clock is divided by either 1, 2, 4, or 8 via register 16.5:4. The measurement clock used is always selected by the channel under test. The high speed latency measurement clock may only be used when operating at one of the eight serial rates specified in the CPRI/OBSAI specifications. It is also possible to run the latency measurement function off of the recovered byte clock for the channel under test (and gives a latency measurement clock frequency equal to the serial bit rate divided by 10) via register bit 16.2 (where the 16.5:4 divider value setting is ignored).

The accuracy for the standard based CPRI/OBSAI application rates is shown in Table 2-6, and assumes the latency measurement clock is not divided down per user selection (division is required to measure a duration greater than 682 µs). For each division of 2 in the measurement clock, the accuracy is also reduced by a factor of two.

Table 2-6. CPRI/OBSAI Latency Measurement Function Accuracy (Undivided Measurement Clock)

Gbps	Rate	Clock Frequency (GHz)	Accuracy (± ns)
0.6144	Eighth	1.2288	0.8138
0.768	Eighth	1.536	0.6510
1.2288	Quarter	1.2288	0.8138
1.536	Quarter	1.536	0.6510
2.4576	Half	1.2288	0.8138
3.072	Half	1.536	0.6510
4.9152	Full	1.2288	0.8138
6.144	Full	1.536	0.6510

The locations where the comma transmission and reception are measured in TLK6002 are shown in Figure 2-12.

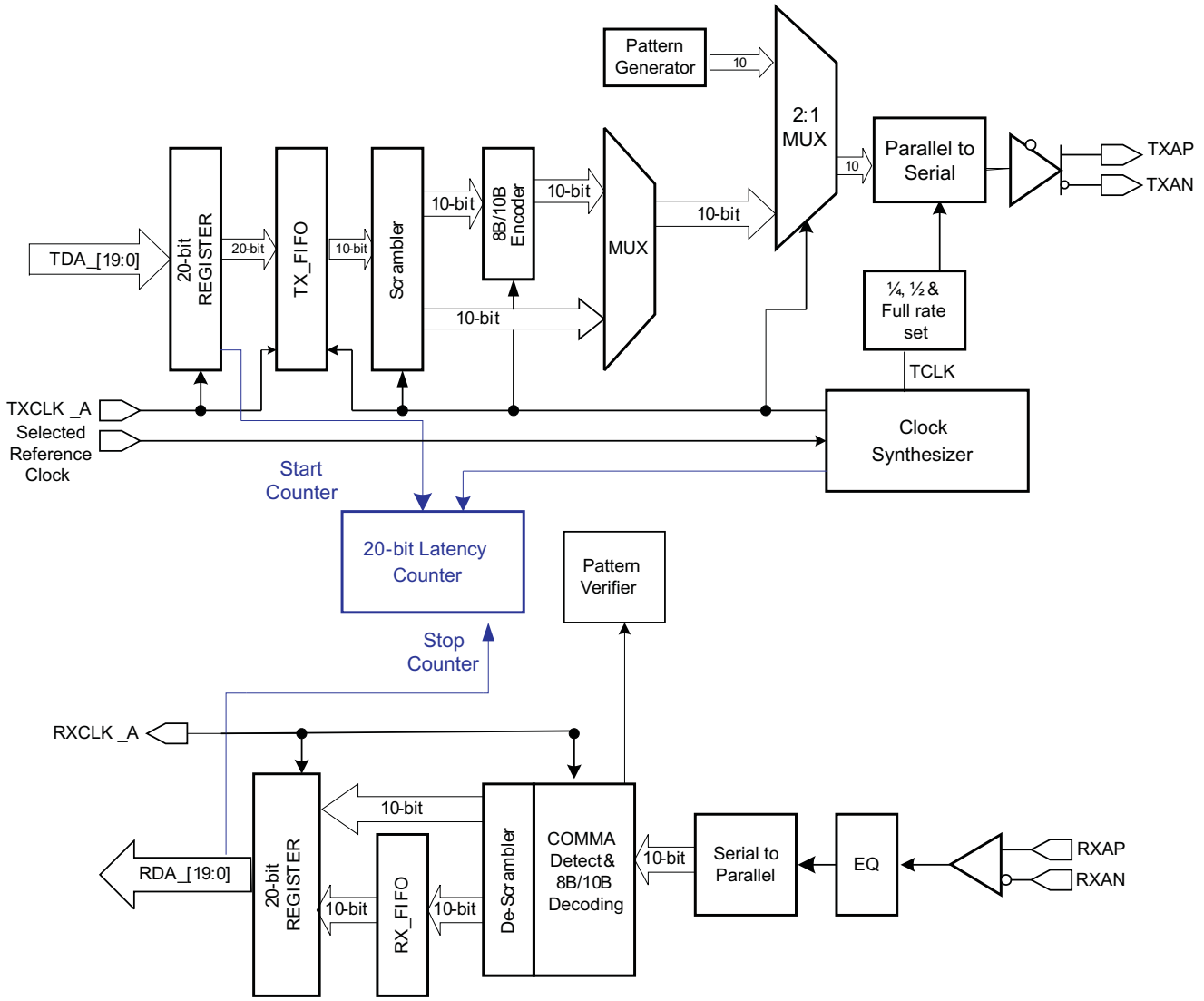


Figure 2-12. Location of TX and RX Comma Character Detection (Only Channel A Shown)

2.20 CPRI/OBSAI Automatic Rate Sense (ARS) Function

An automatic rate sense (ARS) function is implemented in TLK6002 to facilitate determination of the incoming CPRI/OBSAI serial link rate per channel.

When ARS is enabled, only three device input reference clock frequencies are supported: 122.88, 153.6, and 307.2 MHz. ARS should not be enabled unless one of these three frequencies is available on either REFCLK_0_P/N or REFCLK_1_P/N.

The ARS function per channel can operate off of either reference clock (REFCLK_0_P/N or REFCLK_1_P/N), and is selected through device pins REFCLK_A_SEL for Channel A, and REFCLK_B_SEL for Channel B (or alternatively mdio registers). The reference clock rate selection is selected through channel A or B MDIO register bits (ARS_REF_FREQ[1:0], register bits 11.15:14), and must be programmed for proper ARS operation (unless the default values matches the reference clock input frequency).

Using any one of the three supported reference clock frequencies allows all eight currently defined CPRI and OBSAI rates to be achieved with a single reference clock frequency, and eliminates the need for external hardware to support multiple frequencies for OBSAI and CPRI operation. See Table 2-7 for a list of supported CPRI/OBSAI rates.

ARS can be enabled/disabled through device pins (RATE_A/B) or channel A or B MDIO register bits (ARS_EN[1:0], register bits 10.13:12), Software control is enabled by setting RATE_A/RATE_B pins to 100. Pin control is enabled by setting RATE_A/B pins to 101/110/111. ARS can be enabled or disabled independently on each channel.

ARS does not support determination of incoming serial rates other than the eight defined by the CPRI/OBSAI specifications. ARS should not be enabled unless one of those incoming serial rates is anticipated. See Table 2-7 for a list of the supported CPRI/OBSAI incoming serial rates.

When ARS is enabled, a state machine will continuously loop through (and override previously programmed) relevant SERDES control settings for a given input reference clock frequency until either an incoming serial bit rate is successfully determined (indicated by assertion of channel A or B MDIO register ARS_LOCKED, register bit 5.10), or the ARS function is disabled (either through device pin or MDIO software control). Note that the order attempted is always from the highest serial bit rate to the lowest serial bit rate. There is an MDIO register enable per serial bit rate per channel (ARS_SBR_ENABLE[7:0], register bit 11.13:6), such that any number between one and eight of the supported incoming serial rates can be determined. If an incoming serial bit rate is successfully determined, and then subsequently lost, the state machine will automatically continue searching for a stable rate (as long as ARS is not disabled), first starting with the last successful rate (if existing, effecting a single retry of the last working rate), and then continuing down sequentially through the enabled lower serial rates (or if there are none, starting over with the highest enabled incoming serial rate settings).

The ARS function monitors the incoming 8b/10b encoded serial receive data, using both the comma character and 8b/10b disparity errors for a given channel, to determine and validate the incoming serial data rate. The channel synchronization state machine is implemented as specified in IEEE802.3-2002 Clause 36, Figure 36-9, Page 62. The channel synchronization state machine flowchart is shown in Figure 2-14 Channel Synchronization Flowchart. The 8b/10b decoder is used in tandem with the channel synchronization state machine to determine if rate sense is successful at a particular device setting. Note that the 8b/10b decoder is used for the ARS function even if 8b/10b encoding/decoding is disabled for the datapath of the channel. Parallel output data is always output in the pin/software selected format (i.e., unencoded or 8b/10b encoded or byte aligned), and is not a function of whether ARS is enabled. Also note that the RX SERDES CDR lock indication (AGCLOCK) qualifies channel synchronization.

When an ARS enabled channel is found to be in the channel synchronization state, the following rate settings (RATE_TX[1:0] register bits 1.7:6, RATE_RX[1:0] register bits 1.5:4, PLL_MULT[3:0] register bits 1.3:0) are available to be read through the MDIO interface, as indicated by the per channel ARS Locked register bit (ARS_LOCKED register bit 5.10) being asserted high. If the ARS function is not currently locked onto the incoming serial data, the ARS locked register bit (ARS_LOCKED register bit 5.10) will read deasserted, and the rate settings are not valid (although they are always readable). It is also possible through MDIO configuration to make the inverse of ARS_LOCKED indication visible on the LOSA/B outputs per channel, and in this mode can be used as a software interrupt notification. After a successful rate determination is made, the ARS function will continue to monitor channel synchronization status. If channel synchronization is lost, the ARS state machine will begin looping through SERDES settings (reattempting with the last working setting one time rather than with the next different setting) until either ARS is disabled or channel synchronization is achieved. The ARS state machine will stay in a particular setting (expected serial rate) attempting to achieve rate determination for the number of reference clock cycles programmed in ARS_INTERVAL[20:0] (per channel register bits 11.4:0 / 12.15:0), which indicates a duration of time defined as the number of reference clock periods times 1024. This register is sized such

that greater than 4.5 seconds of time can be programmed per attempted interval. Thus, the ARS state machine will attempt to determine a particular serial rate for a programmable number of reference clock periods where channel synchronization cannot be established before attempting the next (and different) lower serial bit rate, in a repeating/looping fashion when the lowest enabled serial bit rate is attempted unsuccessfully.

The ARS function overrides the following SERDES register settings (RATE_TX / RATE_RX / PLL_MULT). MDIO writes to these registers do not impact the actual values controlling internal SERDES device settings as long as ARS is enabled for that channel, and reads instead return the current settings (which may or may not be valid) as controlled by the ARS state machine (and does so until ARS is disabled).

Table 2-7. ARS Looped Device Settings (Looping order highest → lowest enabled bit rate)

ARS Rate / Scale / Multiplier Settings Per Reference Clock				Reference Clock (MHz)		
				153.6	122.88	307.2
Standard	**Serial Rate (Gbps)**	**Rate**	**Rate Scale**	**SERDES Multiplier Setting Loop**		
CPRI	0.6144	Eighth	4	16	20	8
OBSAI	0.768	Eighth	4	20	25	10
CPRI	1.2288	Quarter	2	16	20	8
OBSAI	1.536	Quarter	2	20	25	10
CPRI	2.4576	Half	1	16	20	8
CPRI/OBSAI	3.072	Half	1	20	25	10
CPRI	4.9152	Full	0.5	16	20	8
CPRI/OBSAI	6.144	Full	0.5	20	25	10

2.21 Clock Out Generation In ARS Mode (CLK_OUT_P/N)

Table 2-8 shows the CLK_OUT_P/N output clock frequency in each of the three reference clock frequencies.

Table 2-8. ARS CLK_OUT_P/N Frequencies

ARS CLK_OUT_P/N Frequency Per Reference Clock		VCO Freq./2 (GHz)	Selected Reference Clock (MHz)					
			153.6	122.88	307.2	153.60	122.88	307.20
Standard	Serial Rate (Gbps)		CLK_OUT Division from VCO Frequency/2			CLK_OUT_P/N Frequency (MHz)		
CPRI	0.6144	1.2288	8	20	8	153.60	61.44	153.60
OBSAI	0.768	1.5360	10	25	10	153.60	61.44	153.60
CPRI	1.2288	1.2288	8	20	8	153.60	61.44	153.60
OBSAI	1.536	1.5360	10	25	10	153.60	61.44	153.60
CPRI	2.4576	1.2288	8	20	8	153.60	61.44	153.60
CPRI/OBSAI	3.072	1.5360	10	25	10	153.60	61.44	153.60
CPRI	4.9152	1.2288	8	20	8	153.60	61.44	153.60
CPRI/OBSAI	6.144	1.5360	10	25	10	153.60	61.44	153.60

If supplying reference clock through an external clock jitter cleaning device, the VCXO used with the external cleaning device should be chosen such that REFCLK maintains ±100 ppm accuracy during ARS rate determination, since CLK_OUT behavior will not be deterministic during changes between settings. Per the above table, note that CLK_OUT is always a fixed frequency and attempts to remain synchronous (0 ppm) to the incoming serial data rate.

If reference clock of 153.6 MHz is selected, and an external clock jitter cleaning device is used, the clock cleaning device will need to be configured to multiply the output clock by 1x, since CLK_OUT_P/N is 153.6MHz.

If reference clock of 122.88 MHz is selected, and an external clock jitter cleaning device is used, the clock cleaning device will need to be configured to multiply the output clock by 2x, since CLK_OUT_P/N is 61.44MHz.

If reference clock of 307.2 MHz is selected, and an external clock jitter cleaning device is used, the clock cleaning device will need to be configured to multiply the output clock by 2x, since CLK_OUT_P/N is 153.6MHz.

Figure 2-13 shows the flow of the ARS state machine:

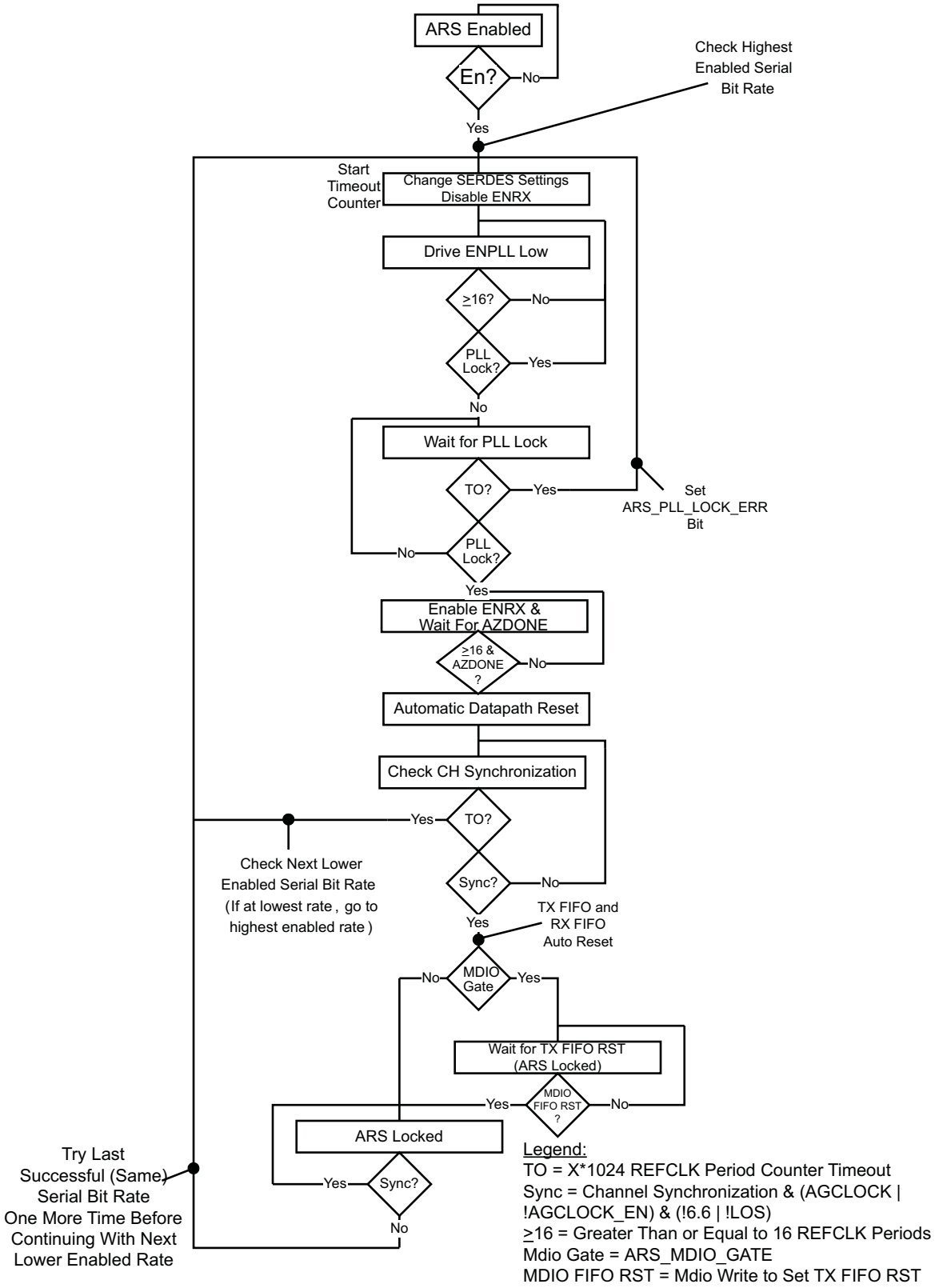


Figure 2-13. ARS State Machine Flowchart

2.22 Transmit Serial Output During ARS Mode

The transmit serial output is always actively driven during ARS mode. The user has flexibility in the value transmitted by the serial output during ARS. Note that since the PLL is shared between a TX and RX channel, that the transmit serial rate will automatically follow the rate setting which ARS is validating in the receive direction (whether it is subsequently determined to be correct or not).

The following bits impact transmitted serial output data:

1. ARS_TX_DATAPATH_OVERRIDE – ARS Transmit Datapath Override – (per channel Register bit 10.10) – When asserted, in tandem with register (ARS_TX_DATA[9:0], register bits 10.9:0), any fixed or repeating sequence of 10 bits can be transmitted during ARS. When deasserted, the transmit parallel interface input data is transmitted and serialized as received during ARS (and may not be deterministic as the TX FIFO will collide on each rate change unless a fixed (static) pattern is input into the parallel input interface making the fifo collision unimpacting to the datapath).
2. ARS_TX_MDIO_GATE – ARS Transmit MDIO Gate – per channel Register bit 10.11 – This bit is only relevant if TX_DATAPATH_OVERRIDE is asserted. When this bit is deasserted, upon successful ARS rate determination, the transmit datapath TX FIFO is automatically reset (centered) and continuity between the parallel input data and serial output is established without MDIO interaction. When this bit is asserted, the transmit datapath will not automatically switch over to serializing parallel input data at the time the ARS state machine successfully validates the incoming serial data rate (although the TX and RX FIFO are both automatically reset). This will give the opportunity for local MDIO firmware to interactively manage any additional device settings. Specifically this gives the device interfacing to TLK6002 the opportunity to read MDIO registers to determine the validated incoming serial rate, manage any other device or system settings required, and also manage TXCLK_A/B synchronicity to REFCLK at the proper data rate. After these steps are complete, the final step is to recenter the TX FIFO (by manually issuing a TX FIFO reset (TXFIFO_RESET register bit 4.2). Transmit datapath reliable operation is fully restored after the TX FIFO reset MDIO write transaction is completed, and datapath continuity between parallel inputs and serial outputs is established.

At the time when ARS rate determination is successful, both a TX and RX FIFO reset is automatically issued internal to TLK6002. Please note that if ARS_TX_MDIO_GATE is not asserted, there may be difficulty in effectively recentering the transmit fifo. Anytime the TX FIFO collides, it automatically recenters itself. This automatic recentering is triggered by the TXCLK_A/B and SERDES TX byte clock (multiplied up and divided down REFCLK_A/B) being asynchronous or having excessive phase drift. The TX FIFO is only effectively centered when the relationship between these two clocks has stabilized, at which point issuing a TX FIFO reset (manual or automatic through collision) will optimally center the TX FIFO. Note that careful external control of the TXCLK_A/B and REFCLK relationship (0 ppm and TXCLK_A/B at the right data rate) must be managed for the mode where ARS_TX_MDIO_GATE is deasserted to work reliably. If the clock relationship is still changing at the time of automatic recenter, the fifo may at some point in the future need to automatically recenter itself (via collision), at which time the transmit serial data will be briefly corrupted before resuming reliable operation. It is recommended that ARS_TX_MDIO_GATE is asserted unless careful system operation has been analyzed.

In any ARS mode, note that the receive datapath software reset (not the same as RX FIFO reset) should not be issued as channel synchronization will be lost, and ARS would inappropriately begin searching for the incoming serial rate again (which is undesirable).

2.22.1 Receive Parallel Output Data During ARS Mode

The parallel outputs are always driven during ARS mode. During ARS mode, it is anticipated that channel synchronization will typically remain lost during the rate determination process, and thus the parallel output data will typically behave predictably as indicated in the previous paragraph labeled Receive Datapath Error Condition Operation.

2.22.2 Receive Parallel Output Clock During ARS Mode

Per channel ARS_RX_CLK_EN (register bit 10.15) allows software programmability as to whether the recovered output byte clock (RXCLK_A/B) is allowed to toggle (dynamically changing rates as the ARS rate determination process executes), or if it is held fixed to zero until the incoming serial rate for the channel has been determined. At the time rate determination is successful, the receive parallel output interface clock is automatically allowed to toggle if it was prevented from toggling during ARS (and enabling toggling is not delayed or gated by MDIO interaction in the case where ARS_TX_MDIO_GATE is asserted).

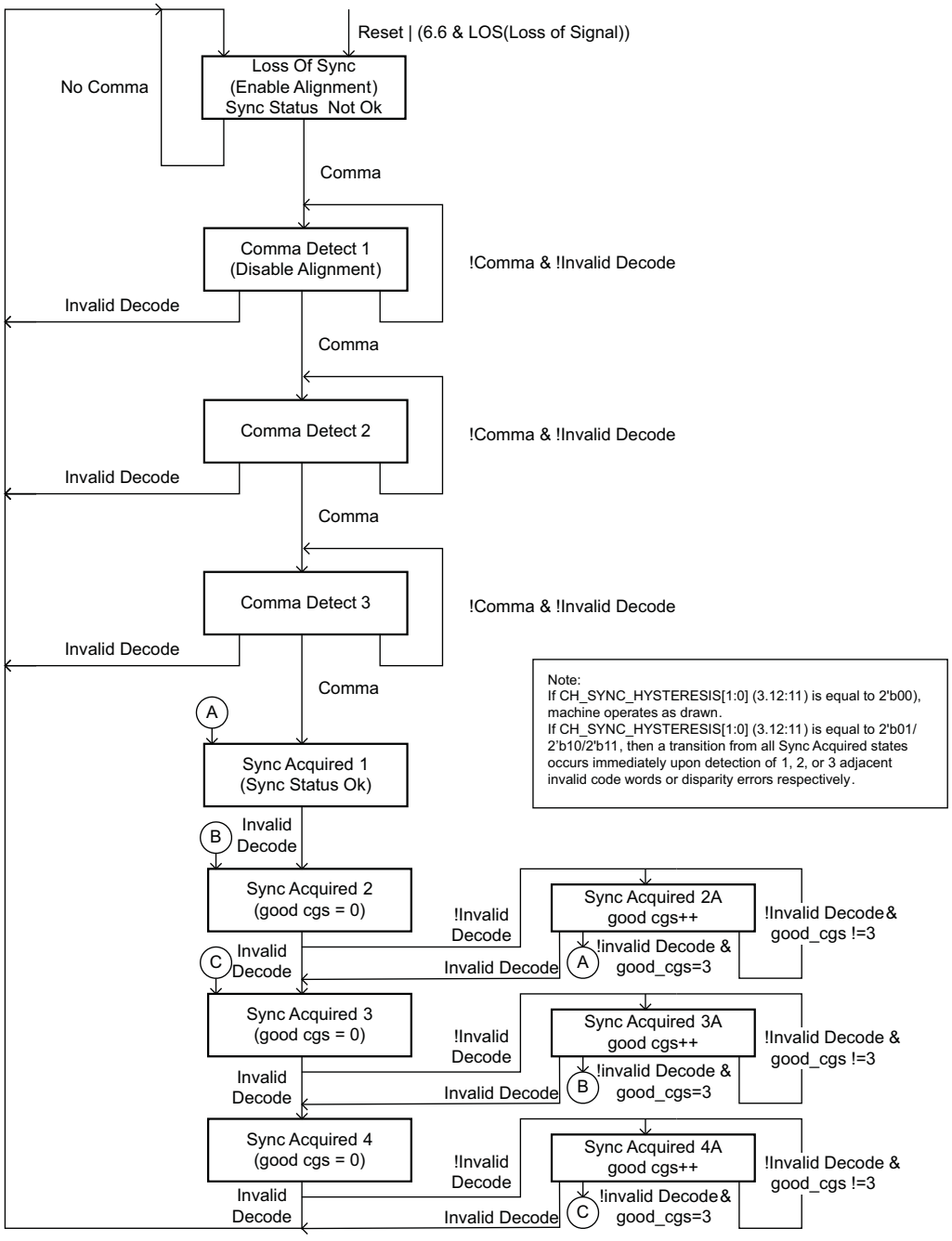


Figure 2-14. Channel Synchronization Flowchart

2.23 Output Clock Selection (CLK_OUT_P/N)

Table 2-9 details CLK_OUT_P/N as a function of device settings.

Table 2-9. CLK_OUT_P/N Frequencies (ARS Enabled and Disabled)

RATE_A[2:0]	RATE_B[2:0]	CLK_OUT_SEL	CLK_OUT_P/N	Selected Channel A REFCLK Frequency (MHz) Indicated By ARS_REF_FREQ	Selected Channel B REFCLK Frequency (MHz) Indicated By ARS_REF_FREQ
000/001/010/011	000/001/010/011	0	RXBCLK_A/(0.5:4)	x	x
000/001/010/011	000/001/010/011	1	RXBCLK_B/(0.5:4)	x	x
110	Not 110	x	153.6 MHz (ppm 0 to RXAP/N)	153.6	x
110	Not 110	x	61.44 MHz (ppm 0 to RXAP/N)	122.88	x
110	Not 110	x	153.6 MHz (ppm 0 to RXAP/N)	307.2	x
110	Not 110	x	61.44 MHz (ppm 0 to RXAP/N)	245.76	x
Not 110	110	x	153.6 MHz (ppm 0 to RXBP/N)	x	153.6
Not 110	110	x	61.44 MHz (ppm 0 to RXBP/N)	x	122.88
Not 110	110	x	153.6 MHz (ppm 0 to RXBP/N)	x	307.2
Not 110	110	x	61.44 MHz (ppm 0 to RXBP/N)	x	245.76
101	000/001/010/011	0	153.6 MHz (ppm 0 to RXAP/N)	153.6	x
101	000/001/010/011	0	61.44 MHz (ppm 0 to RXAP/N)	122.88	x
101	000/001/010/011	0	153.6 MHz (ppm 0 to RXAP/N)	307.2	x
101	000/001/010/011	0	61.44 MHz (ppm 0 to RXAP/N)	245.76	x
101	000/001/010/011	1	RXBCLK_B/(0.5:4)	x	x
000/001/010/011	101	1	153.6 MHz (ppm 0 to RXBP/N)	x	153.6
000/001/010/011	101	1	61.44 MHz (ppm 0 to RXBP/N)	x	122.88
000/001/010/011	101	1	153.6 MHz (ppm 0 to RXBP/N)	x	307.2
000/001/010/011	101	1	61.44 MHz (ppm 0 to RXBP/N)	x	245.76
000/001/010/011	101	0	RXBCLK_A/(0.5:4)	x	x
101	101	0	153.6 MHz (ppm 0 to RXAP/N)	153.6	x
101	101	0	61.44 MHz (ppm 0 to RXAP/N)	122.88	x
101	101	0	153.6 MHz (ppm 0 to RXAP/N)	307.2	x
101	101	0	61.44 MHz (ppm 0 to RXAP/N)	245.76	x
101	101	1	153.6 MHz (ppm 0 to RXBP/N)	x	153.6
101	101	1	61.44 MHz (ppm 0 to RXBP/N)	x	122.88
101	101	1	153.6 MHz (ppm 0 to RXBP/N)	x	307.2
101	101	1	61.44 MHz (ppm 0 to RXBP/N)	x	245.76
111	101/110	x	153.6 MHz (ppm 0 to RXBP/N)	x	153.6
111	101/110	x	61.44 MHz (ppm 0 to RXBP/N)	x	122.88
111	101/110	x	153.6 MHz (ppm 0 to RXBP/N)	x	307.2
111	101/110	x	61.44 MHz (ppm 0 to RXBP/N)	x	245.76
111	000/001/010/011/111	0	RXBCLK_A/(0.5:4)	x	x
111	000/001/010/011/111	1	RXBCLK_B/(0.5:4)	x	x
101/110	111	x	153.6 MHz (ppm 0 to RXAP/N)	153.6	x
101/110	111	x	61.44 MHz (ppm 0 to RXAP/N)	122.88	x
101/110	111	x	153.6 MHz (ppm 0 to RXAP/N)	307.2	x
101/110	111	x	61.44 MHz (ppm 0 to RXAP/N)	245.76	x
000/001/010/011/111	111	0	RXBCLK_A/(0.5:4)	x	x
000/001/010/011/111	111	1	RXBCLK_B/(0.5:4)	x	x

2.24 MDIO Management Interface

The TLK6002 supports the Management Data Input/Output (MDIO) Interface as defined in Clause 22 of the IEEE 802.3 Ethernet specification. The MDIO allows register-based management and control of the serial links. Normal operation of the TLK6002 is possible without use of this interface. However, some features are accessible only through the MDIO.

The MDIO Management Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC). The port address is determined by control pins (see Table 2-10).

Table 2-10. MDIO Related Signals

SIGNAL	TYPE	DESCRIPTION
MDC	LVCMOS 1.5V/1.8V Input VDDO3	**Management Interface Clock.** This clock is used to sample the MDIO signal.
MDIO	LVCMOS 1.5V/1.8V Input/OutputVDDO3	**Management Interface Data.** Bidirectional data line for MDIO Port is sampled on the rising edge of MDC.
		THIS SIGNAL MUST BE EXTERNALLY PULLED UP TO VDDO3. Consult IEEE802.3 Clause 22 for an appropriate resistance value.
PRTAD[4:0]	LVCMOS 1.5V/1.8V Input VDDO2/ VDDO1/ VDDO1/ VDDO1/ VDDO1	**Port Address.** Used to select the Port ID in Clause 22 MDIO mode.
		PRTAD[4:1] selects a block of two sequential Clause 22 port addresses. Each channel is implemented as a different port address, and can be accessed by setting the appropriate port address field within the Clause 22 MDIO transaction.
		PRTAD[0] is not used functionally, but is needed for device testability with other devices in the family of products.
		Channel A responds to port address 0 within the block of two port addresses. Channel B responds to port address 1 within the block of two port addresses.
		It is possible for 16 TLK6002 devices to logically share an MDIO bus.

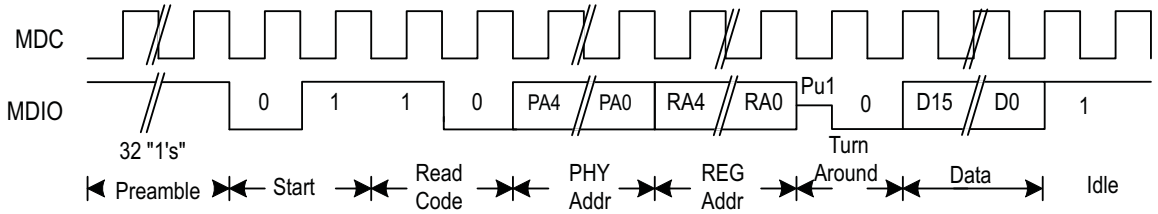
In Clause 22, the top 4 control pins PRTAD[4:1] determine the device port address. In this mode the 2 individual channels in TLK6002 are classified as 2 different ports. So for any PRTAD[4:1] value there will be 2 ports per TLK6002.

TLK6002 will respond if the 4 MSB's of PHY address field on MDIO protocol (PA[4:1]) matches PRTAD[4:1]. The LSB of PHY address field (PA[0]) will determine which channel/port within TLK6002 to respond to.

If PA[0] = 1b0, TLK6002 Channel A will respond.
If PA[0] = 1b1, TLK6002 Channel B will respond.

Write transactions which address an invalid register or device or a read only register will be ignored. Read transactions which address an invalid register will return a 0.

MDIO Protocol Timing:
The Clause 22 timing required to read from the internal registers is shown in Figure 2-9. The Clause 22 timing required to write to the internal registers is shown in Figure 2-10.



(1) Note that the 1 in the Turn Around section is externally pulled up, and driven to Z by TLK6002.

Figure 2-15. CL22 – Management Interface Read Timing

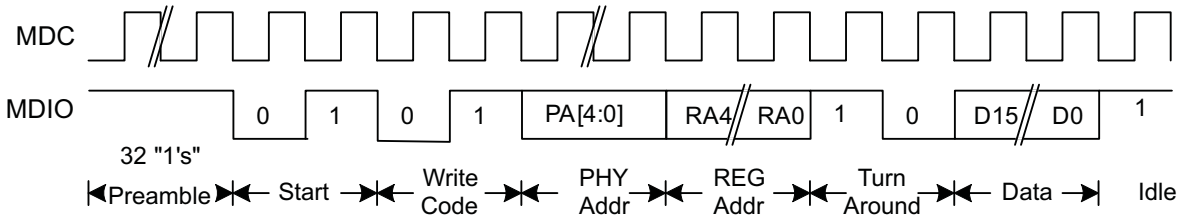


Figure 2-16. CL22 – Management Interface Write Timing

The IEEE 802.3 Clause 22 specification defines many of the registers, and additional registers have been implemented for expanded functionality.

Clause 22 Indirect Addressing:

The TLK6002 Register space is divided into two register groups. One register group can be addressed directly through Clause 22, and one register group can be addressed indirectly through Clause 22. The register group which can be addressed through Clause 22 indirectly is implemented in vendor specific register space (16'h8000 onwards). Due to clause 22 register space limitations, an indirect addressing method is implemented so that this extended register space can be accessed through clause 22. To access this register space (16'h8000 onwards), an address control register (Reg 30, 5'h1E) should be written with the register address followed by a read/write transaction to address data register (Reg 31, 5'h1F) to access the contents of the address specified in address control register.

Figure 2-17 and Figure 2-18 illustrate an example write transaction to Register 16'h8000 using indirect addressing in Clause 22.

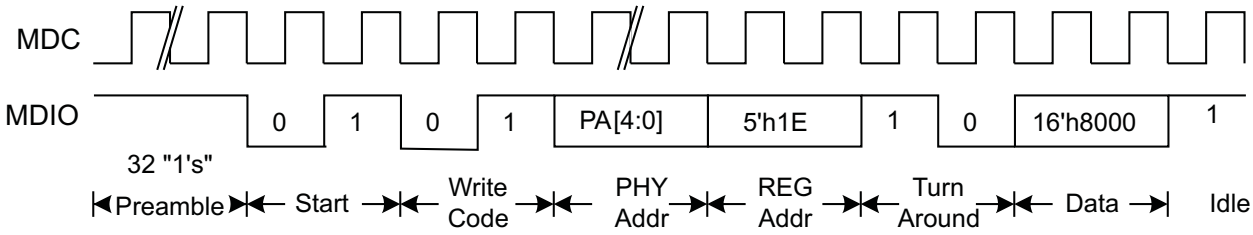


Figure 2-17. CL22 – Indirect Address Method – Address Write

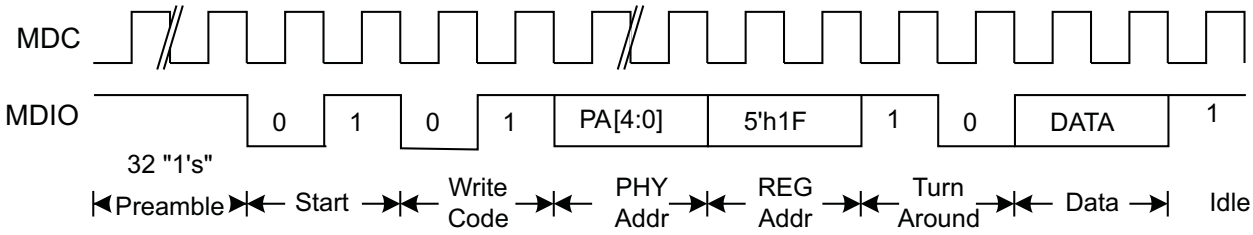


Figure 2-18. CL22 – Indirect Address Method – Data Write

Figure 2-19 and Figure 2-20 illustrate an example read transaction to read contents of Register 16'h8000 using indirect addressing in Clause 22.

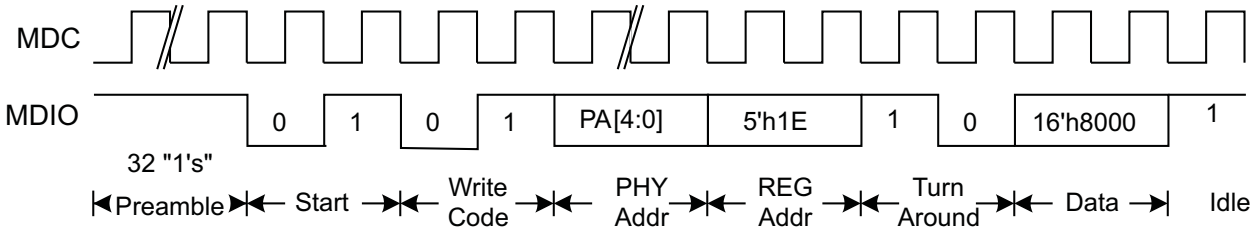


Figure 2-19. CL22 – Indirect Address Method – Address Write

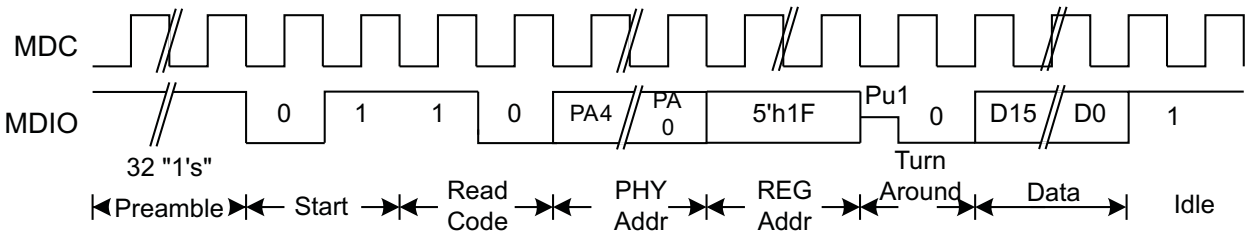


Figure 2-20. CL22 - Indirect Address Method – Data Read

The IEEE 802.3 Clause 22 specification defines many of the registers, and additional registers have been implemented for expanded functionality.

3 PROGRAMMERS REFERENCE

The following registers can be addressed directly through Clause 22. Channel identification is based on PHY (Port) address field. Registers 0x01- 0x0C, 0X14 are per channel basis.

Channel A can be accessed by setting LSB of PHY address to 0.

Channel B can be accessed by setting LSB of PHY address to 1.

Table 3-1. GLOBAL_CONTROL_1

Address: 0x00		Default: 0x0600	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
0.15	GLOBAL_RESET	Global reset (Channel A and B). 0 = Normal operation (Default 1'b0) 1 = Resets TX and RX datapath including MDIO registers. Equivalent to asserting RESET_N.	RW SC(1)
0.11	GLOBAL_WRITE	Global write enable. 0 = Control settings written to Registers 0x01-0x0C, 0x14 are specific to channel addressed (Default 1'b0) 1 = Control settings written to Registers 0x01-0x0C, 0x14 are applied to both Channel A and Channel B regardless of channel addressed	RW
0.10:8	HSTL_IMPED_CLK_DIV[2:0]	HSTL Impedance Control clock divide selection. 000 = Divide by 1 001 = Divide by 2 010 = Divide by 4 011 = Divide by 8 100 = Divide by 16 101 = Divide by 32 110 = Divide by 64 (Default 3'b110) 111 = Divide by 128 This value, in tandem with register bit 0.7, selects the frequency and source of the clock used for dynamic voltage, temperature, and impedance compensation in the HSTL I/O buffers. The division value selected should yield a value less than 10 MHz, and is calculated by dividing the selected REFCLK_0/1_P/N frequency by the value above.	RW
0.7	HSTL_IMPED_CLK_SEL	HSTL Impedance Control reference clock source selection. 0 = Selects channel A reference clock (as selected by REFCLK_A_SEL) as clock reference to HSTL impedance control (Default 1'b0) 1 = Selects channel B reference clock (as selected by REFCLK_B_SEL) as clock reference to HSTL impedance control See register bit 0.10:8 for further details.	RW
0.6	CLKOUT_SEL	Output clock select. Selected RXBCLK_A/B or ARS output clock is sent out on CLK_OUT_P/N pins . Logically OR'ed with CLK_OUT_SEL pin. 0 = Selects Channel A recovered byte clock (RXBCLK_A) as output clock (Default 1'b0) 1 = Selects Channel B recovered byte clock (RXBCLK_B) as output clock. See Figure 1-3	RW
0.5:4	CLKOUT_DIV[1:0]	Output clock divide setting in non-ARS mode.This value is used to divide selected RXBCLK before giving it out onto CLK_OUT_P/N. CLK_OUT_P/N Frequency = (Serial Bit Rate / 10)/(Register 0.5:4 Setting) 00 = Divide by 1 (Default 2'b00) 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8 See Table 2-9 and Figure 1-3	RW

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 3-1. GLOBAL_CONTROL_1 (continued)

Address: 0x00		Default: 0x0600	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
0.2	RETIME_EN	In this mode, serial A input data is sent to both the Parallel A output and Serial B output interface. Serial B input data is sent to both the Parallel B output and Serial A output interface. 0 = Normal functional mode (Default 1'b0) 1 = Enable retime mode Serial A input data rate must match (0 ppm) channel B reference clock. Serial B input data rate must match (0 ppm) channel A reference clock See Figure 2-11	RW
0.1	REFCLK_A_SEL	Channel A Reference clock selection. Logically OR'ed with REFCLK_A_SEL pin. 0 = Selects REFCLK_0_P/N as clock reference to Channel A serdes macro (Default 1'b0) 1 = Selects REFCLK_1_P/N as clock reference to Channel A serdes macro See Figure 1-3	RW
0.0	REFCLK_B_SEL	Channel B Reference clock selection. Logically OR'ed with REFCLK_B_SEL pin. 0 = Selects REFCLK_0_P/N as clock reference to Channel B serdes macro (Default 1'b0) 1 = Selects REFCLK_1_P/N as clock reference to Channel B serdes macro See Figure 1-3	RW

Table 3-2. CHANNEL_CONTROL_1

Address: 0x01		Default: 0x010D	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
1.15	POWERDOWN	Setting this bit high powers down the SERDES datapath channel with exception that MDIO interface stays active. Logically OR'ed with inverse of PD_TRXx_N. 0 = Normal operation (Default 1'b0) 1 = Power Down mode is enabled.	RW
1.10	RESERVED	For TI use only	N/A
1.9:8	LOOP_BANDWIDTH	Serdes PLL Loop Bandwidth settings 00 = Reserved 01 = Applicable when external JC_PLL is NOT used (Default 2'b01) 10 = Applicable when external JC_PLL is used 11 = Reserved	RW
1.7:6	RATE_TX [1:0]	Serdes TX rate settings 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Eighth rate Values written are valid only when RATE_A/B[2:0] pins are set to 3'b100 and ARS is not enabled (10.13:12 = 2'b00) In ARS mode, values written to these bits are not considered to determine serdes TX rate. Instead it is automatically determined by ARS machine. When read, these bits will reflect the final serdes Tx rate values	RW

Table 3-2. CHANNEL_CONTROL_1 (continued)

Address: 0x01		Default: 0x010D	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
1.5:4	RATE_RX [1:0]	Serdes RX rate settings 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Eighth rate Values written are valid only when RATE_A/B[2:0] pins are set to 3'b100 and ARS is not enabled (10.13:12 = 2'b00) In ARS mode, values written to these bits are not considered to determine serdes RX rate. Instead it is automatically determined by ARS machine. When read, these bits will reflect the final serdes Rx rate values	RW
1.3:0	PLL_MULT[3:0]	Serdes PLL multiplier setting (Default 4'b1101). In ARS mode, values written to these bits is not considered to determine serdes PLL multiplier. Instead it is automatically determined by ARS machine and these bits when read will reflect that value. Refer Table 3-3 See Appendix B for more information on PLL multiplier mettings	RW

Table 3-3. PLL Multiplier Control

1[3:0]		1[3:0]	
VALUE	**PLL MULTIPLIER FACTOR**	**VALUE**	**PLL MULTIPLIER FACTOR**
0000	Reserved	1000	12x
0001	Reserved	1001	Reserved
0010	4x	1010	15x
0011	5x	1011	16x
0100	6x	1100	16.5x
0101	8x	1101	20x
0110	8.25x	1110	25x
0111	10x	1111	Reserved

Table 3-4. CHANNEL_CONTROL_2

Address: 0x02		Default: 0x000A	
Bit(s)	**Name**	**Description**	**Access**
2.12:8	TWPOST1[4:0]	Adjacent post cursor Tap weight. Selects TAP settings for TX waveform. (Default 5'b00000) Refer Table 3-5	RW
2.7:4	TWPRE[3:0]	Pre cursor Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000) Refer Table 3-6	RW
2.3:0	SWING[3:0]	Transmitter Output swing control for Serdes. (Default 4'b1010) Refer Table 3-7	RW

Table 3-5. Post-Cursor Transmit Tap Weights

2[12:8]		2[12:8]	
VALUE	**TAP WEIGHT (%)**	**VALUE**	**TAP WEIGHT (%)**
00000	0	10000	0
00001	+2.5	10001	–2.5
00010	+5.0	10010	–5.0
00011	+7.5	10011	–7.5
00100	+10.0	10100	–10.0
00101	+12.5	10101	–12.5
00110	+15.0	10110	–15.0
00111	+17.5	10111	–17.5
01000	+20.0	11000	–20.0
01001	+22.5	11001	–22.5
01010	+25.0	11010	–25.0
01011	+27.5	11011	–27.5
01100	+30.0	11100	–30.0
01101	+32.5	11101	–32.5
01110	+35.0	11110	–35.0
01111	+37.5	11111	–37.5

Table 3-6. Pre-Cursor Transmit Tap Weights

2[7:4]		2[7:4]	
VALUE	**TAP WEIGHT (%)**	**VALUE**	**TAP WEIGHT (%)**
0000	0	1000	0
0001	+2.5	1001	–2.5
0010	+5.0	1010	–5.0
0011	+7.5	1011	–7.5
0100	+10.0	1100	–10.0
0101	+12.5	1101	–12.5
0110	+15.0	1110	–15.0
0111	+17.5	1111	–17.5

Table 3-7. AC Mode Output Swing Control

VALUE 2[3:0]	AC MODETYPICAL AMPLITUDE (mVdfpp)
0000	126
0001	215
0010	303
0011	395
0100	478
0101	572
0110	662
0111	756
1000	839
1001	932
1010	1020
1011	1110
1100	1190
1101	1280
1110	1360
1111	1450

Table 3-8. CHANNEL_CONTROL_3

Address: 0x03		Default: 0x0180	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
3.12:11	CH_SYNC_HYSTERESIS [1:0]	Valid only when comma detection (channel synchronization) is enabled. 00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the unsynchronized state (Default 2'b00) 01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to unsync 10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync 11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync	RW
3.10	TX_SWAP_SEL	0 = Selects same channel Tx parallel interface input data as core input data for that channel (Default 1'b0) 1 = Selects partner channel Tx parallel interface input data as core input data for that channel See Figure 1-4	RW
3.9	RX_SWAP_SEL	0 = Selects same channel deserialized input data to be sent out the Rx parallel output interface (Default 1'b0) 1 = Selects partner channel deserialized input data to be sent out the Rx parallel output interface See Figure 1-5	RW
3.8	RXCLK_OUT_SEL	Parallel output clock (RXCLK_x) selection When RX_SWAP_SEL (3.9) is 1'b0 0 = Selects respective channel SERDES TXBCLK clock 1 = Selects respective channel SERDES RXBCLK clock (Default 1'b1) When RX_SWAP_SEL (3.9) is 1'b1 0 = Selects partner channel SERDES TXBCLK clock 1 = Selects partner channel SERDES RXBCLK clock (Default 1'b1) See Figure 1-5	RW

Table 3-8. CHANNEL_CONTROL_3 (continued)

Address: 0x03		Default: 0x0180	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
3.7	COMMA_ENABLE	0 = Disables comma detection 1 = Enables comma detection (Default 1'b1) Comma detection automatically enabled during CRPAT verification.	RW
3.6	DDR_ENABLE	0 = Enables SDR data mode on parallel Transmit and Receive directions (data is clocked only on rising edge or only on falling edge) (Default 1'b0) 1 = Enables DDR data mode on parallel Transmit and Receive directions (data clocked on both rising and falling edge)	RW
3.5	TX_SYMBOL_ORDER	0 = TDx_[19:10] symbol is serialized before TDx_[9:0]. (Default 1'b0) 1 = TDx_[9:0] symbol is serialized before TDx_[19:10].	RW
3.4	RX_SYMBOL_ORDER	0 = RDx_[19:10] symbol is deserialized before RDx_[9:0] symbol. (Default 1'b0) 1 = RDx_[9:0] symbol is deserialized before RDx_[19:10].	RW
3.3	ENCODE_ENABLE	Encoder enable control. Logically OR'ed with CODE*_EN pin. 0 = 8B/10B encode function is disabled (Default 1'b0) 1 = 8B/10B encode function is enabled Encoder automatically enabled during CRPAT test pattern generation.	RW
3.2	DECODE_ENABLE	Decoder enable control. Logically OR'ed with CODE*_EN pin. 0 = 8B/10B decode function is disabled (Default 1'b0) 1 = 8B/10B decode function is enabled Decoder automatically enabled during CRPAT verification.	RW
3.1	TX_EDGE_MODE	Transmit parallel input interface mode select. (Default 1'b0) When channel is in DDR mode 0 = Source centered timing on transmit parallel interface. Data is sampled on both rising and falling clock edges. 1 = Source aligned timing on transmit parallel interface. Data is aligned with both rising and falling clock edges, and a sampling point is created internal to TLK6002 . When channel is in SDR mode 0 = Falling edge align mode. Incoming data is aligned to falling edge of parallel input clock. Internally data is sampled at the rising edge of the clock 1 = Rising edge align mode. Incoming parallel data is aligned to rising edge of parallel input clock. Internally data is sampled at the falling edge of the clock.	RW
3.0	RX_EDGE_MODE	Receive Parallel output interface mode select. (Default 1'b0) When channel is in DDR mode: 0 = Source centered timing on receive parallel interface. Data changing is offset from the rising and falling clock edge per the HSTL Timing specification section, and is easily sampled by external devices. 1 = Source aligned timing on receive parallel interface. Data changes at clock edge, and a sampling point must be created by external devices. When channel is in SDR mode: 0 = Falling edge align mode. Outgoing parallel data is aligned to the falling edge of the parallel output clock, and is sampled on the rising edge by external devices. 1 = Rising edge align mode. Outgoing parallel data is aligned to the rising edge of the parallel output clock, and is sampled on the falling edge by external devices.	RW

Table 3-9. CHANNEL_CONTROL_4

Address: 0x04		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
4.3	DATAPATH_RESET	Channel datapath reset control. Required once the desired functional mode is configured. 0 = Normal operation. (Default 1'b0) 1 = Resets channel logic excluding MDIO registers. (Resets both Tx and Rx datapath)	RW SC(1)
4.2	TXFIFO_RESET	Transmit FIFO reset control 0 = Normal operation. (Default 1'b0) 1 = Resets transmit datapath FIFO.	
4.1	RXFIFO_RESET	Receive FIFO reset control 0 = Normal operation. (Default 1'b0) 1 = Resets receive datapath FIFO.	

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 3-10. CHANNEL_STATUS_1

Address: 0x05		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
5.14	AZ_DONE	Auto zero complete indicator. When high, indicates auto zero calibration is complete	RO/LL
5.13	AGC_LOCKED	Adaptive gain control loop lock indicator. When high, indicates AGC loop is in locked state	
5.12	TP_ STATUS	Test Pattern status for test pattern selected in 7.10:8 . 0 = Alignment has not achieved 1 = Alignment has been determined and correct pattern has been received. Any bit errors received are reflected in ERROR_COUNTER register (0x0E)	RO
5.11	ARS_PLL_LOCK_ERROR	ARS PLL Lock error indicator. Valid only when ARS function is enabled. When high, indicates ARS did not detect PLL lock within the time specified through ARS_INTERVAL[20:0] (11.4:0,12.15:0).	RO/LH
5.10	ARS_LOCKED	ARS lock indicator. Valid only when ARS function is enabled. When high, indicates ARS has determined incoming serial data rate.	RO/LL
5.9	ENCODE_INVALID	Valid in 16 bit (SDR/DDR) mode (encoder enabled) and during CRPAT test pattern generation. When high, indicates encoder received an invalid control word.	RO/LH
5.8	DECODE_INVALID	Valid in 16 bit (SDR/DDR) mode (decoder enabled) and during CRPAT test pattern verification. When high, indicates decoder received an invalid code word, or a 8b/10b disparity error. In functional mode, number of DECODE_INVALID errors are reflected in ERROR_COUNTER register (0x0E)	RO/LH
5.7	TX_FIFO_UNDERFLOW	When high, indicates underflow has occurred in the transmit datapath FIFO.	RO/LH
5.6	TX_FIFO_OVERFLOW	When high, indicates overflow has occurred in the transmit datapath FIFO.	RO/LH
5.5	RX_FIFO_UNDERFLOW	When high, indicates underflow has occurred in the receive datapath FIFO.	RO/LH
5.4	RX_FIFO_OVERFLOW	When high, indicates overflow has occurred in the receive datapath FIFO.	RO/LH
5.3	GPI1	GPI1 status Indicator. Reflects GPI1 input signal status.	RO
5.2	LOS	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on serial receive inputs	RO/LH
5.1	CHANNEL_SYNC	Channel synchronization status indicator. Valid only when comma detection is enabled When high, indicates channel synchronization has achieved	RO/LL
5.0	PLL_LOCK	Serdes PLL lock indicator When high, indicates Serdes PLL is locked to the selected incoming REFCLK_0/1_P/N	RO/LL

Table 3-11. OVERRIDE_CONTROL

<table>
<tr><th colspan="2">Address: 0x06</th><th colspan="2">Default: 0xC000</th><th></th></tr>
<tr><th>BIT(s)</th><th>NAME</th><th colspan="2">DESCRIPTION</th><th>ACCESS</th></tr>
<tr><td>6.15</td><td>RXCLK_OUT_EN</td><td colspan="2">0 = Holds parallel output clock RXCLK_x output fixed at zero.
1 = Allows RXCLK_x output to toggle normally. (Default 1’b1)</td><td>RW</td></tr>
<tr><td>6.14:12</td><td>TX_FIFO_DEPTH[2:0]</td><td colspan="2">TX FIFO Latency Control (Default 3’b100) This selection allows TX FIFO crash immunity to be traded off against datapath latency. Selecting a large latency allows for the most dynamic phase variation between TXCLK_A/B and the selected SERDES channel reference clock (REFCLK_0/1_P/N). Careful consideration should be made in selecting this value based on the anticipated phase movement between TXCLK_A/B and selected REFCLK_0/1_P/N during system operation to avoid unwanted reoccurring transmit FIFO collision.
<table>
<tr><th>TX_FIFO_DEPTH [2:0]</th><th>TXCLK_A/B and selected REFCLK_0/1_P/N. Relative Phase Movement Allowed (Serial Bit Times)</th><th>Appendix D Datapath Latency Maximum Value (Serial Bit Times)</th></tr>
<tr><td>000</td><td>±4</td><td>Same</td></tr>
<tr><td>001</td><td>±14</td><td>Same +20</td></tr>
<tr><td>010</td><td>±34</td><td>Same +60</td></tr>
<tr><td>011</td><td>±54</td><td>Same +110</td></tr>
<tr><td>1xx (Auto Selection)</td><td>Full Rate: Same as 011
Half Rate: Same as 010
Quarter Rate: Same as 001
Eighth Rate: Same as 000</td><td>Consistent with above four selections.</td></tr>
</table></td><td>RW</td></tr>
<tr><td>6.11</td><td>GPI_OVERLAY</td><td colspan="2">0 = LOSx pin does not reflect GPI1 input signal status (Default 1’b0)
1 = Allows inverse value of GPI1 input signal to be reflected on LOSx pin</td><td>RW</td></tr>
<tr><td>6.10</td><td>LOS_OVERLAY</td><td colspan="2">0 = LOSx pin does not reflect Serdes Rx Loss of signal condition (Default 1’b0)
1 = Allows Serdes Rx Loss of signal condition to be reflected on LOSx pin</td><td>RW</td></tr>
<tr><td>6.9</td><td>CH_SYNC_OVERLAY</td><td colspan="2">0 = LOSx pin does not reflect loss of channel synchronization status (Default 1’b0)
1 = Allows channel loss of synchronization to be reflected on LOSx pin</td><td>RW</td></tr>
<tr><td>6.8</td><td>PLL_LOCK_OVERLAY</td><td colspan="2">0 = LOSx pin does not reflect loss of PLL lock status (Default 1’b0)
1 = Allows loss of PLL lock status to be reflected on LOSx pin</td><td>RW</td></tr>
<tr><td>6.7</td><td>RX_CHAR_CTRL_GPI1</td><td colspan="2">Receive data replacement control when GPI1 input is low
0 = Data passed through as received (Default 1’b0)
1 = Data replaced with K30.7 (when decoder is enabled) or all 0’s (when decoder is disabled)</td><td>RW</td></tr>
<tr><td>6.6</td><td>RX_CHAR_CTRL_LOS</td><td colspan="2">Receive data replacement control during Loss of signal condition
0 = Data passed through as received (Default 1’b0)
1 = Data replaced with K30.7 (when decoder is enabled) or all 0’s (when decoder is disabled)</td><td>RW</td></tr>
<tr><td>6.5</td><td>RX_CHAR_CTRL_CH_SYNC</td><td colspan="2">Receive data replacement control during Loss of synchronization condition
0 = Data passed through as received (Default 1’b0)
1 = Data replaced with K30.7 (when decoder is enabled) or all 0’s (when decoder is disabled)</td><td>RW</td></tr>
<tr><td>6.4</td><td>RX_CHAR_CTRL_PLL_LOCK</td><td colspan="2">Receive data replacement control during Loss of PLL Lock condition
0 = Data passed through as received (Default 1’b0)
1 = Data replaced with K30.7 (when decoder is enabled) or all 0’s (when decoder is disabled)</td><td>RW</td></tr>
<tr><td>6.3</td><td>INVALID_CODE_OVERLAY</td><td colspan="2">0 = LOSx pin does not reflect invalid code word error (Default 1’b0)
1 = Allows invalid code word error to be reflected on LOSx pin</td><td>RW</td></tr>
<tr><td>6.2</td><td>HSTL_SLEW_RATE</td><td colspan="2">Slew Rate setting for RX parallel outputs
0 = No slew control (fastest edge) (Default 1’b0)
1 = 33% slower slew control</td><td>RW</td></tr>
<tr><td>6.1:0</td><td>HSTL_TERM[1:0]</td><td colspan="2">Parallel Input Termination setting for TX parallel inputs
00 = Termination disable (High Impedance) (Default 2’b00)
01 = Half termination strength (200 Ω to VHSTL and GND) – Thevenin equivalent of 100 Ω to (VDDQA/B)/2
1x = Full termination strength (100 Ω to VHSTL and GND) – Thevenin equivalent of 50 Ω to (VDDQA/B)/2.</td><td>RW</td></tr>
</table>

Table 3-12. LOOPBACK_TP_CONTROL

Address: 0x07		Default: 0x0700	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
7.15:14	RESERVED	For TI use only	N/A
7.13	TP_GEN_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits 7.10:8	RW
7.12	TP_VERIFY_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern verification selected by bits 7.10:8	RW
7.10:8	TEST_PATTERN_SEL[2:0]	Test Pattern Selection 000 = Reserved 001 = Reserved 010 = Reserved 011 = CRPAT Long (Supported only in half/quarter/eighth rate modes). 100 = CRPAT Short (Supported only in half/quarter/eighth rate modes). 101 = 2^7 - 1 PRBS pattern 110 = 2^{23} - 1 PRBS pattern 111 = 2^{31} - 1 PRBS pattern (Default 3'b111)	RW
7.7	AGCLOCK_OVERLAY	0 = LOSx pin does not reflect AGC unlock status (Default 1'b0) 1 = Allows AGC unlock status to be reflected on LOSx pin	RW
7.6	AZDONE_OVERLAY	0 = LOSx pin does not reflect auto zero calibration not done status (Default 1'b0) 1 = Allows auto zero calibration not done status to be reflected on LOSx pin	RW
7.5	RX_CHAR_CTRL_AGCLOCK	Receive data replacement control during AGC unlock condition 0 = Data passed through as received (Default 1'b0) 1 = Data replaced with K30.7 (when decoder is enabled) or all 0's (when decoder is disabled)	RW
7.4	RX_CHAR_CTRL_AZDONE	Receive data replacement control during auto zero calibration not done condition 0 = Data passed through as received (Default 1'b0) 1 = Data replaced with K30.7 (when decoder is enabled) or all 0's (when decoder is disabled)	RW
7.3	DEEP_REMOTE_LPBK	In this mode, serial input data traverses entire Rx datapath just before parallel output drivers and is returned through entire Tx datapath and to the channel's serial output. The serial input data will also be available at the parallel output port. Serial input data rate must match (0 ppm) reference clock. 0 = Normal functional mode (Default 1'b0) 1 = Enable deep remote loopback mode See Figure 2-10	RW
7.2	SHALLOW_REMOTE_LPBK	In this mode, serial input following decoder is fed back to the channel's encoder input and to the serial output. The serial input data will also be available at the parallel output port. Serial input data rate must match (0 ppm) reference clock 0 = Normal functional mode (Default 1'b0) 1 = Enable shallow remote loopback mode See Figure 2-10	RW
7.1	DEEP_LOCAL_LPBK	In this mode, parallel input is looped after serializer and fed back to the channel's parallel output. The parallel input data is not available at the TX serial output. Note: SWING[3:0] must be set to 4'b0000 in this mode. 0 = Normal functional mode (Default 1'b0) 1 = Enable deep local loopback mode See figure Figure 2-9 Note that AZDONE must be asserted before asserting DEEP_LOCAL_LPBK. Also note that AGCLOCK is not valid during DEEP_LOCAL_LPBK.	RW
7.0	SHALLOW_LOCAL_LPBK	In this mode, parallel input after the encoder and before the serializer is fed back to the channel's parallel output. The parallel input data will also be serialized and available at the TX serial port 0 = Normal functional mode (Default 1'b0) 1 = Enable shallow local loopback mode See Figure 2-9	RW

Table 3-13. SERDES_CONTROL_1

Address: 0x08		Default: 0x3D4C	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
8.14:12	EQPRE[2:0]	Serdes Rx precursor equalizer selection 000 = 1/9 cursor amplitude 001 = 3/9 cursor amplitude 010 = 5/9 cursor amplitude 011 = 7/9 cursor amplitude (Default 3'b011) 100 = 9/9 cursor amplitude 101 = 11/9 cursor amplitude 110 = 13/9 cursor amplitude 111 = Disable	RW
8.11:10	CDRTHR[1:0]	Clock data recovery algorithm threshold selection 00 = Four vote threshold 01 = Eight vote threshold 10 = Sixteen vote threshold 11 = Thirty two vote threshold (Default 2'b11)	RW
8.9:8	CDRFMULT[1:0]	Clock data recovery algorithm frequency multiplication selection 00 = First order. Frequency offset tracking disabled 01 = Second order. 1x mode (Default 2'b01) 10 = Second order. 2x mode 11 = Reserved	RW
8.7:6	AGCCTRL[1:0]	Adaptive gain control loop 00 = Attenuator will not change after lock has been achieved, even if AGC becomes unlocked 01 = Attenuator will not change when in lock state, but could change when AGC becomes unlocked (Default 2'b01) 10 = Force the attenuator off. 11 = Force the attenuator on	RW
8.5:4	AZCAL[1:0]	Auto zero calibration. 00 = Auto zero calibration initiated when receiver is enabled (Default 2'b00) 01 = Auto zero calibration disabled 10 = Forced with automatic update. 11 = Forced without automatic update	RW
8.3	TX_PMA_BIT_ORDER	Determines whether LSB or MSB of the parallel inputs to be sent out first on serial transmit pins. 0 = TDx[19] or TDx[9] (MSB) is serially transmitted first 1 = TDx[10] or TDx[0] (LSB) is serially transmitted first (Default 1'b1)	RW
8.2	RX_PMA_BIT_ORDER	Determines whether serially received first bit to be sent out on LSB or MSB of the parallel outputs. 0 = RDx[19] or RDx[9] (MSB) is serially received first 1 = RDx[10] or RDx[0] (LSB) is serially received first (Default 1'b1)	RW
8.1	TX_INVPAIR	Transmitter polarity. 0 = Normal polarity. TXxP considered positive data and TXxN considered negative data (Default 1'b0) 1 = Inverted polarity. TXxP considered negative data and TXxN considered positive data	RW
8.0	RX_INVPAIR	Receiver polarity. 0 = Normal polarity. RXxP considered positive data. RXxN considered negative data (Default 1'b0) 1 = Inverted polarity. RXxP considered negative data. RXxN considered positive data	RW

Table 3-14. SCRAMBLER_CONTROL

Address: 0x09		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
9.15	TX_SCRAMBLER_EN	0 = Disables scrambler on the transmit datapath (Default 1'b0) 1 = Enables scrambler on the transmit datapath	RW
9.14:8	TX _SCRAMBLER_SEED[6:0]	7 bit scrambler seed used when TX scrambler is enabled. (Default 7'b0000000)	RW
9.7	RX_DESCRAMBLER_EN	0 = Disables De-scrambler on the receive datapath (Default 1'b0) 1 = Enables De-scrambler on the receive datapath	RW
9.6:0	RX_DESCRAMBLER_SEED[6:0]	7 bit De-scrambler seed used when RX De-scrambler is enabled. (Default 7'b0000000)	RW

Table 3-15. ARS_CONTROL_1

Address: 0x0A		Default: 0x0800	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
10.15	ARS_RX_CLK_EN	Valid only when ARS function is enabled. 0 = Holds parallel output clock RXCLK_x output fixed at zero until serial data rate is determined by the ARS. (Default 1'b0) 1 = Allows RXCLK_x output to toggle normally.	RW
10.14	ARS_ LOCK_OVERLAY	Valid only when ARS function is enabled. 0 = LOSx pin does not reflect ARS loss of lock status (Default 1'b0) 1 = Allows ARS loss of lock status to be reflected on LOSx pin	RW
10.13:12	ARS_ EN[1:0]	ARS enable software control. Applicable when RATE_x[2:0] pins are set to 3'b100. 00 = Serdes settings are determined by MDIO (Default 2'b00) 01 = Enable ARS function in respective channel. Serdes settings for respective channel are determined by ARS in the same channel. Refer RATE_x[2:0] 3'b101 setting for more information. 10 = Enable ARS function in respective channel. Serdes settings for respective channel are determined by ARS in the same channel. Refer RATE_x[2:0] 3'b110 setting for more information. 11 = Enable ARS function in respective channel as slave mode. If ARS is enabled in partner channel, serdes settings in this channel are determined by ARS in partner channel. If ARS is not enabled in partner channel, serdes settings in this channel are determined by MDIO. Refer RATE_x[2:0] 3'b111 setting for more information.	RW
10.11	ARS_TX_MDIO_GATE	Valid only when ARS_TX_DATAPATH_OVERRIDE (10.10) is set 0 = When ARS successfully determines incoming serial data rate, TX_FIFO is automatically reset and parallel data is serialized and sent through serial output pins. 1 = When ARS successfully determines incoming serial data rate, TX FIFO needs to be manually reset by writing to register bit 4.2 to enable proper serialization of the parallel data. (Default 1'b1)	RW
10.10	ARS_TX_DATAPATH_OVERRIDE	Applicable during serial data rate determination by ARS 0 = Transmit parallel input data is serialized as received and sent through serial output pins. (Default 1'b0) 1 = 10 bit data specified in ARS_TX_DATA (10.9:0) is serialized and sent through serial output pins.	RW
10.9:0	ARS_TX_DATA[9:0]	10 bit data to be serialized during serial rate determination by ARS. If TX_PMA_BIT_ORDER (8.3) is set, ARS_TX_DATA [9] is serially transmitted first else ARS_TX_DATA [0] is serially transmitted first.	RW

Table 3-16. ARS_CONTROL_2

Address: 0x0B		Default: 0x7FFF	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
11.15:14	ARS_REF_FREQ[1:0]	Input reference clock frequency selection in ARS mode. 00 = If input reference clock frequency is 122.88 MHz. 01 = If input reference clock frequency is 153.60 MHz. (Default 2'b01) 10 = Reserved 11 = If input reference clock frequency is 307.20 MHz.	RW
11.13:6	ARS_SBR_ENABLE[7:0]	Control to enable rate determination through ARS for each of the 8 supported bit rates. ARS_SBR_ENABLE[7] for the highest serial bit rate and ARS_SBR_ENABLE[0] for the lowest serial bit rate. Refer Table 2-6 for supported serial bit rates.	RW
11.5	RESERVED	For TI use only	N/A
11.4:0	ARS_INTERVAL[20:16]	5 MSB's of 21 bit wide counter defined in terms of number of REFCLK cycles to determine amount of time that ARS state machine needs to stay in a particular setting to achieve rate determination. Wait time is calculated as ARS_INTERVAL[20:0] × 1024 REFCLK periods. If ARS state machine does not achieve rate determination within the wait time specified by this counter, ARS state machine will move into next lower serial rate setting to achieve rate determination.	RW

Table 3-17. ARS_CONTROL_3

Address: 0x0C		Default: 0xFFFF	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
12.15:0	ARS_INTERVAL[15:0]	16 LSB's of 21 bit wide counter defined in terms of number of REFCLK cycles to determine amount of time that ARS state machine needs to stay in a particular setting to achieve rate determination. Wait time is calculated as ARS_INTERVAL[20:0] × 1024 REFCLK periods. If ARS state machine does not achieve rate determination within the wait time specified by this counter, ARS state machine will move into next lowest serial rate setting to achieve rate determination.	RW

Table 3-18. ARS_CONTROL_4

Address: 0x0D		Default: 0x3000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
13.15	RESERVED	For TI use only	N/A
13.14	RESERVED	For TI use only	
13.13	RESERVED	For TI use only	
13.12	RESERVED	For TI use only	
13.11:0	RESERVED	For TI use only	

Table 3-19. ERROR_COUNTER

Address: 0x0E		Default: 0xFFFD	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
14.15:0	ERROR_COUNTER[15:0]	In functional mode if 8b/10b decoder is enabled, this counter reflects number of invalid code words (includes disparity errors) received by decoder. In test pattern verification mode (7.12 = 1'b1), this counter reflects error count for the test pattern selected through 7.10:8 When PRBS_EN pin is set, this counter reflects error count for selected PRBS pattern. Counter value cleared to 16'h0000 when read.	COR

Table 3-20. TI_RESERVED_CONTROL STATUS

Address: 0x0F		Default: 0x0205	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
15.14	RESERVED	For TI use only	N/A
15.13	RESERVED	For TI use only	
15.12	RESERVED	For TI use only	
15.10	RESERVED	For TI use only	
15.9	RESERVED	For TI use only	
15.8	RESERVED	For TI use only	
15.6	RESERVED	For TI use only	
15.5	RESERVED	For TI use only	
15.4	RESERVED	For TI use only	
15.2	RESERVED	For TI use only	
15.1	RESERVED	For TI use only	
15.0	RESERVED	For TI use only	

Table 3-21. LATENCY_MEASURE_CONTROL

Address: 0x10		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
16.10	RESERVED	For TI use only	N/A
16.9	RESERVED	For TI use only	
16.8	RESERVED	For TI use only	
16.5:4	LATENCY_MEAS_CLK_DIV[1:0]	Latency measurement clock divide control. Valid only when bit 16.2 is 0. Divides clock to needed resolution. Higher the divide value, lesser the latency measurement resolution 00 = Divide by 1 (Default 2'b00) (Most Accurate Measurement) 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8 (Longest Measurement Capability) See Table 2-6	RW
16.2	LATENCY_MEAS_CLK_SEL	Latency measurement clock selection. 0 = Selects clock listed in Table 2-6. Bits 16.5:4 can be used to divide this clock to achieve needed resolution. (Default 1'b0) 1 = Selects respective channel recovered byte clock (Frequency = Serial bit rate/ 10).	RW
16.1	LATENCY_MEAS_EN	Latency measurement enable 0 = Disable Latency measurement (Default 'b0) 1 = Enable Latency measurement	RW
16.0	LATENCY_MEAS_CH_SEL	Latency measurement channel selection 0 = Selects Latency measurement for channel A (Default 'b0) 1 = Selects Latency measurement for channel B	RW

Table 3-22. LATENCY_COUNTER_2

Address: 0x11		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
17.15	LATENCY_MEAS_TX_COMMA	Comma indication for the current latency measurement. Cleared when Register 0x12 is read 0 = Indicates Latency measurement detected comma on TXD[19:10] 1 = Indicates Latency measurement detected comma on TXD[9:0]	RO/LH(1)
17.14	LATENCY_MEAS_RX_COMMA	Comma indication for the current latency measurement. Cleared when Register 0x12 is read 0 = Indicates Latency measurement detected comma on RXD[19:10] 1 = Indicates Latency measurement detected comma on RXD[9:0]	
17.4	LATENCY_ MEAS_READY	Latency measurement ready indicator 0 = Indicates latency measurement not complete. 1 = Indicates latency measurement is complete and value in latency measurement counter (LATENCY_MEAS_COUNT[19:0]) is ready to be read.	
17.3:0	LATENCY_MEAS_COUNT[19:16]	Bits[19:16] of 20 bit wide latency measurement counter. Latency measurement counter value represents the latency in number of clock cycles. This counter will return 20'h00000 if it is read before rx comma is received. If latency is more than 20'hFFFFF clock cycles then this counter returns 20'hFFFFF.	COR(1)

(1) User has to make sure Register 0x11 has to be read first before reading Register 0x12. Latency measurement counter value resets to 20'h00000 when Register 0x12 is read. Comma indication (17.15 and 17.14) and count valid (17.4) bits are also cleared when Register 0x12 is read.

Table 3-23. LATENCY_COUNTER_1

Address: 0x12		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
18.15:0	LATENCY_MEAS_COUNT[15:0]	Bits[15:0] of 20 bit wide latency measurement counter.	COR(1)

(1) User has to make sure Register 0x11 has to be read first before reading Register 0x12. Latency measurement counter value resets to 20'h00000 when Register 0x12 is read. Comma indication (17.15 and 17.14) and count valid (17.4) bits are also cleared when Register 0x12 is read.

Table 3-24. TI_RESERVED_CONTROL_1

Address: 0x13		Default: 0x0200	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
19.12	RESERVED	For TI use only	N/A
19.9	RESERVED	For TI use only	
19.8	RESERVED	For TI use only	
19.7	RESERVED	For TI use only	
19.3	RESERVED	For TI use only	
19.0	RESERVED	For TI use only	

Table 3-25. SERDES_CONTROL_2

Address: 0x14		Default: 0x7C4F	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
20.15	RESERVED	For TI use only	N/A
20.14	RESERVED	For TI use only	
20.13	RESERVED	For TI use only	
20.12	RESERVED	For TI use only	
20.11	RESERVED	For TI use only	
20.10	RESERVED	For TI use only	
20.9	RESERVED	For TI use only	
20.8	RESERVED	For TI use only	
20.7	RESERVED	For TI use only	
20.6	RESERVED	For TI use only	
20.5:4	RESERVED	For TI use only	
20.3	RESERVED	For TI use only	
20.2	ENRX	Serdes receiver enable control. Serdes receiver is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables serdes receiver 1 = Enables serdes receiver (Default 1'b1)	RW
20.1	ENTX	Serdes transmitter enable control. Serdes transmitter is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables serdes transmitter 1 = Enables serdes transmitter (Default 1'b1)	RW
20.0	ENPLL	Serdes PLL enable control. Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables PLL in serdes 1 = Enables PLL in serdes (Default 1'b1)	RW

Table 3-26. TI_RESERVED_CONTROL_3

Address: 0x15		Default: 0x0023	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
21.12	RESERVED	For TI use only	N/A
21.11	RESERVED	For TI use only	
21.10	RESERVED	For TI use only	
21:9	RESERVED	For TI use only	
21.8	RESERVED	For TI use only	
21.7	RESERVED	For TI use only	
21.6:4	RESERVED	For TI use only	
21.2:0	RESERVED	For TI use only	

Table 3-27. TI_RESERVED_CONTROL_4

Address: 0x16		Default: 0x0023	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
22.12	RESERVED	For TI use only	N/A
22.11	RESERVED	For TI use only	
22.10	RESERVED	For TI use only	
22.9	RESERVED	For TI use only	
22.8	RESERVED	For TI use only	
22.7	RESERVED	For TI use only	
22.6:4	RESERVED	For TI use only	
22.2:0	RESERVED	For TI use only	

Table 3-28. TI_RESERVED_CONTROL_5

Address: 0x17		Default: 0x0008	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
23.15	RESERVED	For TI use only	N/A
23.14	RESERVED	For TI use only	
23.13:8	RESERVED	For TI use only	
23.7:5	RESERVED	For TI use only	
23.3	RESERVED	For TI use only	

Table 3-29. TI_RESERVED_STATUS_1

Address: 0x18		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
24.13	RESERVED	For TI use only	N/A
24.12	RESERVED	For TI use only	
24.9:4	RESERVED	For TI use only	
24.3	RESERVED	For TI use only	
24.2	RESERVED	For TI use only	
24.1	RESERVED	For TI use only	
24.0	RESERVED	For TI use only	

Table 3-30. TI_RESERVED_CONTROL_6

Address: 0x19		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
25.6	RESERVED	For TI use only	N/A
25.5:4	RESERVED	For TI use only	
25.3:0	RESERVED	For TI use only	

Table 3-31. TI_RESERVED_CONTROL_7

Address: 0x1A		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
26.15:0	RESERVED	For TI use only	N/A

Table 3-32. TI_RESERVED_STATUS_2

Address: 0x1B		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
27.15:0	RESERVED	For TI use only	N/A

Table 3-33. TI_CONTROL_8

Address: 0x1C		Default: 0x0001	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
28.14	CLKOUT_OBS_EN	Enable CLK_OUT_P/N output 0 = Disable clock out observe mode (Default 1'b0) 1 = Enable clock out observe mode	RW
28.13	RESERVED	For TI use only	N/A
28.12	RESERVED	For TI use only	
28.8	RESERVED	For TI use only	
28.7:4	RESERVED	For TI use only	
28.0	RESERVED	For TI use only	

Table 3-34. TI_RESERVED_STATUS_3

Address: 0x1D		Default: 0x0200	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
29.9	RESERVED	For TI use only	N/A
29.8:4	RESERVED	For TI use only	
29.3:0	RESERVED	For TI use only	

Table 3-35. TI_RESERVED_CONTROL_9

Address: 0x1E		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
30.15:0	RESERVED	For TI use only	N/A

Table 3-36. TI_RESERVED_CONTROL_10

Address: 0x1F		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
31.15:0	RESERVED	For TI use only	N/A

Table 3-37. TI_RESERVED_STATUS_4

Address: 0x8000		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
32768.15:0	RESERVED	For TI use only	N/A

Table 3-38. TI_RESERVED_STATUS_5

Address: 0x8001		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
32769.15:0	RESERVED	For TI use only	N/A

Table 3-39. TI_RESERVED_STATUS_6

Address: 0x8002		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
32770.15:0	RESERVED	For TI use only	N/A

Table 3-40. TI_RESERVED_STATUS_7

Address: 0x8003		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
32771.15:0	RESERVED	For TI use only	N/A

Table 3-41. TI_RESERVED_STATUS_8

Address: 0x8004		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
32772.15:0	RESERVED	For TI use only	N/A

Table 3-42. TI_RESERVED_STATUS_9

Address: 0x8005		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
32773.15:0	RESERVED	For TI use only	N/A

Table 3-43. TI_RESERVED_STATUS_10

Address: 0x8006		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
32774.15:0	RESERVED	For TI use only	N/A

Table 3-44. TI_RESERVED_STATUS_11

Address: 0x8007		Default: 0x0000	
BIT(s)	**NAME**	**DESCRIPTION**	**ACCESS**
32775.15:0	RESERVED	For TI use only	N/A

3.1 LL = Latched Low

Latched low means that if a condition is occurring, the register bit will read low. Latched low also means that if a condition has occurred since the last time the register was read, it will read low. If a latched low register bit reads high, it means that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched low register, when read low, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read high. If it is still occurring, the second read will read low.

3.2 LH = Latched High

Latched high means that if a condition is occurring, the register bit will read high. Latched high also means that if a condition has occurred since the last time the register was read, it will read high. If a latched high register bit reads low, it means that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched high register, when read high, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read low. If it is still occurring, the second read will read high.

3.3 COR = Clear On Read

Counters indicated as COR are cleared after being read.

4 ELECTRICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		VALUE / UNIT
Supply voltage	DVDD, AVDD, VDDT, VPP, VDDD	–0.3 to 1.4 V
	VDDRA/B, VDDO1/2/3, VDDQA/B, VREFTA/B	–0.3 to 2.2 V
Input Voltage, V_I	(LVCMOS/LVPECL/HSTL/CML/Analog)	–0.3 to Supply + 0.3 V
Storage temperature		–65°C to 150°C
Electrostatic Discharge	HBM	1 KV
	CDM	500 V
Characterized free-air operating temperature range		–40°C to 85°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground (AGND/DGND).

4.2 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
VDDD AVDD DVDD VDDT VPP	Digital / Analog Supply Voltages		0.95	1.00	1.05	V
VREFTA VREFTB	HSTL Voltage Reference Accuracy	VDDQA/2 or VDDQB/2 Voltage Variance	–1%		1%	
VDDQA/B	HSTL I/O Supply Voltages	1.5V Nominal	1.4	1.5	1.6	V
		1.8V Nominal	1.7	1.8	1.9	
VDDRA VDDRB	SERDES PLL Regulator Voltage	1.5V Nominal	1.425	1.5	1.575	V
		1.8V Nominal	1.71	1.8	1.89	
VDDO1/2/3	LVCMOS I/O Supply Voltage	1.5V Nominal	1.425	1.5	1.575	V
		1.8V Nominal	1.71	1.8	1.89	
I_{DD} Supply Current	VDDD	6.144 Gbps			75	mA
	AVDD				250	
	DVDD + VPP				200	
	VDDT				15	
	VDDQA/B (1.5V /1.8V Mode)				650/800	
	VDDRA + VDDRB (1.5V /1.8V Mode)				40/40	
	VDDO1+VDDO2+VDDO3 (1.5V /1.8V Mode)				5/10	
	VREFTA + VREFTB (1.5V /1.8V Mode)				0.5/0.5	
P_D	All Supplies Worst Case	See Table 4-3.				W
I_{SD} Shutdown Current	VDDD	PD* Asserted			28	mA
	AVDD				15	
	DVDD + VPP				62	
	VDDT				1	
	VDDQA/B (1.5V Mode /1.8V Mode)				5/5	
	VDDRA + VDDRB (1.5V Mode /1.8V Mode)				1/1	
	VDDO1+VDDO2+VDDO3 (1.5V Mode /1.8V Mode)				1/2	
	VREFTA + VREFTB (1.5V /1.8V Mode)				0.05/0.05	

4.3 Reference Clock Timing Requirement (REFCLK_0/1_P/N)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Frequency		122.88	–	800	MHz
Accuracy	Relative to Nominal Serial Data Rate	–100		100	ppm
	Relative to Incoming Serial Data Rate	–200		200	
Accuracy to TXCLK_A/B	Synchronous (Multiple/Divide)	0	0	0	ppm
Duty Cycle	High Time	45%	50%	55%	
Jitter	Random and deterministic			40	ps

4.4 Differential Reference Clock Electrical Characteristics (REFCLK_0/1_P/N)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
V_{id}	Differential Input Voltage		250		2000	mV_{dfpp}
C_{IN}	Input Capacitance				3	pF
R_{IN}	Input Differential Impedance		80	100	120	Ω
T_{rise}	Rise Time	20% to 80%	50		600	ps

4.5 Differential Clock Output Electrical Characteristics (CLK_OUT_P/N)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
V_{od}	Differential Output Voltage	Peak to peak	1000		2000	mV_{dfpp}
T_{Rise}	Output Rise Time	10 to 90% 2pF lumped C loadAC Coupled			180	ps
R_{TERM}	Output Termination	CLK_OUT_P/N to DVDD	40	50	60	Ω
F_{MAX}	Output Frequency		0		625	MHz

4.6 LVCMOS Electrical Characteristics (VDDO = VDDO1/VDDO2/VDDO3)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 2 mA, Driver Enabled (1.8 V)	VDDO – 0.45		VDDO	V
		I_{OH} = 2 mA, Driver Enabled (1.5 V)	0.75×VDDO		VDDO	
V_{OL}	Low-level output voltage	I_{OL} = –2 mA, Driver Enabled (1.8 V)	0		0.45	V
		I_{OL} = –2 mA, Driver Enabled (1.5 V)	0		0.25×VDDO	
V_{IH}	High-level input voltage		0.65×VDDO		VDDO+0.3	V
V_{IL}	Low-level input voltage		-0.3		0.35×VDDO	V
I_{IH}, I_{IL}	Receiver Only	Low/High Input Current			±170	µA
I_{OZ}	Driver Only	Driver Disabled			±25	µA
	Driver/Receiver With Pullup/Pulldown	Driver DisabledWith Pull Up/Down Enabled			±195	µA
C_{IN}	Input capacitance				3	pF

4.7 HSTL Signals Electrical Characteristics (VDDQA/B = 1.5/1.8V)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$V_{OH(dc)}$	High-level output voltage		VDDQA/B – 0.4		VDDQA/B + 0.3	V
$V_{OL(dc)}$	Low-level output voltage				0.40	V
$V_{OH(ac)}$	High-level output voltage		VDDQA/B – 0.5		VDDQA/B + 0.3	V
$V_{OL(ac)}$	Low-level output voltage				0.50	V
$V_{IH(dc)}$	High-level DC input voltage	DC input, logic high	VREFTA/B+ 0.10		VDDQA/B + 0.3	V
$V_{IL(dc)}$	Low-level DC input voltage	DC input, logic low	-0.30		VREFTA/B – 0.1	V
$V_{IH(ac)}$	High-level AC input voltage	AC input, logic high	VREFTA/B + 0.20		VDDQA/B + 0.3	V

HSTL Signals Electrical Characteristics (VDDQA/B = 1.5/1.8V) *(continued)*

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$V_{IL(ac)}$	Low-level AC input voltage	AC input, logic low	–0.30		VREFTA/B – 0.20	V
$I_{OH(dc)}$	High output current		8			mA
$I_{OL(dc)}$	Low output current		–8			mA
I_{IH}	Input High Current				10	µA
I_{IL}	Input Low Current				–10	µA
C_{IN}	Input Capacitance				4	pF
Tacr	AC Test Condition	Rise Time Rate (In 20 → 80% Swing Region)	1	1	1	ns/V
Tacs	AC Test Condition	Signal Swing	1	1	1	V

4.8 Serial Transmitter Characteristics

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
$V_{OD(pp)}$	TX Output Differential Peak-to-Peak voltage swing See Figure 4-1 and Figure 4-2	SWING (2.3:0) = 0000	84	126	160	mV_{dfpp}
		SWING (2.3:0) = 0001	163	215	253	
		SWING (2.3:0) = 0010	247	303	347	
		SWING (2.3:0) = 0011	331	395	444	
		SWING (2.3:0) = 0100	415	478	538	
		SWING (2.3:0) = 0101	499	572	633	
		SWING (2.3:0) = 0110	582	662	735	
		SWING (2.3:0) = 0111	668	756	835	
		SWING (2.3:0) = 1000	740	839	927	
		SWING (2.3:0) = 1001	831	932	1020	
		SWING (2.3:0) = 1010	904	1020	1130	
		SWING (2.3:0) = 1011	988	1110	1220	
		SWING (2.3:0) = 1100	1060	1190	1340	
		SWING (2.3:0) = 1101	1150	1280	1430	
		SWING (2.3:0) = 1110	1220	1360	1530	
		SWING (2.3:0) = 1111	1300	1450	1630	
$V_{pre/post}$	TX Output Pre/Post Cursor Emphasis Voltage	See register bits TWPOST1 2.12:8 and TWPRE 2.7:4 for de-emphasis settings. See Figure 4-2.	–17.5/ –37.5%		+17.5/ +37.5%	
V_{CMT}	TX output common mode voltage	See Figure 4-1		VDDT – [0.25×$V_{OD(pp)}$]		mV
t_{skew}	Output Skew	CPRI LV			15	ps
		CPRI HV			25	
		CPRI LV-II (DCD ≤ 0.05UI)			15	
tr, tf	Differential output signal rise, fall time (20% to 80%)Differential Load = 100Ω	CPRI LV (Note: MIN is not per CPRI)	54	–	–	ps
		CPRI HV (Note: MIN is not per CPRI)	55	–	327	
		CPRI LV-II	30	–	–	
J_T	Serial Output Total Jitter (CPRI LV/LV-II and OBSAI rates)	Serial Rate ≤ 3.072 Gbps(Not Applicable to LV-II)			0.35	UI
		Serial Rate > 3.072 Gbps(And All LV-II Rates)			0.30	
J_D	Serial Output Deterministic Jitter (CPRI LV/LV-II and OBSAI rates)	Serial Rate ≤ 3.072 Gbps(Not Applicable to LV-II)			0.17	UI
		Serial Rate > 3.072 Gbps(And All LV-II Rates)			0.15	
J_T	Serial Output Total JitterJitter (CPRI E.6/12.HV)	CPRI E.6/12.HV(0.6144 and 1.2288 Gbps)			0.279	
J_D	Serial Output Deterministic Jitter (CPRI E.6/12.HV)				0.14	
$T_{(LATENCY)}$	Transmit Latency	See latency specifications in Appendix D.	–	–	–	Bit Times

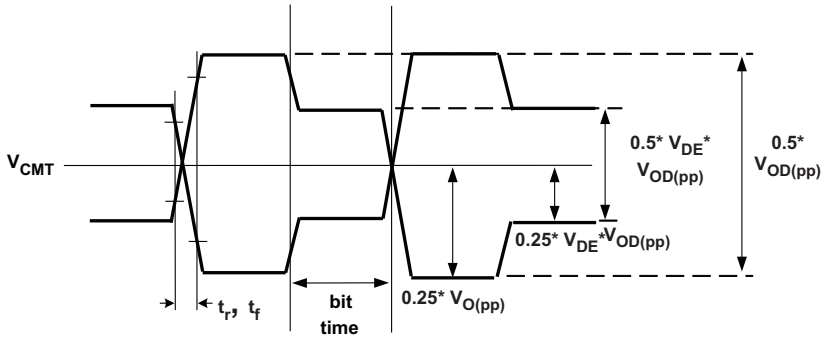
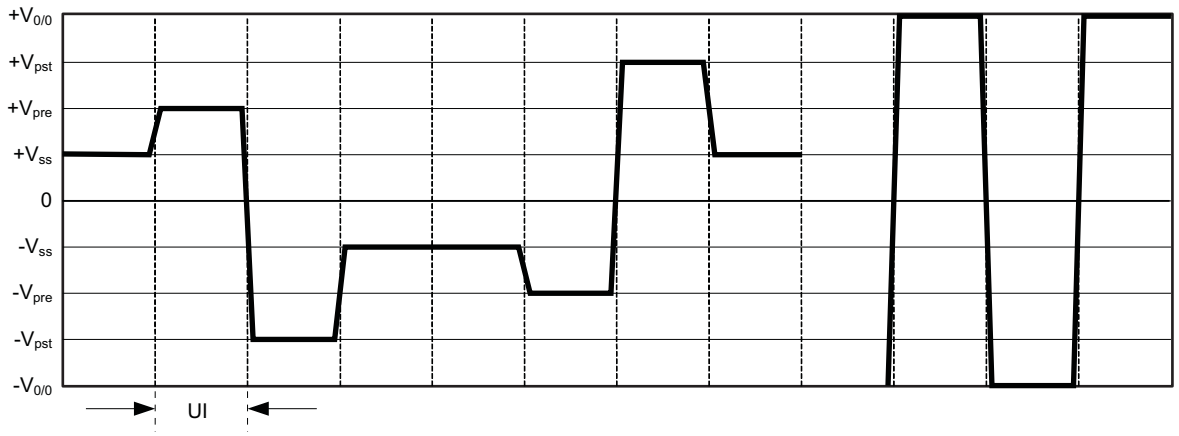


Figure 4-1. Transmit Output Waveform Parameter Definitions



h_{-1} = TWPRE (0%⟶-17.5% for typical application) setting
h_1 = TWPOST1 (0%⟶-37.5% for typical application) setting
$h_0 = 1 - |h_1| - |h_{-1}|$
$V_{0/0}$ = Output Amplitude with TWPRE = 0%, TWPOST = 0%.
V_{ss} = Steady State Output Voltage = $V_{0/0} * | h_1 + h_0 + h_{-1}|$
V_{pre} = PreCursor Output Voltage = $V_{0/0} * | -h_1 – h_0 + h_{-1}|$
V_{pst} = PostCursor Output Voltage = $V_{0/0} * | -h_1 + h_0 + h_{-1}|$

Figure 4-2. Pre/Post Cursor Swing Definitions

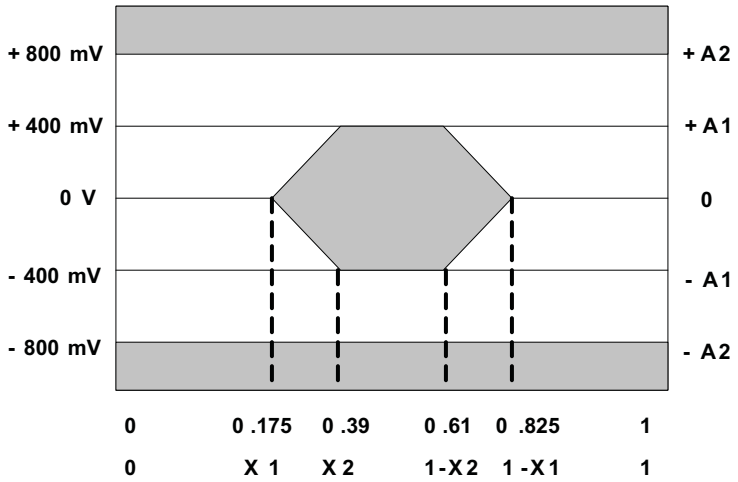


Figure 4-3. CPRI TX LV Mask for: E.6/12/24/30.LV (0.6144/1.2288/2.4576/3.072 Gbps)

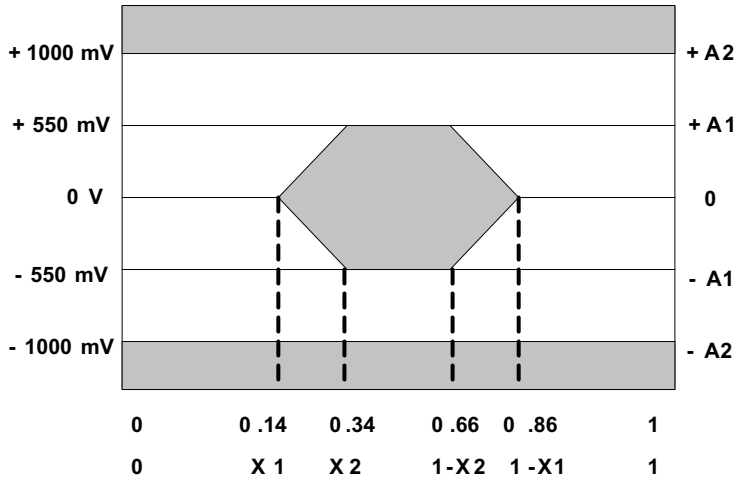


Figure 4-4. CPRI TX HV Output Mask for: E.6/12.HV (0.6144/1.2288 Gbps)

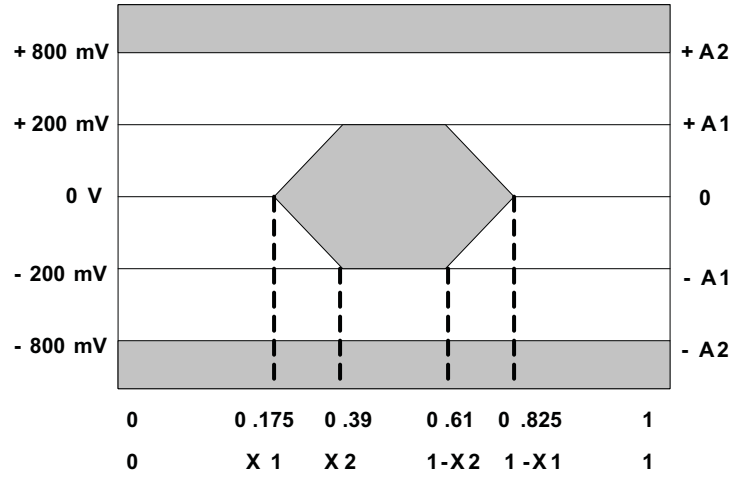


Figure 4-5. OBSAI TX Output Mask for Rates ≤ 3.072 Gbps

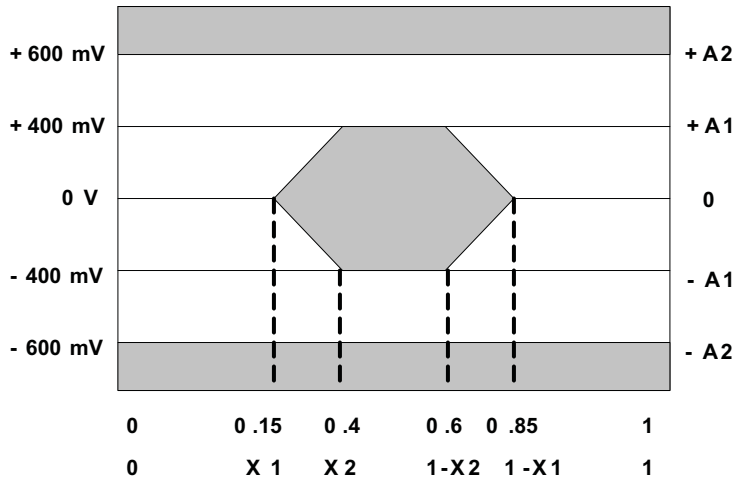


Figure 4-6. OBSAI 6.144 Gbps and CPRI (LV-II) (All Rates) TX Output Mask

Note: Due to process variation, the output mask cannot always be achieved with a common setting for all devices. However, for a given device, a particular swing setting will pass output mask requirements.

4.9 Serial Receiver Characteristics

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
V_{ID}	RX input differential voltage|RXP – RXN|	Full Rate AC Coupled	50		600	mV
		Half/Quarter/Eighth Rate AC Coupled	50		800	
$V_{ID(pp)}$	RX input differential peak-to-peak voltage swing 2×|RXP – RXN|	Full Rate AC Coupled	100		1200	mV_{dfpp}
		Half/Quarter/Eighth Rate AC Coupled	100		1600	
C_I	RX input capacitance				2	pF
J_{TOL}	Jitter Tolerance, Total Jitter at Serial Input (DJ + RJ)(BER 10^{-15})	Zero crossing Half/Quarter/Eighth Rate			0.66	UI_{p-p}
		Zero crossing Full Rate			0.65	
J_{DR}	Serial Input Deterministic Jitter(BER 10^{-15})	Zero crossing Half/Quarter/Eighth Rate			0.50	
		Zero crossing Full Rate			0.35	
$T_{(LATENCY)}$	Receive Latency	See latency specifications in Appendix D	–	–	–	Bit Times

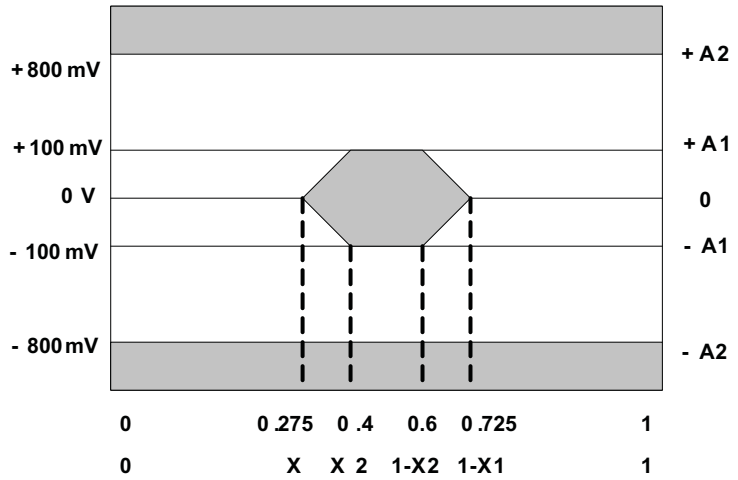


Figure 4-7. CPRI LV Receiver Mask for E.6/12/24/30.LV (0.6144/1.2288/2.4576/3.072 Gbps)

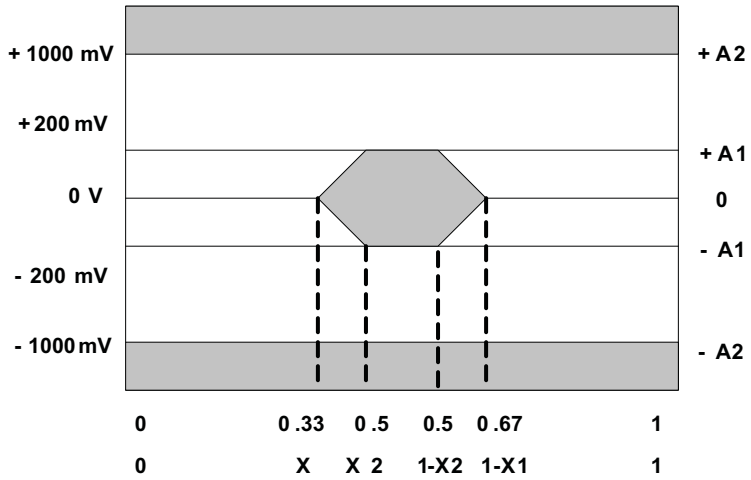


Figure 4-8. CPRI HV Receiver Mask for E.6/12.HV (0.6144/1.2288 Gbps)

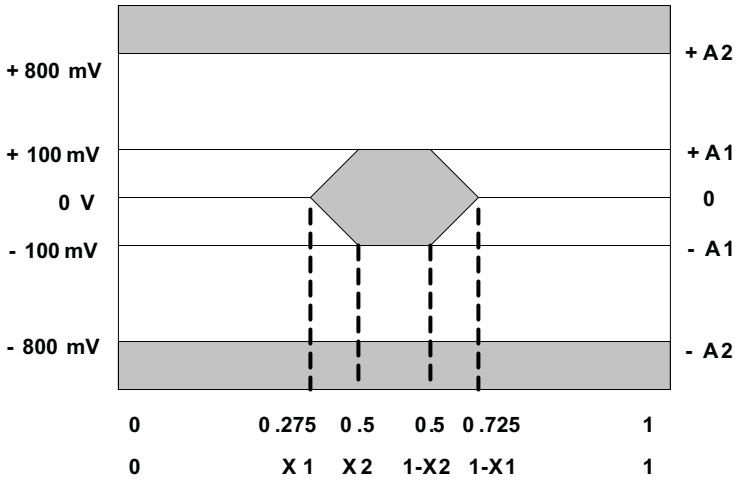


Figure 4-9. OBSAI Receiver Mask for Rates ≤ 3.072 Gbps

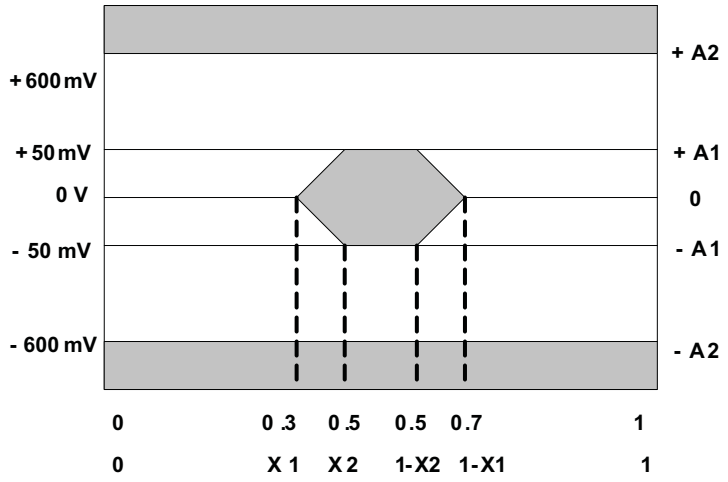


Figure 4-10. OBSAI 6.144 Gbps and CPRI LV-II (All Rates) Receiver Mask

Jitter Tolerance:

The peak to peak total jitter tolerance for the RP3 receiver is 0.65 UI. This total jitter is composed of three components; deterministic jitter, random jitter, and an additional sinusoidal jitter.

The deterministic jitter tolerance is 0.37 UI minimum. The sum of deterministic and random jitter is 0.55 UI minimum. The additional sinusoidal jitter which the receiver must tolerate will have frequencies and amplitudes conforming to the mask presented in Figure 4-11 and Table 4-1.

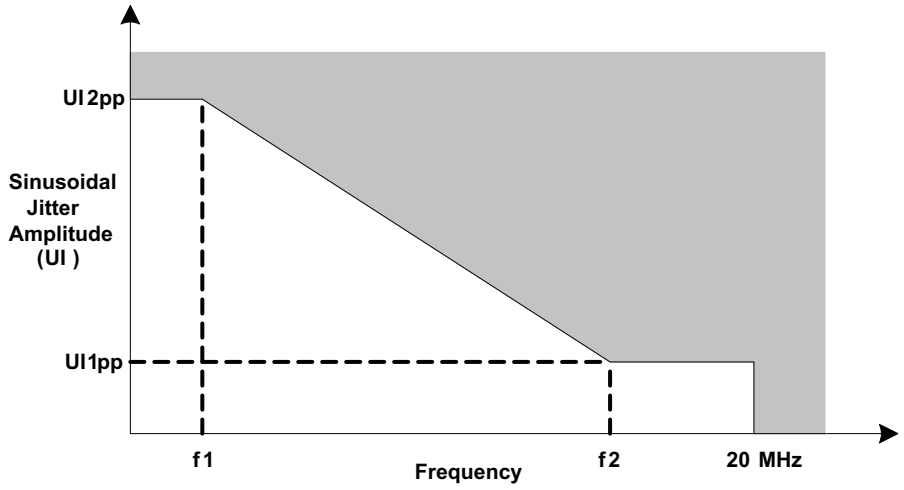
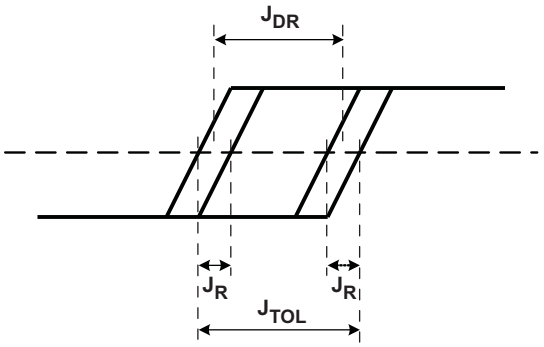


Figure 4-11. OBSAI Sinusoidal Jitter Mask

Table 4-1. Sinusoidal Jitter Mask Values

Frequency (MBaud)	f1 (kHz)	f2 (kHz)	UI1pp	UI2pp
768	5.4	460.8	0.1	8.5
1536	10.9	921.6	0.1	8.5
3072	21.8	1843.2	0.1	8.5
6114	36.9	3686	0.05	8.5

Input Jitter Definition



NOTE: $J_{TOL} = J_R + J_{DR}$, where J_{TOL} is the receive jitter tolerance, J_{DR} is the received deterministic jitter, and J_R is the Gaussian random edge jitter distribution at a maximum BER = 10^{-12} for CPRI link and BER = 10^{-15} for OBSAI (RP3) link.

4.10 HSTL Output Switching Characteristics (DDR Timing Mode Only)

(over recommended operating conditions unless otherwise noted).

PARAMETER		CONDITION	MIN	MAX	UNIT
t_{setup}	RDx(1) setup prior to RXCLK_x transition high or low	Source Centered. See Figure 4-12(2)	0.15 × tperiod		ps
t_{hold}	RDx hold after RXCLK_x transition high or low	Source Centered. See Figure 4-12(2)	0.15 × tperiod		ps
T_{duty}	RXCLK_x(3) Duty Cycle	Source Centered and Source Aligned.(2)	45%	55%	
t_{period}	RXCLK_x Period	Source Centered and Source Aligned.	6.4	85.11	ns
T_{freq}	RXCLK_x Frequency	Source Centered and Source Aligned.	11.75	156.25	MHz
T_{pd}	RXCLK_x rising or falling to RDx valid.	Source Aligned See Figure 4-13(2)	–0.10 × tperiod	+0.10 × tperiod	ps

(1) RDx refers to either RDA or RDB for channels A and B respectively
(2) Cload = 10pF, using timing reference of (VDDQA/B)/2.
(3) RXCLK_x refers to RXCLK_A or RXCLK_B for channels A and B respectively.

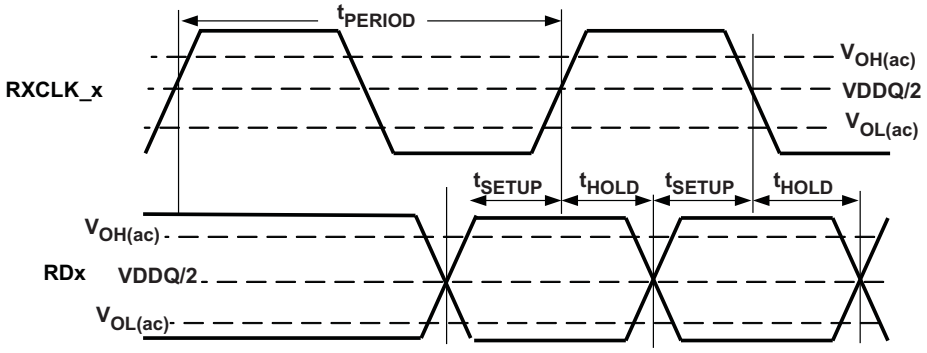


Figure 4-12. HSTL (DDR Timing Mode Only) Source Centered Output Timing Requirements

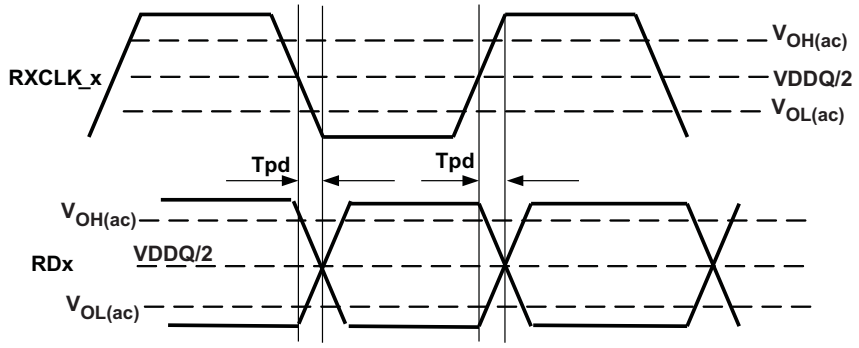


Figure 4-13. HSTL (DDR Timing Mode Only) Source Aligned Output Timing Requirements

4.11 HSTL Output Switching Characteristics (SDR Timing Mode Only)

PARAMETER		CONDITION	MIN	MAX	UNIT
T_{duty}	RXCLK_x(1) Duty Cycle	Rising and Falling Edge Aligned Data(2)	40%	60%	
t_{period}	RXCLK_x Period	Rising and Falling Edge Aligned Data	3.2	42.55	ns
T_{freq}	RXCLK_x Frequency	Rising and Falling Edge Aligned Data	23.5	312.5	MHz
T_{pd}	RXCLK_x rising to RDx(3) valid.	Rising Edge Aligned, See Figure 4-14.(2)	–0.10 × t_{period}	+0.10 × t_{period}	ps
	RXCLK_x falling to RDx valid.	Falling Edge Aligned, See Figure 4-15.(2)	–0.10 × t_{period}	+0.10 × t_{period}	ps

(1) RXCLK_x refers to RXCLK_A or RXCLK_B for channels A and B respectively.
(2) Cload = 10pF, using timing reference of (VDDQA/B)/2.
(3) RDx refers to either RDA or RDB for channels A and B respectively.

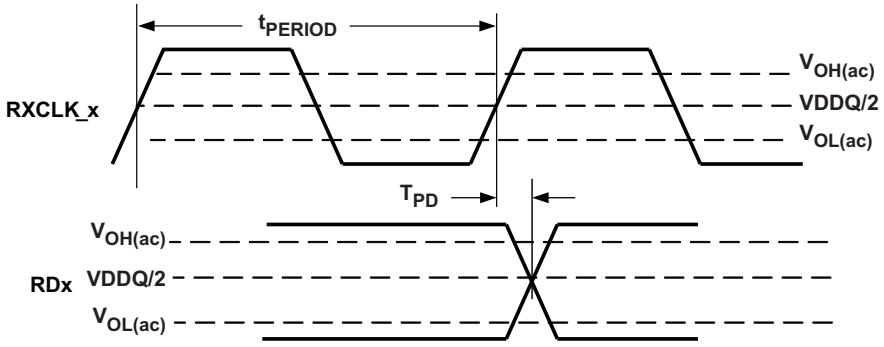


Figure 4-14. HSTL (SDR Timing Mode Only) Rising Edge Aligned Output Timing Requirements

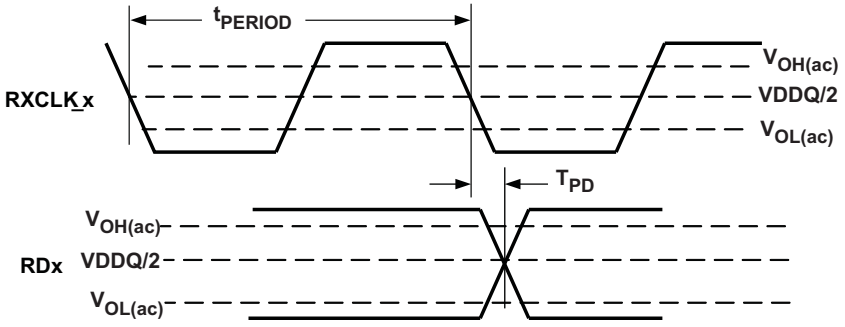


Figure 4-15. HSTL (SDR Timing Mode Only) Falling Edge Aligned Output Timing Requirements

4.12 HSTL (DDR Timing Mode Only) Input Timing Requirements

PARAMETER		CONDITION	MIN	MAX	UNIT
t_{setup}	TDx(1) setup prior to TXCLK_x(2) transition high or low	Source Centered, See Figure 4-16 and (3)	0.075 × t_{period}		ps
t_{hold}	TDx hold after TXCLK_x transition high or low	Source Centered, See Figure 4-16 and (3)	0.075 × t_{period}		ps
t_{duty}	TXCLK_x Duty Cycle	Source Centered, See Figure 4-16 and (3)	40%	60%	
		Source Aligned, See Figure 4-17 and (3)	45%	55%	
t_{period}	TXCLK_x Period	Source Centered and Aligned	6.4	85.11	ns
T_{freq}	TXCLK_x Frequency	Source Centered and Aligned	11.75	156.25	MHz
T_{skew}(4)(5)	TXCLK_x rising or falling to TDx valid.	Source Aligned, See Figure 4-17 and (3)	–0.14 × t_{period}	+0.14 × t_{period}	ps

(1) TDx refers to either channel A (TDA) or B (TDB).
(2) TXCLK_x refers to either channel A (TXCLK_A) or channel B (TXCLK_B).
(3) Input timing reference of (VDDQA/B)/2 with ±1 ns/V rise time on all input signals.
(4) When T_{freq} ≤60 MHz, Tskew Minimum is –3ns.
(5) When T_{freq} ≤60 MHz, Tskew Maximum is 3ns.

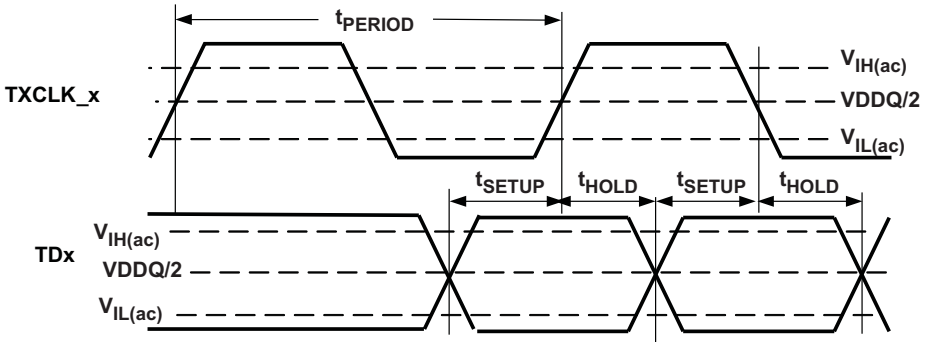


Figure 4-16. HSTL (DDR Timing Mode Only) Source Centered Data Input Timing Requirements

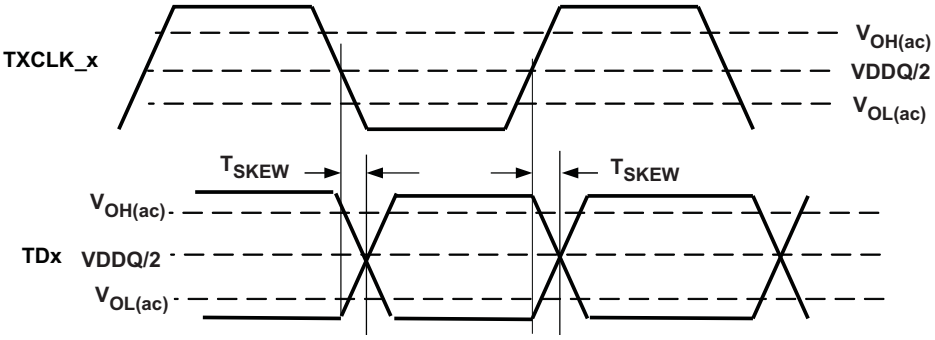


Figure 4-17. HSTL (DDR Timing Mode Only) Source Aligned Data Input Timing Requirements

4.13 HSTL (SDR Timing Mode Only) Input Timing Requirements

PARAMETER		CONDITION	MIN	MAX	UNIT
t_{setupH}	TDx(1) setup prior to TXCLK_x(2) transition high	Falling Edge Aligned (Rising Edge Sampled) Data,(3) See Figure 4-18	480		ps
t_{holdH}	TDx hold after TXCLK_x transition high		480		ps
t_{setupL}	TDx setup prior to TXCLK_x transition low	Rising Edge Aligned (Falling Edge Sampled) Data,(3) See Figure 4-19	480		ps
t_{holdL}	TDx hold after TXCLK_x transition low		480		ps
t_{duty}	TXCLK_x Duty Cycle	Rising and Falling Edge Sampled Data	40%	60%	
t_{period}	TXCLK_x Period	Rising and Falling Edge Aligned Data	3.2	42.55	ns
T_{freq}	TXCLK_x Frequency	Rising and Falling Edge Aligned Data	23.5	312.5	MHz

(1) TDx refers to either channel A (TDA) or B (TDB).
(2) TXCLK_x refers to either channel A (TXCLK_A) or channel B (TXCLK_B).
(3) Input timing reference of (VDDQA/B)/2 with ±1 ns/V rise time on all input signals.

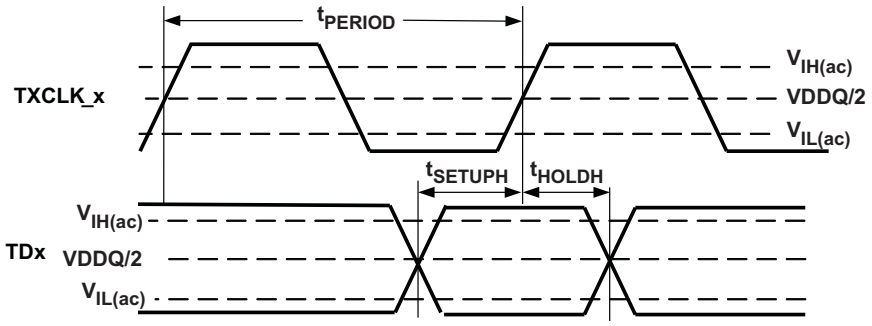


Figure 4-18. HSTL (SDR Timing Mode Only) Falling Edge Aligned (Rising Edge Sampled) Data Input Timing Requirements

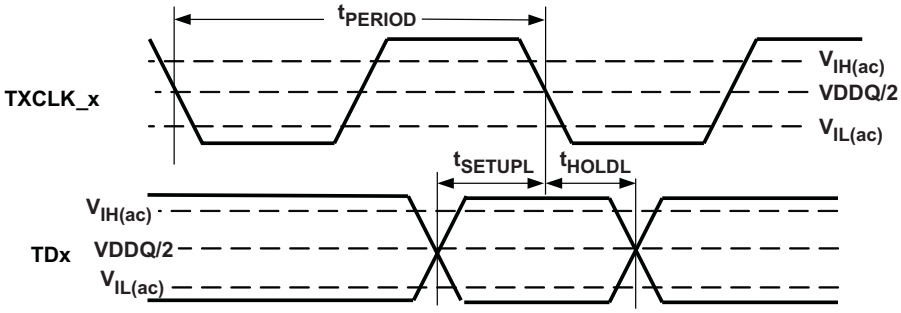


Figure 4-19. HSTL (SDR Timing Mode Only) Rising Edge Aligned (Falling Edge Sampled) Data Input Timing Requirements

4.14 MDIO Timing Requirements Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
t_{period}	MDC period	See Figure 4-20	100			
t_{setup}	MDIO setup to ↑ MDC		10			
t_{hold}	MDIO hold to ↑ MDC		10			
T_{valid}	MDIO valid from MDC ↑		0		40	ns

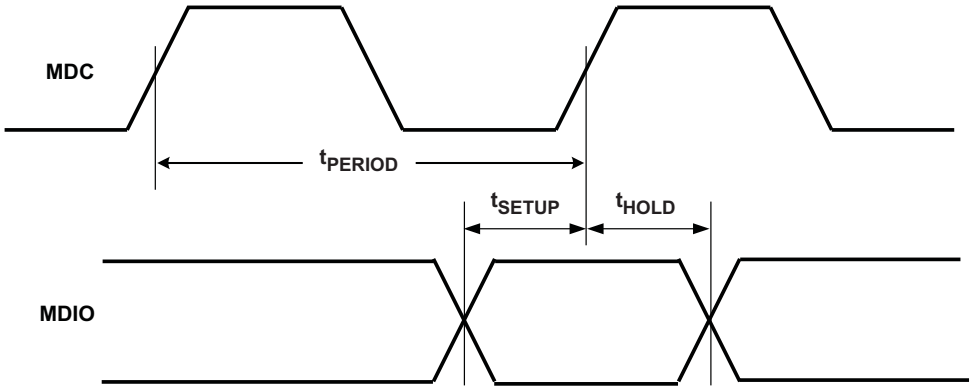


Figure 4-20. MDIO Read/Write Timing

4.15 JTAG Timing Requirements Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
T_{period}	TCK period	See Figure 4-21	66.67			ns
T_{setup}	TDI/TMS/TRST_N setup to ↑ TCK		3			ns
T_{hold}	TDI/TMS/TRST_N hold from ↑ TCK		5			ns
T_{valid}	TDO delay from TCK Falling		0		10	ns

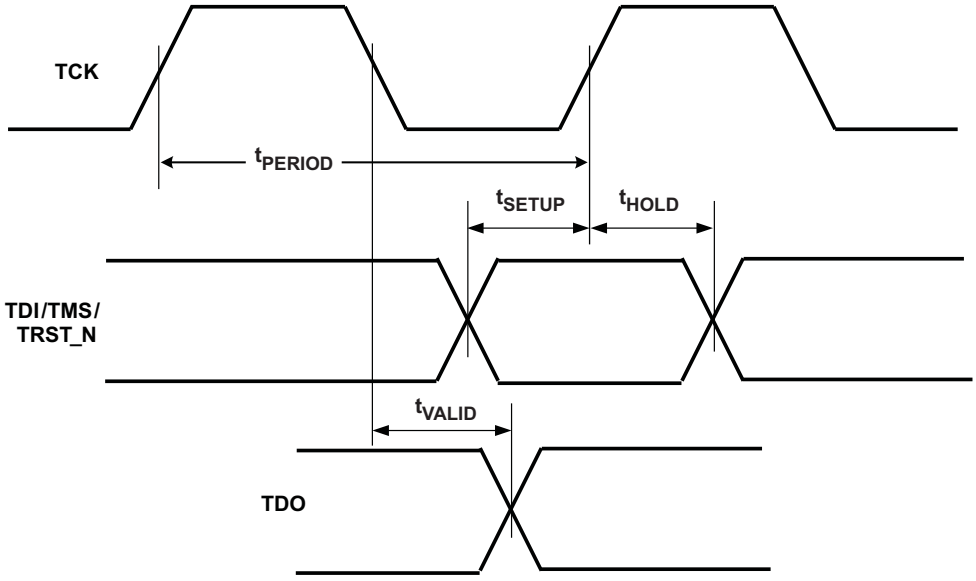


Figure 4-21. JTAG Timing

4.16 Power Sequencing Guidelines

The TLK6002 allows either the core or I/O power supply to be powered up for an indefinite period of time while the other supply is not powered up, if all of the following conditions are met:

1. All maximum ratings and recommending operating conditions are followed
2. Bus contention while 1.5/1.8V power is applied (>0V) must be limited to 100 hours over the projected lifetime of the device.
3. Junction temperature is less than 105°C during device operation. Note: Voltage stress up to the absolute maximum voltage values for up to 100 hours of lifetime operation at a T_J of 105°C or lower will minimally impact reliability.

The TLK6002 inputs are not failsafe (i.e. cannot be driven with the I/O power disabled). TLK6002 inputs should not be driven high until their associated power supply is active.

4.17 HSTL Interface

The HSTL interface allows for either 1.5V or 1.8V operation. Source series (output) and parallel end (input) resistance is dynamically updated to compensate for process, voltage, and temperature. RES* device pins are referenced to accurately set the impedances.

The source series (HSTL output) impedance is dynamically calibrated to 50 Ω using an external 50 Ω resistor.

There are three options on parallel end (HSTL input) termination:

1. No end termination. This yields the lowest power dissipation, at the cost of signal integrity performance.
2. Half Strength Mode – 100 Ω Thevenin Equivalent – This mode is comprised of two 200 Ω resistors, placed between the input signal and VDDQA/B, and the input signal and DGND. This selection yields a blend between signal integrity performance and power dissipation.
3. Full Strength Mode – 50 Ω Thevenin Equivalent – This mode is comprised of two 100 Ω resistors, placed between the input signal and VDDQA/B, and the input signal and DGND. This selection yields the best signal integrity performance at the cost of highest power dissipation.

All three HSTL input modes can be selected through the MDIO interface on a per channel basis through register bits (6.1:0). The HSTL output driver slew rate is also selectable, and is selected in register bit (6.2).

Figure 4-22 shows the schematic of the internal HSTL driver and internal HSTL receiver.

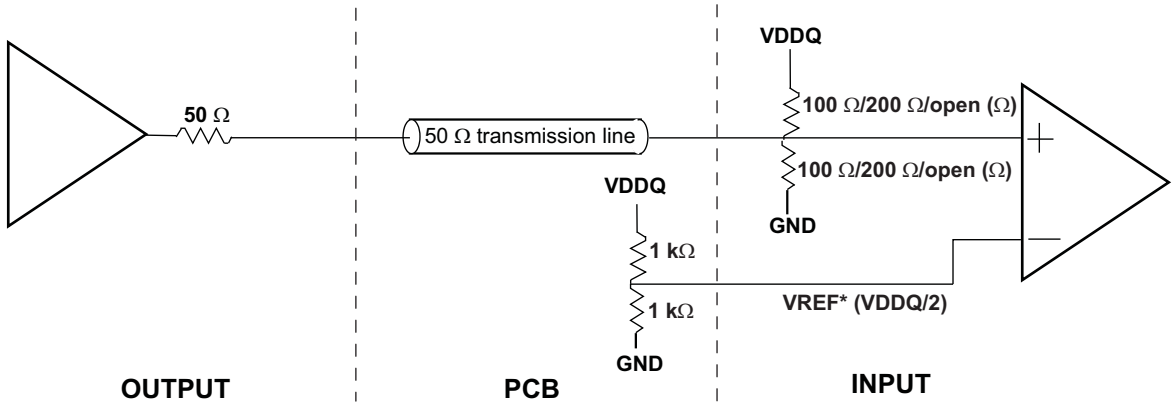


Figure 4-22. HSTL I/O Schematic

4.18 Device Initialization

The following subsections provide proper provisioning sequences for various TLK6002 operating modes using the MDIO interface. Please note that the provisioning method for optimal serial link performance is dependent on system characteristics such as the length of an electrical cable or printed circuit board trace connected to the serial interface. For long electrical serial links such as long backplane and cable channels, the standard MDIO provisioning method is preferred. For short electrical serial links such as between the SERDES and an optical module, the STCI-via-MDIO provisioning method is preferred. The STCI-via-MDIO provisioning method provides a way to further fine-tune the serial link performance. The STCI-via-MDIO provisioning method is described in detail in the “TLK6002 Provisioning for Optimal Serial Link Performance” application note.

4.18.1 20-Bit Interface Mode (8b/10b Encoder/Decoder Disabled) (All CPRI/OBSAI Rates)

Note: Assume both channel A and channel B have the same setup.

REFCLK frequency = 122.88 MHz, Mode = Transceiver, Parallel Interface = 20-Bit SDR Falling Edge Aligned Mode, RXCLK_A/B out = RXBCLK_A/B, Serial Data Rate is CPRI/OBSAI standard rate as shown below.

- Device Pin Setting(s) – Pin settings allow for maximum software configurability.
  - Ensure CODEA_EN input pin is Low.
  - Ensure CODEB_EN input pin is Low.
  - Ensure RATE_A[2:0] input pins are 3’b100 (High, Low, Low) to enable software control.
  - Ensure RATE_B[2:0] input pins are 3’b100 (High, Low, Low) to enable software control.
  - Ensure PD_TRXA_N input pin is High.
  - Ensure PD_TRXB_N input pin is High.
  - Ensure PRBS_EN input pin is Low.
  - Ensure REFCLK_A_SEL input pin is Low to enable software control.
  - Ensure REFCLK_B_SEL input pin is Low to enable software control.
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 µs -or- Write 1’b1 to 0.15 GLOBAL_RESET) after power supply stabilization.
- Enable MDIO global write so that each MDIO write affects both channels to shorten provisioning time
  - Write 1’b1 to 0.11 GLOBAL_WRITE
- Clock Configuration
  - Select Channel A SERDES REFCLK input (Default = REFCLK_0_P/N)
    - If REFCLK_0_P/N used – Write 1’b0 to 0.1 REFCLK_A_SEL
    - If REFCLK_1_P/N used – Write 1’b1 to 0.1 REFCLK_A_SEL
  - Select Channel B SERDES REFCLK input (Default = REFCLK_0_P/N)
    - If REFCLK_0_P/N used – Write 1’b0 to 0.0 REFCLK_B_SEL
    - If REFCLK_1_P/N used – Write 1’b1 to 0.0 REFCLK_B_SEL
- Data Rate Setting (select one of the following 8 cases)
  - If serial data rate is 6144.00Mbps: write 2’b00 to 1.7:6 RATE_TX[1:0], write 2’b00 to 1.5:4 RATE_RX[1:0], write 4’b1110 to 1.3:0 PLL_MULT[3:0] to select FULL rate and 25x MPY (CHANNEL_CONTROL_1 = 0x010E).
  - If serial data rate is 4915.20Mbps: Write 2’b00 to 1.7:6 RATE_TX[1:0], write 2’b00 to 1.5:4 RATE_RX[1:0], write 4’b1101 to 1.3:0 PLL_MULT[3:0] to select FULL rate and 20x MPY (CHANNEL_CONTROL_1 = 0x010D).
  - If serial data rate is 3072.00Mbps: Write 2’b01 to 1.7:6 RATE_TX[1:0], write 2’b01 to 1.5:4 RATE_RX[1:0], write 4’b1110 to 1.3:0 PLL_MULT[3:0] to select HALF rate and 25x MPY (CHANNEL_CONTROL_1 = 0x015E).
  - If serial data rate is 2457.60Mbps: Write 2’b01 to 1.7:6 RATE_TX[1:0], write 2’b01 to 1.5:4

RATE_RX[1:0], write 4'b1101 to 1.3:0 PLL_MULT[3:0] to select HALF rate and 20x MPY (CHANNEL_CONTROL_1 = 0x015D).
  - If serial data rate is 1536.00Mbps: Write 2'b10 to 1.7:6 RATE_TX[1:0], write 2'b10 to 1.5:4 RATE_RX[1:0], write 4'b1110 to 1.3:0 PLL_MULT[3:0] to select QUARTER rate and 25x MPY (CHANNEL_CONTROL_1 = 0x01AE).
  - If serial data rate is 1228.80Mbps: Write 2'b10 to 1.7:6 RATE_TX[1:0], write 2'b10 to 1.5:4 RATE_RX[1:0], write 4'b1101 to 1.3:0 PLL_MULT[3:0] to select QUARTER rate and 20x MPY (CHANNEL_CONTROL_1 = 0x01AD).
  - If serial data rate is 768.00Mbps: Write 2'b11 to 1.7:6 RATE_TX[1:0], write 2'b11 to 1.5:4 RATE_RX[1:0], write 4'b1110 to 1.3:0 PLL_MULT[3:0] to select EIGHTH rate and 25x MPY (CHANNEL_CONTROL_1 = 0x01FE).
  - If serial data rate is 614.40Mbps: Write 2'b11 to 1.7:6 RATE_TX[1:0], write 2'b11 to 1.5:4 RATE_RX[1:0], write 4'b1101 to 1.3:0 PLL_MULT[3:0] to select EIGHTH rate and 20x MPY (CHANNEL_CONTROL_1 = 0x01FD).
- Serial Configuration
  - Configure the following bits per the desired application
    - 1.9:8 (LOOP_BANDWIDTH[1:0])
    - 2.12:8 (TWPOST1[4:0])
    - 2.7:4 (TWPRE[3:0])
    - 2.3:0 (SWING[3:0])
    - 8.14:12 (EQPRE[2:0])
    - 8.11:10 (CDRTHR[1:0]) = 2'b01
    - 8.9:8 (CDRFMULT[1:0]) = 2'b00
- Mode Control
  - Channel synchronization (comma enable) is on by default and the parallel output 10 bit codes are byte aligned.
  - The default MDIO register settings should enable TBI SDR Falling Edge Aligned mode. To use a different parallel IO align mode:
    - If SDR Rising Edge Aligned: write 0x0183 to CHANNEL_CONTROL_3 register.
    - If DDR Source Centered: write 0x01C0 to CHANNEL_CONTROL_3 register.
    - If DDR Source Aligned: write 0x01C3 to CHANNEL_CONTROL_3 register.
- Enable desired status signals to LOSA and LOSB for real time monitoring per channel. Any number of signals can be enabled at once.
  - If SERDES Rx Loss of Signal condition monitored: write 1'b1 to 6.10 LOS_OVERLAY.
  - If channel synchronization status monitored: write 1'b1 to 6.9 CH_SYNC_OVERLAY.
  - If PLL lock status monitored: write 1'b1 to 6.8 PLL_LOCK_OVERLAY.
  - If SERDES AGC unlock status monitored: write 1'b1 to 7.7 AGCLOCK_OVERLAY.
  - If SERDES AZDONE status monitored: write 1'b1 to 7.6 AZDONE_OVERLAY.
- Check SERDES PLL Status for Locked State
  - Poll 5.0 PLL_LOCK (per channel) until it is asserted (high)
- Toggle ENRX
  - Write 1'b0 to 20.2 (ENRX)
  - Write 1'b1 to 20.2 (ENRX)
- Final CDR Configuration
  - Wait until either AGC_LOCKED asserted or 250M UI
  - Write 8.9:8 (CDRFMULT[1:0]) = 2'b01
  - Poll 5.13 AGC_LOCKED (1'b1) (per channel)
- Issue Data path Reset
  - Write 1'b1 to 4.3 DATAPATH_RESET

- Clear Latched Registers
  - Read 5 CHANNEL_STATUS_1 to clear (per channel)
- Device provisioning has completed at this point
- Periodically Check Device Operational Mode Status (Non-Errored Read Values Shown Below):
  - Read 5 CHANNEL_STATUS_1 and verify the following bits:
    - 5.14 AZ_DONE (1'b1) (per channel)
    - 5.13 AGC_LOCKED (1'b1) (per channel)
    - 5.7 TX_FIFO_UNDERFLOW (1'b0) (per channel)
    - 5.6 TX_FIFO_OVERFLOW (1'b0) (per channel)
    - 5.5 RX_FIFO_UNDERFLOW (1'b0) (per channel)
    - 5.4 RX_FIFO_OVERFLOW (1'b0) (per channel)
    - 5.2 LOS (1'b0) (per channel). This read value is only useful if the serial input is guaranteed to be above 150mVdfpp.
    - 5.1 CHANNEL_SYNC (1'b1) (per channel)
    - 5.0 PLL_LOCK (1'b1) (per channel)

4.18.2 16-Bit Interface Mode (8b/10b Encoder/Decoder Enabled) (All CPRI/OBSAI Rates)

Note: Assume both channel A and channel B have the same setup.

REFCLK frequency = 122.88 MHz, Mode = Transceiver, Parallel Interface = 16-Bit DDR Source Aligned Mode, RXCLK_A/B out = RXBCLK_A/B, Serial Data Rate is CPRI/OBSAI standard rate as shown below.

- Device Pin Setting(s) – Pin settings allow for maximum software configurability.
  - Ensure CODEA_EN input pin is Low.
  - Ensure CODEB_EN input pin is Low.
  - Ensure RATE_A[2:0] input pins are 3'b100 (High, Low, Low) to enable software control.
  - Ensure RATE_B[2:0] input pins are 3'b100 (High, Low, Low) to enable software control.
  - Ensure PD_TRXA_N input pin is High.
  - Ensure PD_TRXB_N input pin is High.
  - Ensure PRBS_EN input pin is Low.
  - Ensure REFCLK_A_SEL input pin is Low to enable software control.
  - Ensure REFCLK_B_SEL input pin is Low to enable software control.
- Reset Device
  - Issue a hard or soft reset (RESET_N asserted for at least 10 us -or- Write 1'b1 to 0.15 GLOBAL_RESET) after power supply stabilization.
- Enable MDIO global write so that each MDIO write affects both channels to shorten provisioning time
  - Write 1'b1 to 0.11 GLOBAL_WRITE
- Clock Configuration
  - Select Channel A SERDES REFCLK input (Default = REFCLK_0_P/N)
    - If REFCLK_0_P/N used – Write 1'b0 to 0.1 REFCLK_A_SEL
    - If REFCLK_1_P/N used – Write 1'b1 to 0.1 REFCLK_A_SEL
  - Select Channel B SERDES REFCLK input (Default = REFCLK_0_P/N)
    - If REFCLK_0_P/N used – Write 1'b0 to 0.0 REFCLK_B_SEL
    - If REFCLK_1_P/N used – Write 1'b1 to 0.0 REFCLK_B_SEL
- Data Rate Setting (select one of the following 8 cases)
  - If serial data rate is 6144.00Mbps: Write 2'b00 to 1.7:6 RATE_TX[1:0], write 2'b00 to 1.5:4 RATE_RX[1:0], write 4'b1110 to 1.3:0 PLL_MULT[3:0] to select FULL rate and 25x MPY (CHANNEL_CONTROL_1 = 0x010E).
  - If serial data rate is 4915.20Mbps: Write 2'b00 to 1.7:6 RATE_TX[1:0], write 2'b00 to 1.5:4 RATE_RX[1:0], write 4'b1101 to 1.3:0 PLL_MULT[3:0] to select FULL rate and 20x MPY (CHANNEL_CONTROL_1 = 0x010D).
  - If serial data rate is 3072.00Mbps: Write 2'b01 to 1.7:6 RATE_TX[1:0], write 2'b01 to 1.5:4 RATE_RX[1:0], write 4'b1110 to 1.3:0 PLL_MULT[3:0] to select HALF rate and 25x MPY (CHANNEL_CONTROL_1 = 0x015E).
  - If serial data rate is 2457.60Mbps: Write 2'b01 to 1.7:6 RATE_TX[1:0], write 2'b01 to 1.5:4 RATE_RX[1:0], write 4'b1101 to 1.3:0 PLL_MULT[3:0] to select HALF rate and 20x MPY (CHANNEL_CONTROL_1 = 0x015D).
  - If serial data rate is 1536.00Mbps: Write 2'b10 to 1.7:6 RATE_TX[1:0], write 2'b10 to 1.5:4 RATE_RX[1:0], write 4'b1110 to 1.3:0 PLL_MULT[3:0] to select QUARTER rate and 25x MPY (CHANNEL_CONTROL_1 = 0x01AE).
  - If serial data rate is 1228.80Mbps: Write 2'b10 to 1.7:6 RATE_TX[1:0], write 2'b10 to 1.5:4 RATE_RX[1:0], write 4'b1101 to 1.3:0 PLL_MULT[3:0] to select QUARTER rate and 20x MPY (CHANNEL_CONTROL_1 = 0x01AD).
  - If serial data rate is 768.00Mbps: Write 2'b11 to 1.7:6 RATE_TX[1:0], write 2'b11 to 1.5:4 RATE_RX[1:0], write 4'b1110 to 1.3:0 PLL_MULT[3:0] to select EIGHTH rate and 25x MPY (CHANNEL_CONTROL_1 = 0x01FE).
  - If serial data rate is 614.40Mbps: Write 2'b11 to 1.7:6 RATE_TX[1:0], write 2'b11 to 1.5:4

RATE_RX[1:0], write 4'b1101 to 1.3:0 PLL_MULT[3:0] to select EIGHTH rate and 20x MPY (CHANNEL_CONTROL_1 = 0x01FD).

- Serial Configuration
  - Configure the following bits per the desired application
    - 1.9:8 (LOOP_BANDWIDTH[1:0])
    - 2.12:8 (TWPOST1[4:0])
    - 2.7:4 (TWPRE[3:0])
    - 2.3:0 (SWING[3:0])
    - 8.14:12 (EQPRE[2:0])
    - 8.11:10 (CDRTHR[1:0]) = 2'b01
    - 8.9:8 (CDRFMULT[1:0]) = 2'b00
- Mode Control
  - Channel synchronization (comma enable) is on by default and the parallel output 9 bit codes are byte aligned.
  - Write 1'b1 to 3.3 ENCODE_ENABLE
  - Write 1'b1 to 3.2 DECODE _ENABLE
  - Set the DDR Source Aligned Mode
    - Write 1'b1 to 3.6 DDR_ENABLE
    - Write 1'b1 to 3.1 TX_EDGE_MODE to select Transmit DDR Source Aligned Mode
    - Write 1'b1 to 3.0 RX_EDGE_MODE to select Receive DDR Source Aligned Mode
- If a different parallel IO align mode used:
  - If SDR Falling Edge Aligned: write 0x018C to CHANNEL_CONTROL_3 register.
  - If SDR Rising Edge Aligned: write 0x018F to CHANNEL_CONTROL_3 register.
  - If DDR Source Centered: write 0x01CC to CHANNEL_CONTROL_3 register.
- Enable desired status signals to LOSA and LOSB for real time monitoring per channel. Any number of signals can be enabled at once.
  - If SERDES Rx Loss of Signal condition monitored: write 1'b1 to 6.10 LOS_OVERLAY.
  - If channel synchronization status monitored: write 1'b1 to 6.9 CH_SYNC_OVERLAY.
  - If PLL lock status monitored: write 1'b1 to 6.8 PLL_LOCK_OVERLAY.
  - If invalid code word status monitored: write 1'b1 to 6.3 INVALID_CODE_OVERLAY
  - If SERDES AGC unlock status monitored: write 1'b1 to 7.7 AGCLOCK_OVERLAY.
  - If SERDES AZDONE status monitored: write 1'b1 to 7.6 AZDONE_OVERLAY.
- Check SERDES PLL Status for Locked State
  - Poll 5.0 PLL_LOCK (per channel) until it is asserted (high).
- Toggle ENRX
  - Write 1'b0 to 20.2 (ENRX)
  - Write 1'b1 to 20.2 (ENRX)
- Final CDR Configuration
  - Wait until either AGC_LOCKED asserted or 250M UI
  - Write 8.9:8 (CDRFMULT[1:0]) = 2'b01
  - Poll 5.13 AGC_LOCKED (1'b1) (per channel)
- Issue Data path Reset
  - Write 1'b1 to 4.3 DATAPATH_RESET
- Clear Latched Registers
  - Read 5 CHANNEL_STATUS_1 to clear all (per channel)
  - Read 14.15:0 ERROR_COUNTER to clear (per channel)
- Device provisioning has completed at this point

- Periodically Check Device Operational Mode Status (Non-Errored Read Values Shown Below):
  - Read 5 CHANNEL_STATUS_1 and verify the following bits:
    - 5.14 AZ_DONE (1'b1) (per channel)
    - 5.13 AGC_LOCKED (1'b1) (per channel)
    - 5.9 ENCODE_INVALID (1'b0) (per channel)
    - 5.8 DECODE_INVALID (1'b0) (per channel)
    - 5.7 TX_FIFO_UNDERFLOW (1'b0) (per channel)
    - 5.6 TX_FIFO_OVERFLOW (1'b0) (per channel)
    - 5.5 RX_FIFO_UNDERFLOW (1'b0) (per channel)
    - 5.4 RX_FIFO_OVERFLOW (1'b0) (per channel)
    - 5.2 LOS (1'b0) (per channel). This read value is only useful if the serial input is guaranteed to be above 150mVdfpp.
    - 5.1 CHANNEL_SYNC (1'b1) (per channel)
    - 5.0 PLL_LOCK (1'b1) (per channel)
  - Read 14.15:0 ERROR_COUNTER[15:0] and verify it is 0 (per channel)

4.19 JITTER TEST PATTERN GENERATION AND VERIFICATION PROCEDURES

Use one of the following procedures to generate and verify the respective test patterns. It is assumed that an appropriate external cable has been connected between serial outputs and serial inputs. No external parallel side connections are necessary.

4.19.1 IEEE802.3 Clause 36A Based Continuous Random Pattern (CRPAT) Long/Short Test Pattern:

- Reset Device:
  - Issue a hard or soft reset (RESET_N asserted –or- Write 1 to 0.15 GLOBAL_RESET)
- Select SERDES Reference Clock Input:
  - If REFCLK_0_P/N used - Ensure REFCLK_A_SEL (or REFCLK_B_SEL if channel B is used) primary input pin is low
  - If REFCLK_1_P/N used - Ensure REFCLK_A_SEL (or REFCLK_B_SEL if channel B is used) primary input pin is high
- Ensure a legal reference clock operation frequency is selected based on Appendix B (Continuous Rate Device Configuration), and provision CHANNEL_CONTROL_1 register accordingly.
- Serial Configuration
  - Configure the following bits per the desired application:
    - 1.9:8 (LOOP_BANDWIDTH[1:0])
    - 2.12:8 (TWPOST1[4:0])
    - 2.7:4 (TWPRE[3:0])
    - 2.3:0 (SWING[3:0])
    - 8.14:12 (EQPRE[2:0])
    - 8.11:10 (CDRTHR[1:0]) = 2'b01
    - 8.9:8 (CDRFMULT[1:0]) = 2'b00
    - 1.3:0 PLL_MULT[3:0]
    - 1.7:6 RATE_TX[1:0] (CRPAT supported only in half/quarter/eighth rate modes
    - 1.5:4 RATE_RX[1:0] (CRPAT supported only in half/quarter/eighth rate modes).
- Check SERDES PLL Status for Locked State
  - Poll 5.0 PLL_LOCK (per channel) until it is asserted (high).
- Toggle ENRX
  - Write 1'b0 to 20.2 (ENRX)

  - Write 1’b1 to 20.2 (ENRX)
- Select Test Pattern:
  - If CRPAT Long Pattern is desired:
    - Write 3’b011 to 7.10:8 TEST_PATTERN_SEL[2:0]
  - If CRPAT Short Pattern is desired:
    - Write 3’b100 to 7.10:8 TEST_PATTERN_SEL[2:0]
- Enable Test Pattern Generation:
  - Write 1’b1 to 7.13 TP_GEN_EN
  - Poll 5.13 AGC_LOCKED (1’b1) (per channel)
- Final CDR Configuration
  - Wait until either AGC_LOCKED asserted or 250M UI
  - Write 8.9:8 (CDRFMULT[1:0]) = 2’b01
  - Poll 5.13 AGC_LOCKED (1’b1) (per channel)
- Issue Data path Reset
  - Write 1’b1 to 4.3 DATAPATH_RESET
- Enable Test Pattern Verification:
  - Write 1’b1 to 7.12 TP_VERIFY_EN
- Clear Counters:
  - Read 14.15:0 ERROR_COUNTER[15:0] and discard the value.
- Verify Test In Progress:
  - Poll 5.12 TP_STATUS until asserted.
- The pattern verification is now in progress.
- Verify Error Free Operation (as many times as desired during the duration of the test period):
  - Read 14.15:0 ERROR_COUNTER[15:0], and verify 16’h0000 is read to confirm error free operation.

If more than one test is specified results are unpredictable.

If another test type is desired, begin at the first step of that procedure.

4.19.2 PRBS TEST GENERATION AND VERIFICATION PROCEDURES

Use one of the following procedures to generate and verify the respective PRBS test patterns. It is assumed that an appropriate external cable has been connected between serial outputs and serial inputs. No external parallel side connections are necessary.

4.19.2.1 2^7-1 / 2^{23}-1 / 2^{31}-1 PRBS Register Based Testing

- Note: PRBS TX does not support eighth rate mode.
- Reset Device:
  - Issue a hard or soft reset (RESET_N asserted -or- Write 1 to 0.15 GLOBAL_RESET)
- Select SERDES Reference Clock Input:
  - If REFCLK_0_P/N used – Ensure REFCLK_A_SEL (or REFCLK_B_SEL if channel B is used) primary input pin is low
  - If REFCLK_1_P/N used – Ensure REFCLK_A_SEL (or REFCLK_B_SEL if channel B is used) primary input pin is high
- Ensure a legal reference clock operation frequency is selected based on Appendix B (Continuous Rate Device Configuration), and provision CHANNEL_CONTROL_1 register accordingly. **(Note: Eighth Rate TX Is Not Supported)**.
- Serial Configuration
  - Configure the following bits per the desired application:
    - 1.9:8 (LOOP_BANDWIDTH[1:0])
    - 2.12:8 (TWPOST1[4:0])
    - 2.7:4 (TWPRE[3:0])
    - 2.3:0 (SWING[3:0])
    - 8.14:12 (EQPRE[2:0])
    - 8.11:10 (CDRTHR[1:0]) = 2'b01
    - 8.9:8 (CDRFMULT[1:0]) = 2'b00
    - 1.3:0 PLL_MULT[3:0]
    - 1.7:6 RATE_TX[1:0]
    - 1.5:4 RATE_RX[1:0]
- Check SERDES PLL Status for Locked State
  - Poll 5.0 PLL_LOCK (per channel) until it is asserted (high).
- Toggle ENRX
  - Write 1'b0 to 20.2 (ENRX)
  - Write 1'b1 to 20.2 (ENRX)
- Select Test Pattern:
  - If 2^7-1 PRBS Pattern is desired:
    - Write 3'b101 to 7.10:8 TEST_PATTERN_SEL[2:0]
  - If 2^{23}-1 PRBS Pattern is desired:
    - Write 3'b110 to 7.10:8 TEST_PATTERN_SEL[2:0]
  - If 2^{31}-1 PRBS Pattern is desired:
    - Write 3'b111 to 7.10:8 TEST_PATTERN_SEL[2:0]
- Enable Test Pattern Generation:
  - Write 1'b1 to 7.13 TP_GEN_EN
- Final CDR Configuration
  - Wait until either AGC_LOCKED asserted or 250M UI
  - Write 8.9:8 (CDRFMULT[1:0]) = 2'b01
  - Poll 5.13 AGC_LOCKED (1'b1) (per channel)
- Issue Data path Reset

  - Write 1’b1 to 4.3 DATAPATH_RESET
- Enable Test Pattern Verification:
  - Write 1’b1 to 7.12 TP_VERIFY_EN
- The pattern verification is now in progress.
- PRBSA_PASS contains a real time output that when low indicates the input PRBS pattern on RXAP/N contains error.
- PRBSB_PASS contains a real time output that when low indicates the input PRBS pattern on RXBP/N contains error.
- The following steps can be performed if the number of errors needs to be monitored:
  - Read 14.15:0 ERROR_COUNTER[15:0] and discard the value.
  - Read 14.15:0 ERROR_COUNTER[15:0], and verify 16’h0000 is read to confirm error free operation. (as many times as desired during the duration of the test period)

4.19.2.2 2^7-1 / 2^{23}-1 / 2^{31}-1 PRBS Pin Based Testing

- Note: PRBS TX does not support eighth rate mode.
- Device Pin Setting(s):
  - Ensure PRBS_EN primary input pin is high.
  - PRBS Selection
    - PRBS 2^{31}-1 will be selected by default.
- Reset Device:
  - Issue a hard or soft reset (RESET_N asserted –or- Write 1 to 0.15 GLOBAL_RESET)
- Select SERDES Reference Clock Input:
  - If REFCLK_0_P/N used - Ensure REFCLK_A_SEL (or REFCLK_B_SEL if channel B is used) primary input pin is low
  - If REFCLK_1_P/N used - Ensure REFCLK_A_SEL (or REFCLK_B_SEL if channel B is used) primary input pin is high
- Ensure a legal reference clock operation frequency is selected based on Appendix B (Continuous Rate Device Configuration), and provision CHANNEL_CONTROL_1 register accordingly. **(Note: Eighth Rate TX Is Not Supported).**
- Serial Configuration
  - Configure the following bits per the desired application:
    - 1.9:8 (LOOP_BANDWIDTH[1:0])
    - 2.12:8 (TWPOST1[4:0])
    - 2.7:4 (TWPRE[3:0])
    - 2.3:0 (SWING[3:0])
    - 8.14:12 (EQPRE[2:0])
    - 8.11:10 (CDRTHR[1:0]) = 2’b01
    - 8.9:8 (CDRFMULT[1:0]) = 2’b00
    - 1.3:0 PLL_MULT[3:0]
    - 1.7:6 RATE_TX[1:0]
    - 1.5:4 RATE_RX[1:0]
- Check SERDES PLL Status for Locked State
  - Poll 5.0 PLL_LOCK (per channel) until it is asserted (high).
- Toggle ENRX
  - Write 1’b0 to 20.2 (ENRX)
  - Write 1’b1 to 20.2 (ENRX)
- Select Test Pattern if either 2^7-1 or 2^{23}-1 PRBS Pattern is desired. Skip this step if 231-1 PRBS Pattern is desired.

  - If 2^7-1 PRBS Pattern is desired:
    - Write 3'b101 to 7.10:8 TEST_PATTERN_SEL[2:0]
  - If 2^{23}-1 PRBS Pattern is desired:
    - Write 3'b110 to 7.10:8 TEST_PATTERN_SEL[2:0]
- Final CDR Configuration
  - Wait until either AGC_LOCKED asserted or 250M UI
  - Write 8.9:8 (CDRFMULT[1:0]) = 2'b01
  - Poll 5.13 AGC_LOCKED (1'b1) (per channel)
- Issue Data path Reset
  - Write 1'b1 to 4.3 DATAPATH_RESET
- The pattern verification is now in progress.
- PRBSA_PASS contains a real time output that when low indicates the input PRBS pattern on RXAP/N contains error.
- PRBSB_PASS contains a real time output that when low indicates the input PRBS pattern on RXBP/N contains error.
- The following steps can be performed if the number of errors needs to be monitored:
  - Read 14.15:0 ERROR_COUNTER[15:0] and discard the value.
  - Read 14.15:0 ERROR_COUNTER[15:0], and verify 16'h0000 is read to confirm error free operation. (as many times as desired during the duration of the test period)

4.20 PACKAGE DISSIPATION RATINGS

The following tables detail the thermal characteristics of the TLK6002 package.

Table 4-2. Package Thermal Characteristics

PARAMETER		JEDEC STANDARD BOARD	CUSTOM TYPICAL APPLICATION BOARD
		VALUE	VALUE
θ_{JA}	Theta-JA	24.3	19.2
θ_{JB}	Theta-JB	11.6	11.6
θ_{JC}	Theta-JC	4.5	4.5
Ψ_{JT}	Psi-JT	4.5	4.5
ψ_{JB}	Psi-JB	11.5	11.3

Note: Custom Typical Application Board Characteristics:

- 10 x 15 inches
- 12 layer
  - 8 power/ground layers – 95% copper (1oz)
  - 4 signal layers – 20% copper (1oz)

$\Psi_{JB} = (T_J – T_B)/(\text{Total Device Power Dissipation})$

T_J = Device Junction Temperature

T_B = Temperature of PCB 1mm from device edge.

$\Psi_{JT} = (T_J – T_C)/(\text{Total Device Power Dissipation})$

T_J = Device Junction Temperature

T_C = Hottest temperature on the case of the package

4.21 Device Total Worst Case Power Dissipation

The following table details the worst case total device power dissipation:

Table 4-3. Device Worst Case Total Power Dissipation

	VDDQA/B, VDDRA/B, VDDO1/2/3 = 1.6V			VDDQA/B, VDDRA/B, VDDO1/2/3 = 1.9V		
	HSTL Input Termination			HSTL Input Termination		
Serial Rate (Gbps)	Disabled (6.1:0 = 2'b00)	Half Strength (6.1:0 = 2'b01)	Full Strength (6.1:0 = 2'b1x)	Disabled (6.1:0 = 2'b00)	Half Strength (6.1:0 = 2'b01)	Full Strength (6.1:0 = 2'b1x)
0.47	552	994	1322	674	1301	1775
0.6144	596	1024	1351	727	1348	1813
0.768	653	1067	1395	781	1395	1864
1.2288	677	1065	1371	834	1389	1842
1.536	750	1129	1443	906	1462	1889
2.4576	829	1162	1440	1032	1498	1898
3.072	917	1225	1499	1131	1574	1954
4.9512	975	1245	1507	1210	1612	1952
6.144	1046	1315	1562	1305	1690	2038
6.25	1057	1320	1580	1286	1696	2064

The test conditions for above data are: two channels active in transceiver mode, parallel/serial loopback connections installed external to the device, CRPAT Long data pattern, all unlisted power supplies at 1.05V, and T=85C.

Device Errata:

If VDDQ power supply ramp leads DVDD, the following items must be noted:

1. Register 0x0F usage is not possible
2. CS_N/GPI1/SDI/SDO/DCI signals are not usable (left unconnected)
3. Register 28.14 must be asserted manually for CLK_OUT_P/N normal operation

5 Appendix A – Application Board Supply Recommendations

Nominal Board Voltages Required: 1.0V, and either 1.5 or 1.8V

Ground - Connect all device grounds together on the application board (DGND, AGND)

1.0V – Bulk Decoupled

1. Ferrite Bead → DVDD (Locally Decoupled)
2. Ferrite Bead → AVDD / VDDT / VDDD (Locally Decoupled)

1.5V or 1.8V – Bulk Decoupled

1. Ferrite Bead → VDDQA/B (Locally Decoupled)
2. Ferrite Bead → VDDRA,VDDRB (Separate, Locally Decoupled)
3. Ferrite Bead → VDDO1,VDDO2,VDDO3 (Locally Decoupled)

VREF* can be generated using 1k resistors between VDDQA/B and DGND, and should be locally decoupled.

Note: Ferrite beads should have high impedance near the fundamental frequency that the parallel data is running at.

Note: Bulk decoupling prior to the ferrite beads required in order to decouple noise from power source. This decoupling will be determined by your power source and what frequencies of noise it creates.

Note: For close to device localized decoupling (after ferrite beads), 1.0µF and 0.1µF caps should be placed on the pins of the device on the back side of the board.

It is strongly recommended that TI review relevant pages of your application board schematics and layout before fabrication to ensure first pass success.

6 Appendix B – Continuous Rate Device Configuration

The REFCLK needed based on a particular SERDES configuration is as follows:

SERDES Reference Clock = (Rate Scale) × (Serial Bit Rate) / (Serdes Multiplier)

Note that Table 6-1 indicates legal ranges for each setting.

Table 6-1. Continuous Rate SERDES Configuration Settings

	SERDES Serial Rate Configuration											
	SERDES Reference Clock				Serial Rate (Gbps)							
SERDES Multiplier	Period (ns)		Frequency (MHz)		Full		Half		Quarter		Eighth	
	Min	Max	Max	Min	Max	Max	Min	Max	Max	Min	Max	Max
4	1.25	2.14	800	467	3.74	6.25	1.87	3.20	0.93	1.60	0.47	0.80
5	1.33	2.67	752	375	3.75	6.25	1.87	3.76	0.94	1.88	0.47	0.94
6	1.6	3.2	625	313	3.75	6.25	1.88	3.75	0.94	1.88	0.47	0.94
8	2.13	4.26	469	235	3.76	6.25	1.88	3.76	0.94	1.88	0.47	0.94
8.25	2.19	4.4	457	227	3.75	6.25	1.88	3.77	0.94	1.88	0.47	0.94
10	2.67	5.33	375	188	3.75	6.25	1.88	3.75	0.94	1.87	0.47	0.94
12	3.2	6.4	313	156	3.75	6.25	1.88	3.75	0.94	1.88	0.47	0.94
15	4	8.14	250	122.88	3.69	6.25	1.84	3.75	0.92	1.88	0.46	0.94
16	4.25	8.14	235	122.88	3.93	6.25	1.97	3.76	0.98	1.88	0.49	0.94
16.5	4.39	8.14	228	122.88	4.06	6.25	2.03	3.76	1.01	1.88	0.51	0.94
20	5.33	8.14	188	122.88	4.92	6.25	2.46	3.75	1.23	1.88	0.61	0.94
25	6.67	8.14	150	122.88	6.14	6.25	3.07	3.75	1.54	1.87	0.77	0.94
Note: In Full Rate Mode, the SERDES Reference Clock range shown above must be limited such that serial side operation does not exceed 6.25 Gbps.												
Rate Scale					Full		Half		Quarter		Eighth	
					0.5		1		2		4	

Serial performance is optimal when the highest reference clock and lowest SERDES multiplier is chosen for a given application rate.

7 Appendix C – 8b/10B Control Characters Supported

Table 7-1 contains 8b/10b control characters are valid and are supported in TLK6002.

The K28.7 usage is not advised as comma characters can be created on non-symbol boundaries without depending upon adjacent characters.

Further detail on 8b/10b encoding/decoding of data characters can be found in IEEE802.3-2002 Clause 36.

Table 7-1. 8b/10b Control Characters Supported

CONTROL CHARACTER	DATA BYTE	CONTAINS COMMA CHARACTER
K28.0	0x1C	
K28.1	0x3C	Y
K28.2	0x5C	
K28.3	0x7C	
K28.4	0x9C	
K28.5	0xBC	Y
K28.6	0xDC	
K28.7	0xFC	Y
K23.7	0xF7	
K27.7	0xFB	
K29.7	0xFD	
K30.7	0xFE	

8 Appendix D – Device Latency Specification

The following tables show the absolute device latency in each operation mode.

Table 8-1. Device Absolute Transmit Latency – SDR and DDR Modes

SDR TRANSMIT ABSOLUTE LATENCY (Serial Bit Times)				
Note: TX FIFO, in register 6.14:12, defaults to Auto Selection Mode. This table contains latencies when the TX FIFO is set in the minimum latency mode (6.14:12 = 3'b000).				
LATENCY COMPONENTS				
Item	**Minimum**	**Maximum**	**Description**	
A	8	12	Sampling edge of TXCLK_* to TX FIFO Input Register	
B	10	40	TX FIFO Input Register to TX FIFO Output Register	
C	20	20	TX FIFO Output Register to 8b/10b Encoder Register	
D	10	10	8b/10b Encoder Register to PMA Retime Register	
E	20	20	PMA Retime Register to TX SERDES Input Register	
F	16	22	TX SERDES Input Register to Serialized Output Bit	
Bit Detail	**Latency**	**Minimum**	**Maximum**	Assumption: TX*_[19] is first transmitted bit. TX*_[19:10] is first transmitted symbol. 8b/10b encoder is enabled. Disabling 8b/10b encoder reduces latency by 10 bit times.
TX*_[19]	0	84	124	
TX*_[10]	9	93	133	
TX*_[9]	10	94	134	
TX*_[0]	19	103	143	

Latency Summary	**Encoder Enabled**		**Encoder Disabled**	
	Minimum	**Maximum**	**Minimum**	**Maximum**
TX*_[19]	84	124	74	114
TX*_[10]	93	133	83	123
TX*_[9]	94	134	84	124
TX*_[0]	103	143	93	133

DDR TRANSMIT ABSOLUTE LATENCY (Serial Bit Times)				
DDR Transmit Latency is the same as transmit SDR mode, except that all numbers are 8 to12 bit times larger.				
Latency Summary	**Encoder Enabled**		**Encoder Disabled**	
	Minimum	**Maximum**	**Minimum**	**Maximum**
TX*_[19]	92	136	82	126
TX*_[10]	101	145	91	135
TX*_[9]	102	146	92	136
TX*_[0]	111	155	101	145

Table 8-2. Device Absolute Receive Latency – SDR and DDR Modes

RX SDR/DDR RECEIVE ABSOLUTE LATENCY								
Note: RX FIFO Depth (When FIFO Enabled) is 4 words.								
Latency Components								
Item	**Minimum**	**Maximum**	**Description**					
A	47	57	Serial Input Bit to RX SERDES Output Register					
B	10	10	RX SERDES Output Register to RX PMA Register					
C	10	10	RX PMA Register to Channel Sync Input Register					
D	10	20	Channel Sync Input Register to Channel Sync Output Register					
E	10	10	Channel Sync Output Register to 8b/10b Decoder Input Register					
F	10	10	8b/10b Decoder Input Register to 8b/10b Output Register					
G	10	10	8b/10b Output Register to RX FIFO Input Register					
H	10	40	RX FIFO Input Register to RX FIFO Output Register					
I	10	20	RXFIFO Output Register to RX Parallel Output Register Driven					
Bit Detail	Latency	Minimum	Maximum	Assumption: RX*_[10 and 0] are the first received bits.				
RX*_[19]	0	127	187					
RX*_[10]	9	136	196					
RX*_[9]	0	127	187					
RX*_[0]	9	136	196					
Disabling Channel Synchronization Reduces Above Numbers by 20 Minimum and 30 Maximum bit times.								
Disabling Decoder Reduces Above Numbers by 20 bit times.								
Bypassing RX FIFO Reduces Above Numbers by 20 Minimum and 50 Maximum bit times.								
Latency Summary	RX FIFO Bypassed		RX FIFO Bypassed		RX FIFO Bypassed		RX FIFO Enabled	
	Channel Sync On		Channel Sync On		Channel Sync Off		Channel Sync On	
	8b/10b Decoder On		8b/10b Decoder Off		8b/10b Decoder Off		8b/10b Decoder On	
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum
RX*_[19]	107	137	87	117	67	87	127	187
RX*_[10]	116	146	96	126	76	96	136	196
RX*_[9]	107	137	87	117	67	87	127	187
RX*_[0]	116	146	96	126	76	96	136	196

Table 8-3 show the static latency variance. Note that static latency variation is the difference in absolute latency values possible across device reset/power ups.

Table 8-3. Device Static Latency Variance

TRANSMIT STATIC LATENCY VARIANCE – Maximum		
8b/10b Encoder	**Interface Mode**	**Serial Bit Times**
Enabled	SDR	33
Enabled	DDR	33
Disabled	SDR	33
Disabled	DDR	33
Note: TX_FIFO_DEPTH[2:0] = 3'b000		

RECEIVE STATIC LATENCY VARIANCE – Maximum			
Receive FIFO	**Channel Synchronization**	**8b/10b Decoder**	**Serial Bit Times**
Bypassed	Enabled	Enabled	30
Bypassed	Enabled	Disabled	30
Bypassed	Disabled	Disabled	20
Enabled	Enabled	Enabled	60

Table 8-4 shows the device dynamic latency variance. Note that the dynamic latency variation is the difference in latency when voltage and temperature are varied for a particular absolute static latency, after traffic (including channel synchronization) has been established. The dynamic latency variance numbers do not include phase movement between the parallel input clocks and input reference clocks.

Table 8-4. Device Dynamic Latency Variance

Transmit Dynamic Latency Variance			Receive Dynamic Latency Variance	
Minimum	Maximum		Minimum	Maximum
0 ns	2 ns		0 ns	2 ns

9 Appendix E – Device Test Modes

This device can be placed into one of the four modes: functional mode including JTAG testing mode, scan 1 testing mode, scan 2 testing mode, and Cooper/eFuse testing mode. The scan 1, scan 2 and Cooper/eFuse testing modes are for TI use only, and may be ignored by external users of this device.

Table 9-1. Device Mode Configuration

FUNCTIONAL DEVICE PIN NAME	FUNCTIONAL MODE/JTAG TESTING	SCAN 1 MODE	SCAN 2 MODE	COOPER/EFUSE MODE
TESTEN	0	0	1	1
GPI0	0	1	0	1

Table 9-2. Device Test Mode Pin Configuration

FUNCTIONAL DEVICE PIN NAME	FUNCTIONAL MODE SIGNAL DIRECTION	TEST MODE SIGNAL DIRECTION	FUNCTIONAL MODE/JTAG TESTING	SCAN 1 MODE	SCAN 2 MODE	COOPER/EFUSE MODE
CODEA_EN	I	I	CODEA_EN	Scan In 8	Scan In 8	STCICFG0
RATE_A2	I	I	RATE_A2	Scan In 7	Scan In 7	STCI_D
RATE_A1	I	I	RATE_A1	Scan In 6	Scan In 6	EFUSE_TMS
RATE_A0	I	I	RATE_A0	Scan In 5	Scan In 5	EFUSE_TDI
RATE_B2	I	I	RATE_B2	Scan In 4	Scan In 4	STCICFG1
RATE_B1	I	I	RATE_B1	Scan In 3	Scan In 3	EFUSE_INITZ
RATE_B0	I	I	RATE_B0	Scan In 2	Scan In 2	EFUSE_TRST
REFCLK_A_SEL	I	I	REFCLK_A_SEL	Scan In 1	Scan In 1	REFCLK_A_SEL
REFCLK_B_SEL	I	I	REFCLK_B_SEL	Scan Enable	Scan Enable	REFCLK_B_SEL
CLK_OUT_SEL	I	I	CLK_OUT_SEL	At Speed Scan Enable 0: stuck-at fault 1: transition fault	HSTL Force Up	EFUSE_TCK
CODEB_EN	I	I	CODEB_EN	Scan Clock Select (0: from device pin, 1: from Cooper), also EFUSE_SYS_CLK	HSTL Force Down	EFUSE_SYS_CLK
TDI	I	I	TDI	Adaptive Scan Enable (Test Mode)	Adaptive Scan Enable (Test Mode)	TDI
PRBS_EN	I	I	PRBS_EN	Scan Clock	Scan Clock	STCICLK
PRTAD4	I	O or I	PRTAD4	Scan Out 8 (O)	Scan Out 8 (O)	TESTCLK_R (I)
PRTAD3	I	O or I	PRTAD3	Scan Out 7 (O)	Scan Out 7 (O)	efuse_cooper_sel (I) (0: Cooper mode, 1: eFuse mode)
PRTAD2	I	O or I	PRTAD2	Scan Out 6 (O)	Scan Out 6 (O)	TESTCLK_T (I)
PRTAD1	I	O or I	PRTAD1	Scan Out 5 (O)	Scan Out 5 (O)	Not Used (I)
PRTAD0	I	O or I	PRTAD0	Scan Out 4 (O)	Scan Out 4 (O)	Not Used (I)
PRBSA_PASS	O	O	PRBSA_PASS	Scan Out 3 (O)	Scan Out 3 (O)	Tied Low
LOSA	O	O	LOSA	Scan Out 2 (O)	Scan Out 2 (O)	STCI_Q
PRBSB_PASS	O	O	PRBSB_PASS	Scan Out 1 (O)	Scan Out 1 (O)	EFUSE_TDO
LOSB	O	O	LOSB	Burnin_Output	Burnin_Output	Burnin_Output

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2010) to A Revision ..... **Page**

- Changed SPI_CONTROL_STATUS table to TI_RESERVED_CONTROL STATUS 56
- Changed table 3-33, TI_RESERVED_CONTROL_8, to TI_CONTOL_8 59
- Changed bit 28.14 in TI_CONTROL_8 table 59
- Changed Device Initialization section 76

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK6002ZEU	ACTIVE	BGA	ZEU	324	84	RoHS & Green	SNAGCU	Level-4-260C-72 HR	-40 to 85	TLK6002	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

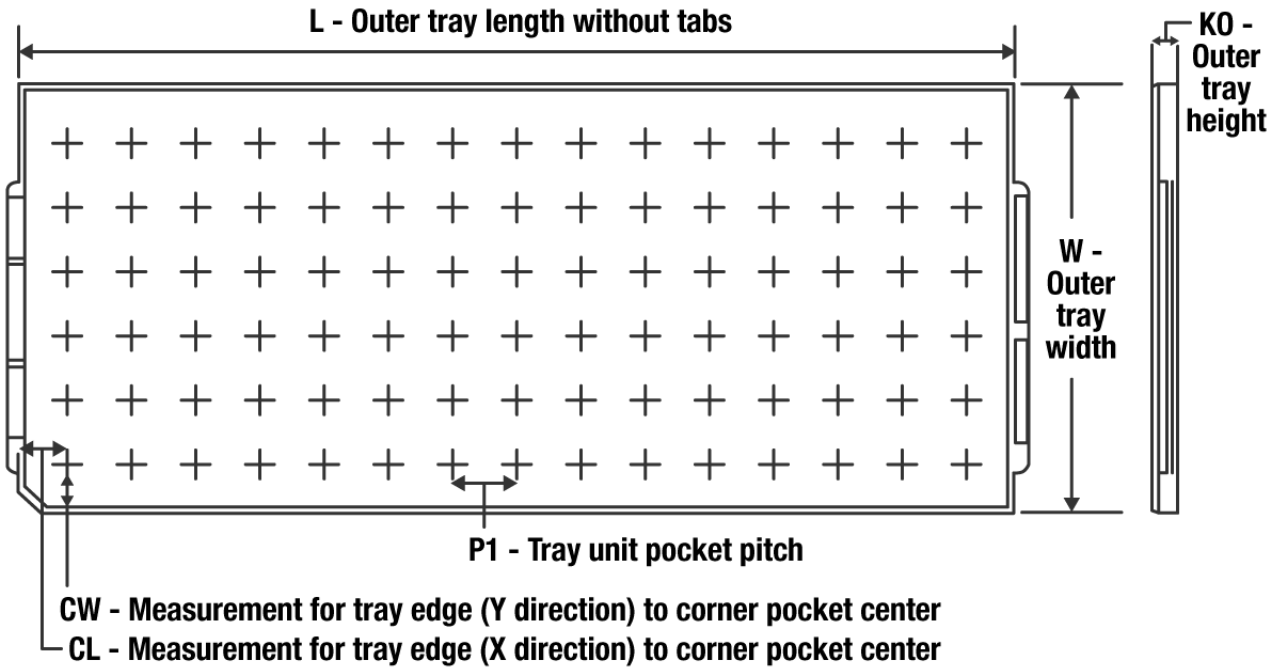
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY

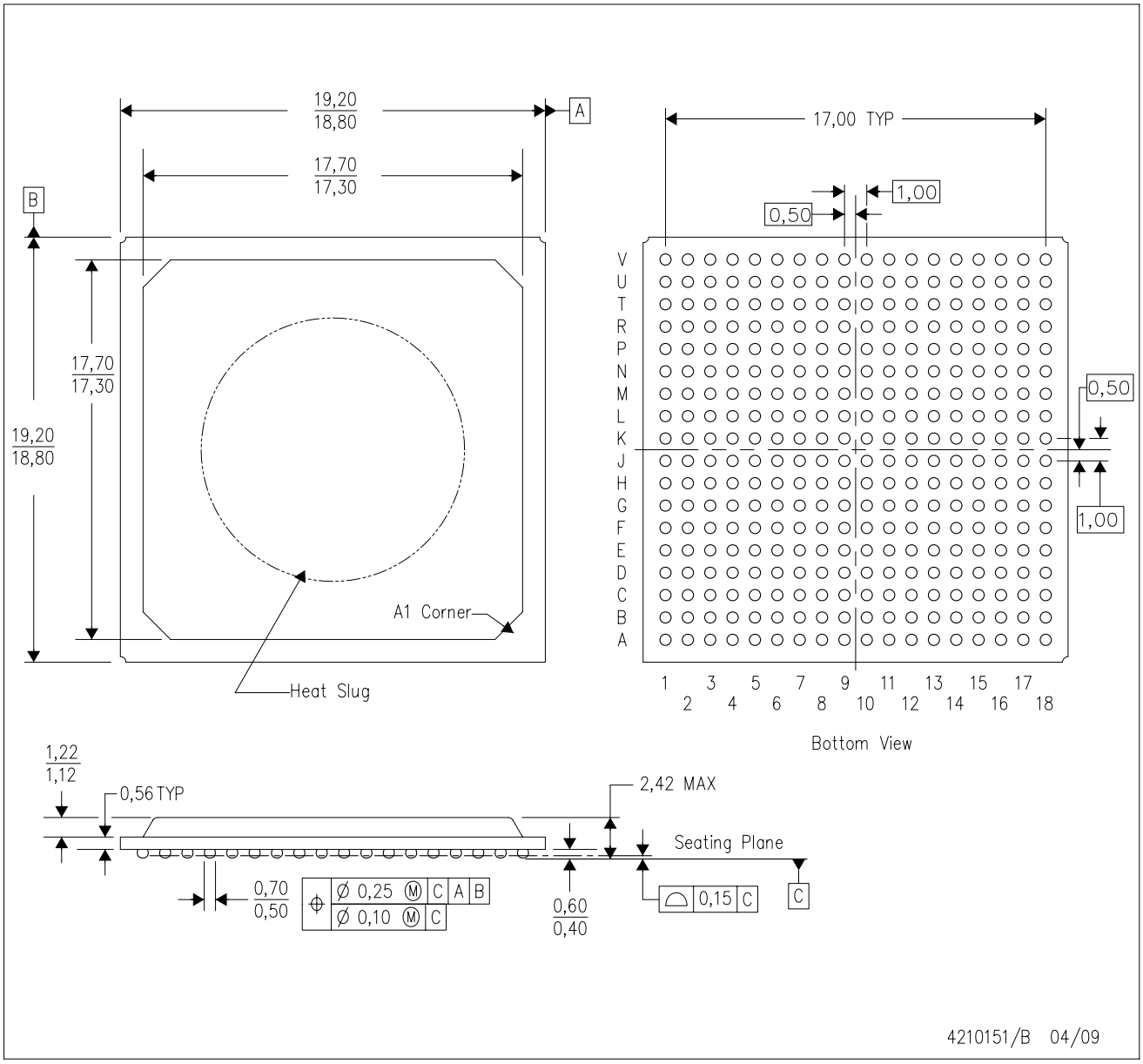


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TLK6002ZEU	ZEU	BGA	324	84	6X14	150	315	135.9	7620	21.34	18.79	14.6

ZEU (S–PBGA–N324) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package with heat slug (HSL).
D. This is a Pb–free solder ball design

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