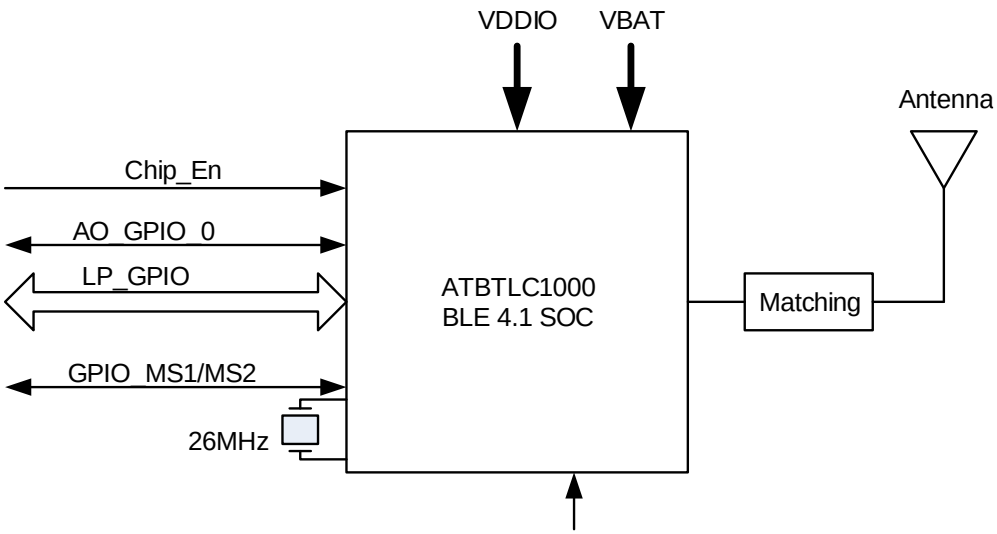
ATBTLC1000 Hardware Design Guidelines

Ultra Low Power BLE 4.1 SoC

USER GUIDE



Block Diagram

Introduction

This document details the hardware design guidelines for a customer to design the Atmel® ATBTLC1000 IC onto their board.

Table of Contents

1 Reference Schematic

1.1 Schematic

Figure 1-1 shows the reference schematic for a system using the ATBTLC1000.

Figure 1-1. Reference Schematic

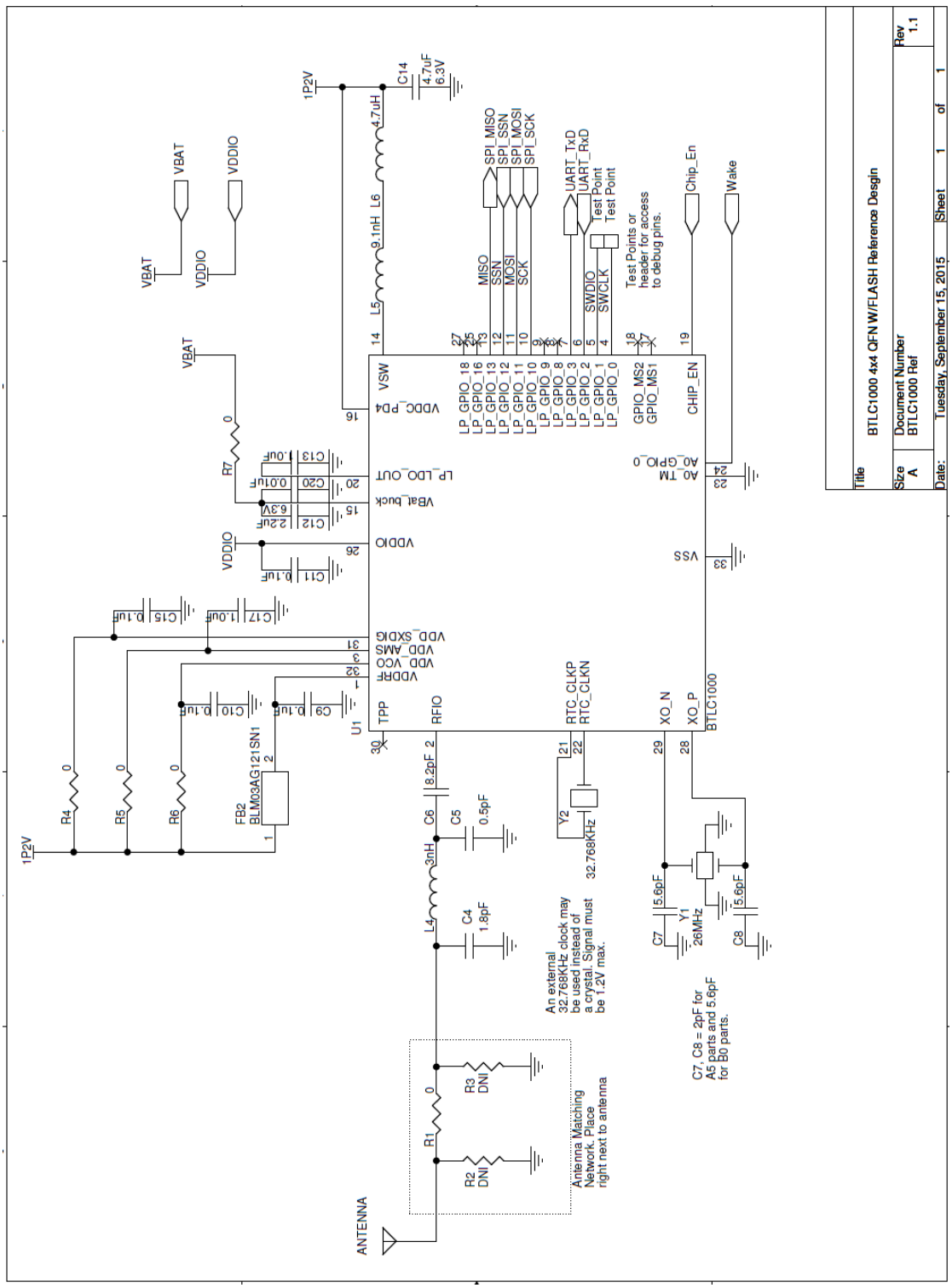


Figure 1-2 shows the Bill of Materials for the schematic.

Figure 1-2. Bill of Materials

BTLC1000 4x4 QFN W/FLASH Reference Desgin Revised: Tuesday, September 15, 2015
BTLC1000 Ref Revision: 1.1

Bill Of Materials September 15,2015 11:40:06

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	1	ANTENNA		Antenna,2.4-2.5GHz, 50ohm, -40 - +85C			
2	1	C4	1.8pF	CAP,CER,1.8pF,+/-0.1pF,NPO,0201,25V,-55-125C	TDK	C0603C0G1E1R8C	0201
3	1	C5	0.5pF	CAP,CER,0.5pF,+/-0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1ER50BA0	0201
4	1	C6	8.2pF	CAP,CER,8.2pF,+/-0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1E8R2DDC1	0201
5	2	C7,C8	5.6pF	CAP,CER,5.6pF,+/-0.5pF,NPO,0201,25V,-55-125C	TDK	C0603C0G1E5R6D030BA	0201
6	3	C9,C10,C15	0.1uF	CAP,CER,0.1uF,10%,X5R,0201,6.3V,-55-85C	Murata	GRM033R60J104KE19D	0201
7	1	C11	0.1uF	CAP,CER,0.1uF,10%,X5R,0201,6.3V,-55-125C	Murata	GRM033R60J104KE19D	0201
8	1	C12	2.2uF	CAP,CER,2.2uF,10%,X5R,0402,6.3V,-55-85C	TDK	C1005X5R0J225K	0402
9	1	C13	1.0uF	CAP,CER,1.0uF,20%,X5R,0201,6.3V,-55-85C	TDK	C0603X5R0J105M030BC	0201
10	1	C14	4.7uF	CAP,CER,4.7uF,10%,X5R,0402,6.3V,-55-85C	TDK	C1005X5R0J475K050BC	0402
11	1	C17	1.0uF	CAP,CER,1.0uF,20%,X6S,0201,4V,-55-85C	Murata	GRM033C80G105MEA2D	0201
12	1	C20	0.01uF	CAP,CER,0.01uF,10%,X5R,0201,10V,-55-125C	Murata	GRM033R61A103KA01D	0201
13	1	FB2	BLM03AG121SN1	FERRITE,120 OHM @100MHz,200mA,0201,-55-125C	Murata	BLM03AG121SN1	0201
14	1	L4	3nH	Inductor,3nH,+/-0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C	Taiyo Yuden	HKQ06033S3N0C-T	0201
15	1	L5	9.1nH	INDUCTOR,Multilayer,9.1nH,5%,300mA,0.32 ohmsQ=8@100MHz,-55C-125C,0402	Murata	LQG15HS9N1J02D	0402
16	1	L6	4.7uH	INDUCTOR,unshielded,4.7uH,20%,120mA Saturation,0.5ohms,SRF=80MHz,0603,-55-125C	TDK	MLZ1608M4R7WT000	0603
17	5	R1,R4,R5,R6,R7	0	RESISTOR,Thick Film,0 ohm,0201	Panasonic	ERJ-1GN0R00C	0201
18	2	R2,R3	DNI	RESISTOR,Thick Film,0 ohm,0201	Panasonic	ERJ-1GN0R00C	0201
19	2	TP1,TP2	Test Point	Test Point,Surface Mount,0.040"sq w/0.25"hole		40X40_SM_TEST_POINT	0.04"SQx0.025"H
20	1	U1	BTLC1000	IC, BLE, 32QFN	Atmel	BTLC1000	32QFN
21	1	Y1	26MHz	CRYSTAL,26MHz,CL=8pF,20ppm temp.,-40-85C,ESR=80,2.5x2mm	Taitien	A0183-X-001-3	2.5x2.0mm
22	1	Y2	32.768KHz	Crystal, 32.768KHz,+/-20ppm,-40-+85C,CL=7pF, 2 lead, SM	ECS	ECS-.327-7-34B-TR	

2 Notes on Interfacing to the ATBTLC1000

2.1 Programmable Pull-up Resistors

The ATBTLC1000 provides programmable pull-up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused module pin on the ATBTLC1000 should leave these pull-up resistors enabled so the pin will not float. The default state at power up is for the pull-up resistor to be enabled. However, any pin which is used should have the pull-up resistor disabled. The reason for this is that if any pins are driven to a low level while the ATBTLC1000 is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the device. Since the value of the pull-up resistor is approximately 100kΩ, the current through any pull-up resistor that is being driven low will be VDDIO/100K. For VDDIO = 3.3V, the current through each pull-up resistor that is driven low would be approximately 3.3V/100kΩ = 33µA. Pins which are used and have had the programmable pull-up resistor disabled, should always be actively driven to either a high or low level and not be allowed to float.

See the ATBTLC1000 Programming Guide for information on enabling/disabling the programmable pull up resistors.

2.2 Using an External RTC

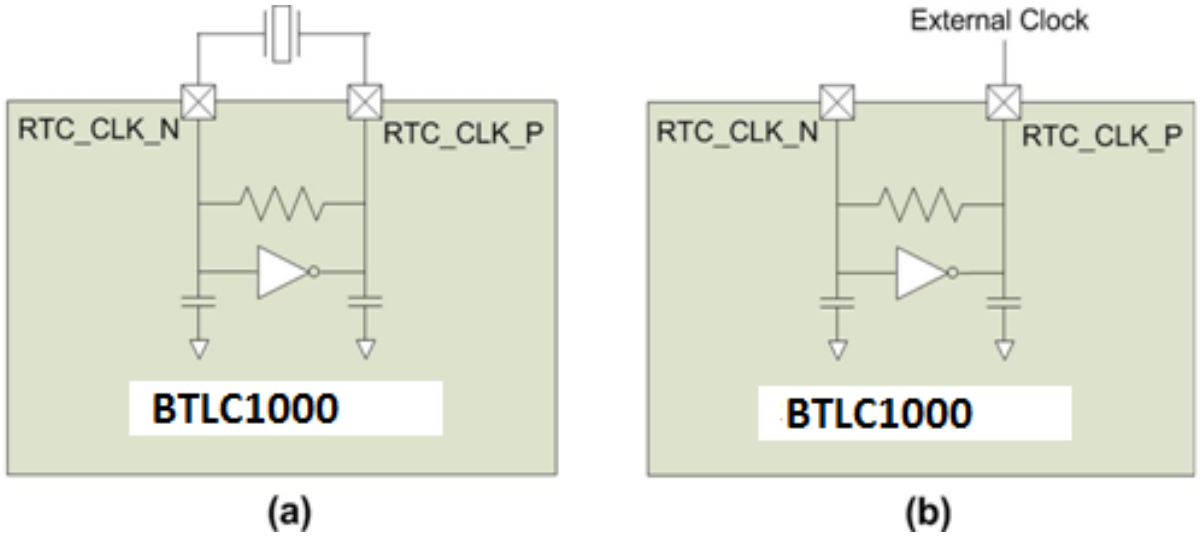
The ATBTLC1000 requires a 32.768kHz clock. This can be supplied by connecting a 32.768kHz crystal to the RTC_CLKP and RTC_CLKN pins as shown in the reference schematic. Alternatively, if a 32.768kHz clock is already available in the system (from a host MCU, for example), this clock can be used thereby saving the cost of the crystal. To use the external clock, connect it to the RTC_CLKP pin of the ATBTLC1000 device.

The block diagram in Figure 2-1(a) shows how the internal low frequency Crystal Oscillator (XO) is connected to the external crystal.

Typically, the crystal should be chosen to have a load capacitance of 7pF to minimize the oscillator current. The ATBTLC1000 device has switchable on chip capacitance that can be used to adjust the total load the crystal sees to meet its load capacitance specification. Refer to the ATBTLC1000 QFN SoC datasheet for more information.

Alternatively, if an external 32.768kHz clock is available, it can be used to drive the RTC_CLKP pin instead of using a crystal. The XO has 5.625F internal capacitance on the RTC_CLKP pin. To bypass the crystal oscillator an external signal capable of driving 5.625pF can be applied to the RTC_CLK_P terminal as shown in Figure 2-1(b). This signal must be 1.2V maximum. RTC_CLK_N must be left unconnected when driving an external source into RTC_CLK_P.

Figure 2-1. ATBTLC1000 XO Connections to Low Frequency Crystal Oscillator



(a) Crystal Oscillator is used

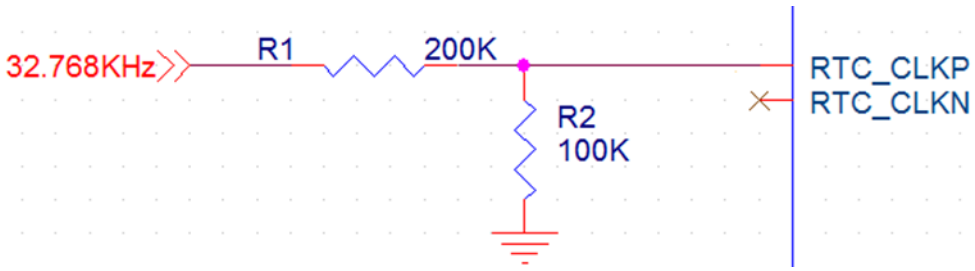
(b) Crystal Oscillator is bypassed

Table 2-1. ATBTLC1000 32.768kHz External Clock Specification

Parameter	Min.	Typ.	Max.	Unit	Comments
Oscillation frequency		32.768		KHz	Must be able to drive 6pF load @ desired frequency
VinH	0.7		1.2	V	High level input voltage
VinL	0		0.2	V	Low level input voltage
Stability – Temperature	-250		+250	ppm	

Note that the maximum voltage into the RTC_CLK pin is 1.2V. If the clock source provides a larger swing than this, it must be reduced before being introduced into the RTC_CLK pin. This can be accomplished with a simple resistor divider. Figure 2-2 shows an example of a resistor divider used to reduce the voltage of an external clock. However, note that the resistor divider will consume current. For example, if the clock swing into the resistor divider circuit in Figure 2-2 is 3.3V, the circuit will consume approximately 5.5µA of additional current, so this trade-off should be taken into consideration.

Figure 2-2. Resistor Divider Example for an External RTC



2.3 Restrictions for Power States

When VDDIO is off (either disconnected or at ground potential), a voltage must not be applied to the device pins. This is because each pin contains an ESD diode from the pin to the VDDIO supply. This diode will turn on when a voltage higher than one diode-drop is supplied to the pin. This in turn will try to power up the part through the VDDIO supply.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

2.4 Power-up Sequence

The power-up sequence for ATBTLC1000 is shown in Figure 2-3. The timing parameters are provided in Table 2-2.

Figure 2-3. Power-up Sequence

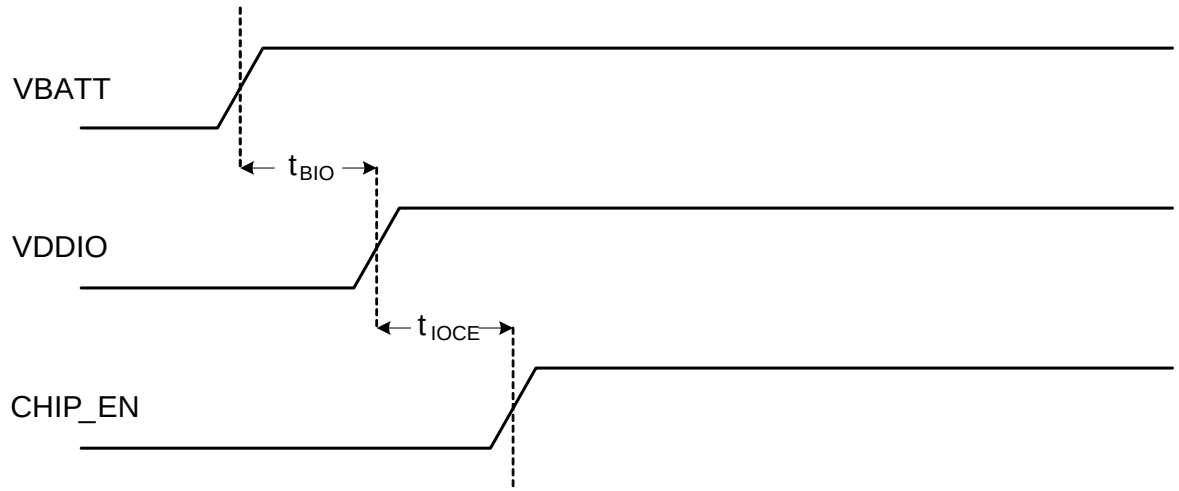


Table 2-2. Power-up Sequence Timing

Parameter	Min.	Max.	Unit	Description	Notes
t_{BIO}	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together
t_{IOCE}	0		ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating

3 Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- The board should have a solid ground plane. The center ground pad of the device must be solidly connected to the ground plane by using a 3 x 3 grid of vias.
- Keep away from antenna, as far as possible, and large metal objects, to avoid electromagnetic field blocking
- Do not enclose the antenna within a metal shield
- Keep any components which may radiate noise or signals within the 2.4 – 2.5GHz frequency band far away from the antenna, or better yet, shield those components. Any noise radiated from the main board in this frequency band will degrade the sensitivity of the module.

3.1 Power and Ground

Dedicate one layer as a ground plane. Make sure that this ground plane does not get broken up by routes. Power can route on all layers except the ground layer. Power supply routes should be heavy copper fill planes to insure the lowest possible inductance. The power pins of the NMC1000 should have a via directly to the power plane as close to the pin as possible. Decoupling capacitors should have a via right next to the capacitor pin and this via should go directly down to the power plane – that is to say, the capacitor should not route to the power plane through a long trace. The ground side of the decoupling capacitor should have a via right next to the pad which goes directly down to the ground plane. Each decoupling capacitor should have its own via directly to the ground plane and directly to the power plane right next to the pad. The decoupling capacitors should be placed as close to the pin that it is filtering as possible.

3.2 RF Traces and Components

The RF trace that routes from the ATBTLC1000's RFIO pin to the antenna must be 50Ω controlled impedance. This is pin 2 of the 32-pin QFN package. This controlled impedance trace must reference a ground plane on a lower layer. To achieve 50Ω impedance, a typical design might implement a coplanar waveguide utilizing 1oz copper and a dielectric constant of 4.0 with a 12 mil wide trace and 6 mil spacing on either side to the top layer ground and referenced to a ground plane on an inner layer, which is 6.5 mils below the trace. This must be adjusted depending on the dielectric and copper weight used. No other traces must route through the RF area on layers between the RF traces and the ground reference plane. In fact, try not to route any other traces in the RF area on any layer. This ground reference plane must extend entirely under the ATBTLC1000 package.

Be sure that the route from pin 2 to the antenna is as short as possible to reduce path losses and to minimize the opportunity for the trace to pick up noise.

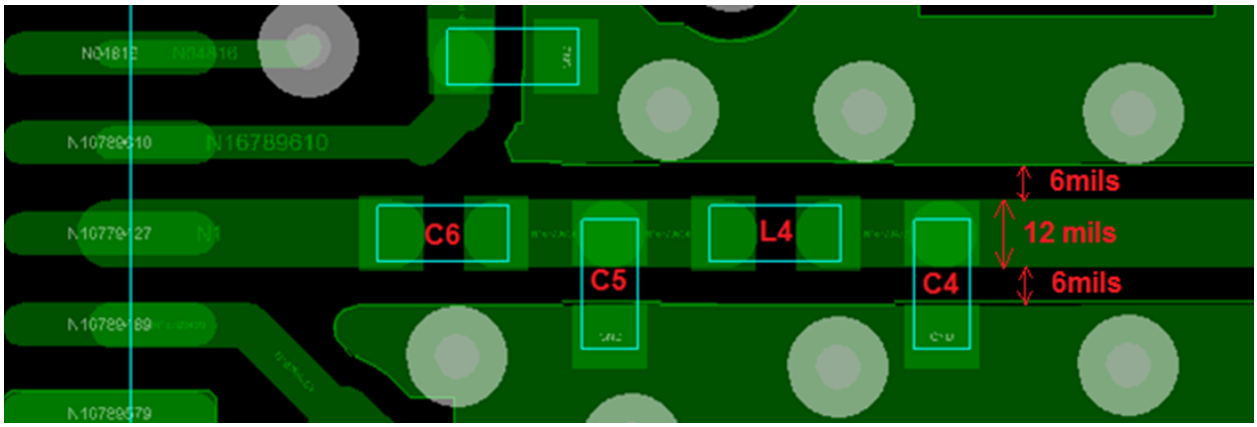
Be sure to add as many ground vias as possible, tying all ground layers together (ground stitching) all along the RF traces and throughout the area where the RF traces are routed. Add at least one ground via right next to the ground pad of each of the components in the RF path. Place ground vias all along the RF traces on either side.

Tie the center ground pad of the ATBTLC1000 to the inner ground layer using a grid of nine vias. The ground path going from the ground pad down to the ground plane must have as low impedance as absolutely possible. The ground return path for the RF must not be broken. It must be a solid, continuous, unbroken low impedance path.

Do not use thermal relief pads for the ground pads of all components in the RF path. These component pads must be completely filled in with ground copper.

Be sure to place the DC blocking capacitor (C4) and matching components (C5, L4, C4) as close to the RFIO pin as possible. Figure 3-1 shows the placement and routing of these components using the design parameters detailed in the first paragraph of this section. Note that they are placed as close as possible to the ATBTLC1000's pin 2. The components used for this design are 0201. Note that the width of the route matches the width of the component pads. This will avoid impedance discontinuities which would occur if there is a large mismatch in trace width versus the component pad size.

Figure 3-1. Placement and Routing of DC Blocking Cap and Matching Components



Be sure that the route from the antenna to the ATBTLC1000 is as short as possible and is completely isolated from all other signals on the board. No signals should route under this trace on any layer of the board. Make sure that all digital signals that may be toggling while the ATBTLC1000 is active are placed as far away from the antenna as possible. No connectors which have digital signals going to them should be near the antenna. All digital components and switching regulators on the board should be shielded so they do not radiate any noise that can be picked up by the antenna.

In summary, make sure that anything that switches is shielded and kept away from the antenna, the ATBTLC1000, or the route from the ATBTLC1000 to the antenna.

3.3 Power Management Unit (PMU)

The ATBTLC1000 contains an on-chip switching regulator, which regulates the VBAT supply down to approximately 1.2V for supplying the rest of the device. It is crucial to place and route the components associated with this circuit correctly to ensure proper operation and especially to reduce any radiated noise, which can be picked up by the antenna and can severely reduce the receiver sensitivity. The external components for the PMU consist of two inductors, L5 = 15nH and L6 = 4.7µH and a capacitor, C14 = 4.7µF. These components must be placed as close as possible to ATBTLC1000 pin 14. The smaller inductor, L5, must be placed closest to pin 14. Current will flow from pin 14, through L5, then L6, and then through C14 to ground and back to the center ground paddle of the ATBTLC1000 package. Place components so this current loop is as small as possible. Make sure there is a ground via to the inner ground plane right next to the ground pin of C14. The ground return path must be extremely low inductance. Failure to provide a short, heavy ground return between the capacitor and the ATBTLC1000 ground pad will result in incorrect operation of the on chip switching regulator. Figure 3-2 shows an example placement and routing of these components. The current loop described above is indicated by the red line, with the dashed portions indicating the path on inner layers. The route from pin 14 to L5 is on an inner layer and is shown in Figure 3-3 in red/white.

Figure 3-2. Placement and Routing of PMU Components

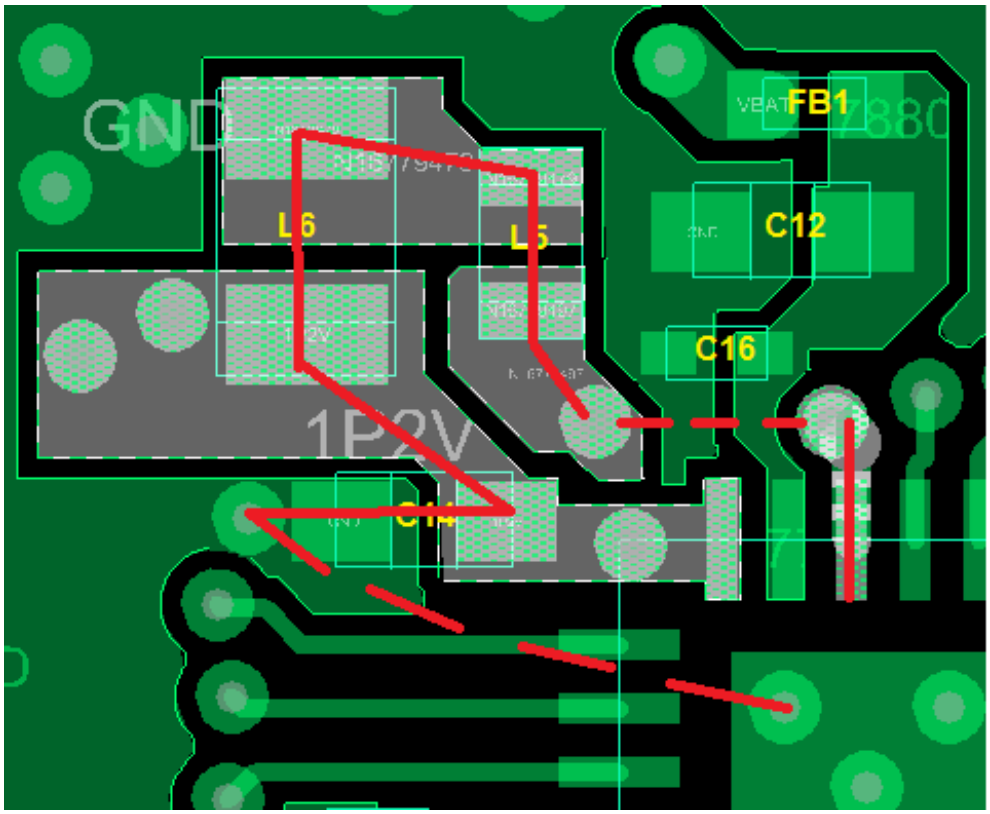
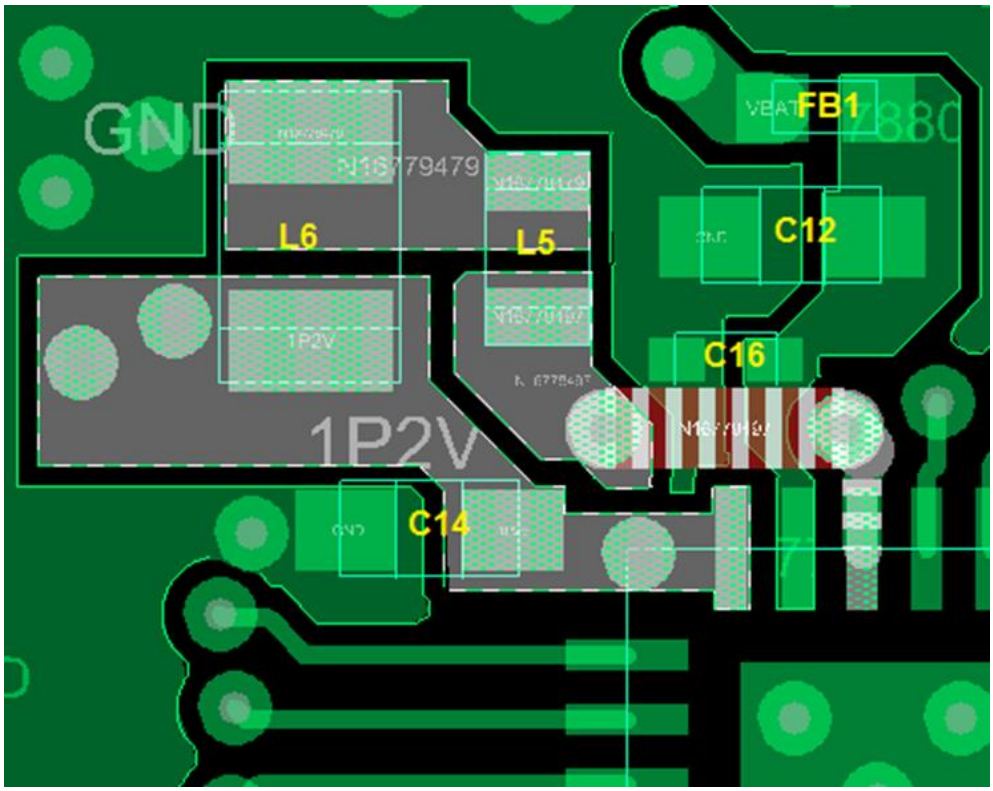


Figure 3-3. Inner Layer PMU Route



Placement of FB1, C12, and C16 should be as close as possible to the VBAT_BUCK pin (pin 15), with the smaller capacitor, C16, placed closest to the pin. Again, the route should be as heavy as possible to provide a low impedance path. The placement and routing of these components is shown in Figure 3-2.

Note that the PMU is a switching regulator and produces noise within the 2.4GHz receive band. Therefore it is essential that the RF route, components, and antenna be kept as far away from the PMU and its components (L5, L6, and C14) as possible.

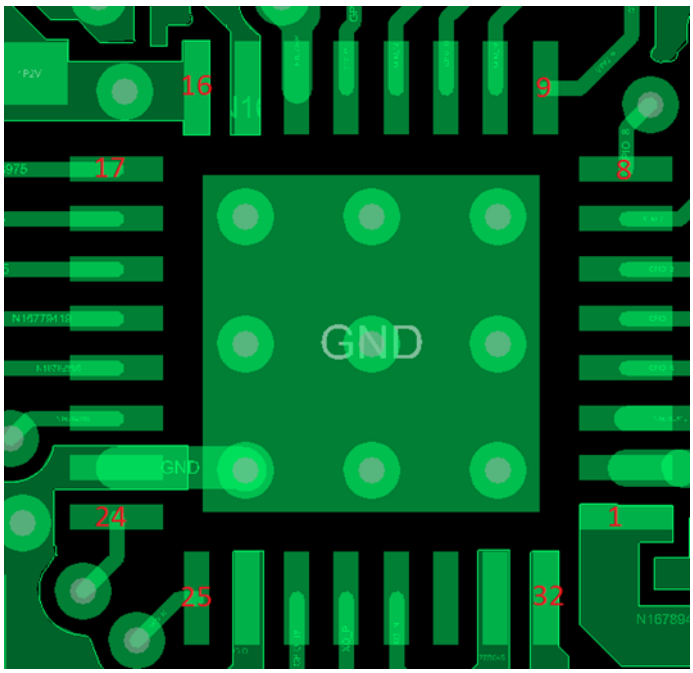
The same goes for the VBAT_Buck supply. This is the supply for the PMU and noise from the PMU feeds back to this supply pin. FB1 is used to suppress this noise to keep it from radiating from the supply route. Therefore, the RF route should also be kept away from the VBAT_Buck supply route and FB1, C12, and C16.

A shield should be placed over the ATBTLC1000 and PMU components to keep any RF radiation from being picked up by the antenna.

3.4 Ground

Proper grounding is essential for correct operation of the device and peak performance. A solid inner layer ground plane should be provided. The center ground paddle of the device must have a grid of ground vias solidly connecting the pad to the inner layer ground plane. A 3x3 grid of ground vias is recommended. These ground vias must surround the perimeter of the pad. One of these ground vias must be in the center pad as close as possible to pin 2 (RFIO). This ground via serves as the RF ground return. There must also be a ground via in the center pad as close as possible to pin 14. This is the ground return for the PMU. See Figure 3-4 for an example of the recommended grounding of the center pad.

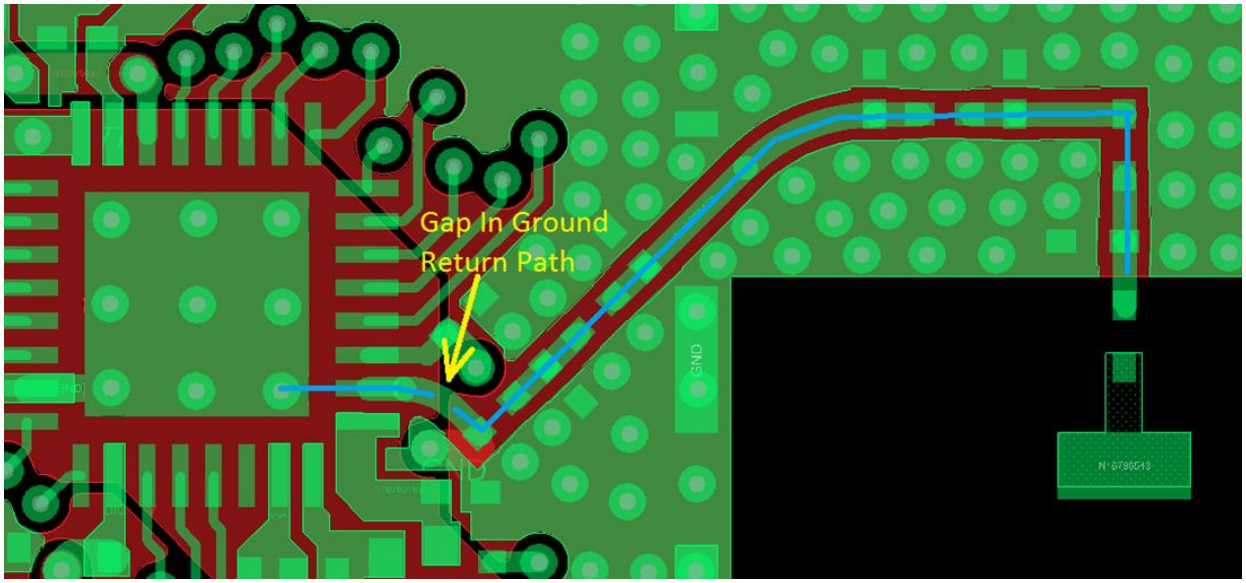
Figure 3-4. Proper Grounding of Center Ground Pad



As mentioned previously, one inner layer should be dedicated as a ground plane. It is important that the ground return currents have direct low impedance path back to the device ground. This is especially crucial for the RF and PMU ground returns. Figure 3-5 shows the top layer RF path route superimposed over an example of an incorrect second layer ground. In Figure 3-5 the top layer is shown in green and the second layer is shown in red. The RF route is indicated by the blue line. The RF return current will flow back along this path to the package ground pin closest to the RFIO pin (pin 2). But as shown in Figure 3-

5, a gap exists in the ground plane blocking the return current. This discontinuity in the ground will greatly affect the RF performance and must be avoided at all costs. This example also shows the correct placement of ground vias in the center paddle. Note that there is a ground via placed directly next to the RFIO pin.

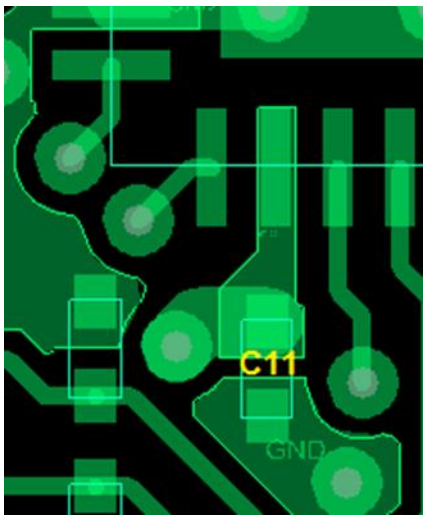
Figure 3-5. Example of an Incorrect Ground Plane



3.5 VDDIO

VDDIO (pin 26) is also a supply input pin and the route to this should be a large power route. The decoupling capacitor for this supply (C11) should be placed as close as possible to the pin. Figure 3-6 shows the placement of the decoupling capacitor and the route to this power pin.

Figure 3-6. VDDIO Route and Decoupling Capacitor Placement



3.6 LP_LDO_OUT

LP_LDO_OUT (pin20) is the output of an on-chip regulator. It requires a 1µF ceramic capacitor (C13) to be placed as close as possible to the pin.

3.7 Sensitive Routes

The following signals are very sensitive to noise and one must take care to keep them as short as possible and keep them isolated from all other signals by routing them far away from other traces or by using ground to shield them. Pay special attention to routes on layers above and below these routes. Any noisy signals running above or below these signals on other layers will couple noise into these routes:

XO_N

XO_P

RFIO

3.8 Supply Pins

The following are power supply pins for the ATBTLC1000. They are supplied with approximately 1.2V by the on-chip PMU. It is important that the decoupling capacitors for these supplies are placed as close to the ATBTLC1000 pin as possible. This is necessary to reduce the trace inductance between the capacitor and ATBTLC1000 power pin to an absolute minimum:

VDDRF (pin 1)

VDD_AMS (pin 3)

VDD_SXDIG (pin 31)

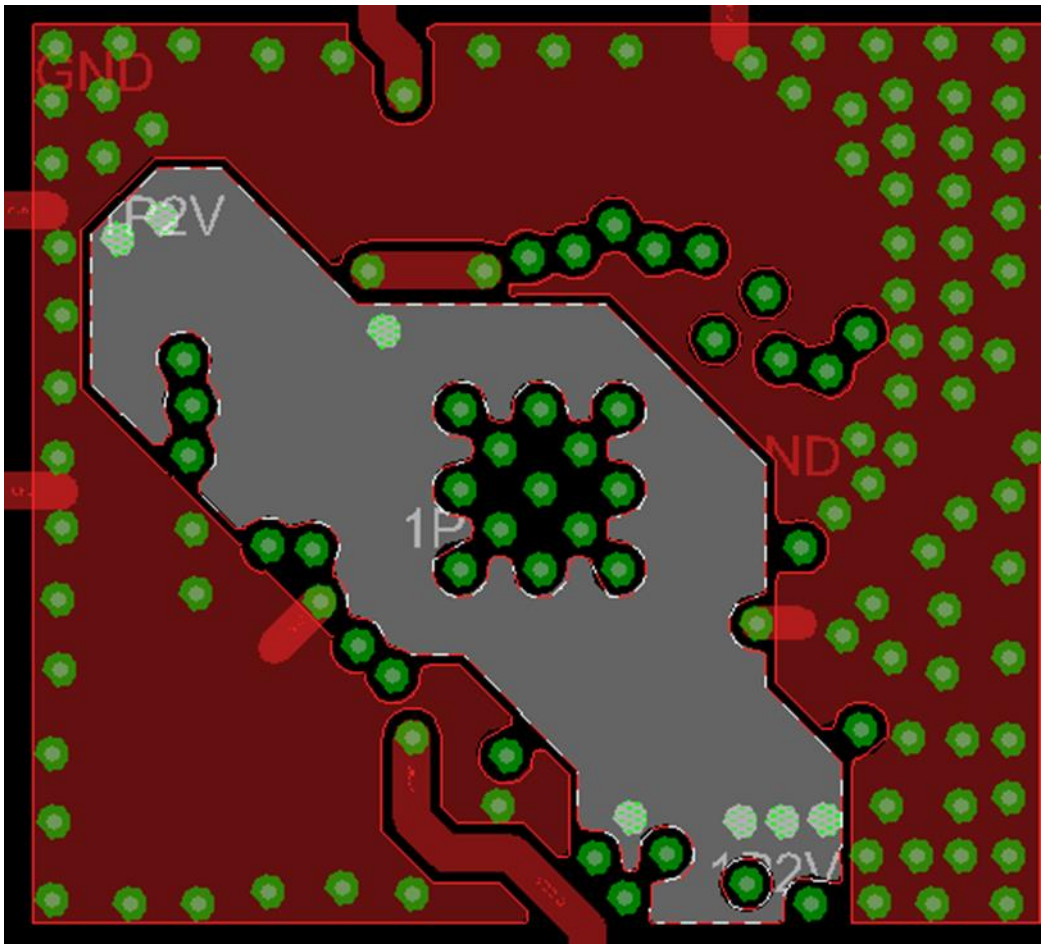
VDD_VCO (pin 32)

VDDC_PD4 (pin16)

Place one 0.1µF capacitor as close as possible to pins 3, 31 and 32. Place a 1µF capacitor as close as possible to pin 3.

The route going from C14 in the reference schematic to pins 1, 3, 16, 31, and 32 is a power route. It should be as short and heavy as possible. Try to route it as a power plane on an inner layer. In Figure 3-7, shown in grey, is an example of a route of this supply on an inner layer of a PCB. The three vias in the upper left portion go to C14 and the 1.2V route on the top layer, visible in Figure 3-2. The via below and to the right goes to ATBTLC1000 pin 16 and vias in the bottom right go to pins 1, 3, 31, and 32.

Figure 3-7. Routing of 1P2V Supply



Additionally, while the VBAT_BUCK (pin 15) supply is not sensitive to picking up noise, it is a noise generating supply. Therefore, be sure to keep the decoupling capacitors for this supply pin as close as possible to the VBAT_BUCK pin and make sure that the route for this supply stays far away from sensitive pins and supplies.

3.9 Additional Suggestions

Make sure that traces route directly through the pads of all filter capacitors and not by a stub route. Figure 3-8 shows the correct way to route through a capacitor pad. Figure 3-9 shows a stub route to the capacitor pad. This should be avoided as it adds additional impedance in series with the capacitor.

Figure 3-8. Correct Routing Through Capacitor Pad

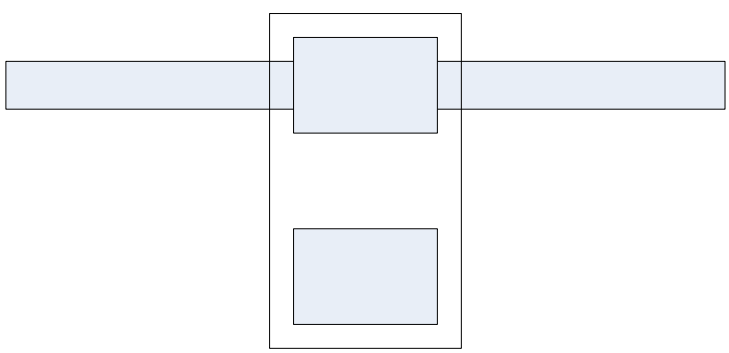
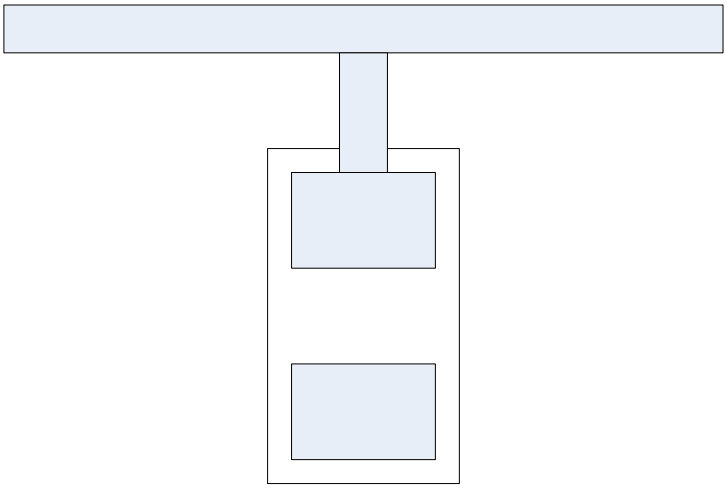


Figure 3-9. Incorrect Stub Route To Capacitor Pad



4 Interferers

One of the major problems with RF receivers is poor performance due to interferers on the board radiating noise into the antenna or coupling into the RF traces going to input LNA. Care must be taken to make sure that there is no noisy circuitry placed anywhere near the antenna or the RF traces. All noise generating circuits should also be shielded so they do not radiate noise that is picked up by the antenna. Also, make sure that no traces route underneath the RF portion of the ATBTLC1000. Also, make sure that no traces route underneath any of the RF traces from the antenna to the ATBTLC1000 input. This applies to all layers. Even if there is a ground plane on a layer between the RF route and another signal, the ground return current will flow on the ground plane and couple into the RF traces.

5 Antenna

Make sure to choose an antenna that covers the proper frequency band; 2.400GHz to 2.500GHz. Talk to the antenna vendor and make sure he understands that the full frequency range must be covered by the antenna.

Make sure the antenna is designed for a 50Ω system.

Make sure the PCB pad that the antenna is connected to is properly designed for 50Ω impedance. **This is extremely important!** The antenna vendor must specify the pad dimensions, the spacing from the pad to the ground reference plane, and the spacing from the edges of the pad to the ground fill on the same layer as the pad. Also, since the ground reference plane for the 50 trace going from the antenna pad to the ATBTLC1000 will probably be on a different layer than the ground reference for the antenna pad, make sure the pad design has a proper transition from the pad to the 50Ω trace.

Make sure that the antenna matching components are placed as close to the antenna pad as possible. The antenna cannot be properly matched if the matching components are far away from the antenna.

6 Reference Documentation and Support

6.1 Reference Documents

Atmel offers a set of collateral documentation to ease integration and device ramp.

Table 6-1 shows a list of documents available on the Atmel web or integrated into development tools.

Table 6-1. Document List

Title	Content
ATBTLC1000 QFN SoC, Datasheet	
Design Files Package	User Guide, Schematic, PCB layout, Gerber, BOM & System notes on: RF/Radio Full Test Report, radiation pattern, design guidelines, temperature performance, ESD.
Platform Getting started Guide	How to use package: Out of the Box starting guide, HW limitations and notes, SW Quick start guidelines.
HW Design Guide	This document
SW Design Guide	Integration guide with clear description of: High level Arch, overview on how to write a networking application, list all API, parameters and structures. Features of the device, SPI/handshake protocol between device and host MCU, with flow/sequence/state diagram, timing.
SW Programmer guide	Explain in details the flow chart and how to use each API to implement all generic use cases (e.g. start AP, start STA, provisioning, UDP, TCP, http, TLS, p2p, errors management, connection/transfer recovery mechanism/state diagram) - usage and sample application note

For a complete listing of development-support tools and documentation, visit http://www.atmel.com/ or contact the nearest Atmel field representative.

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8 Revision History

Doc Rev.	Date	Comments
42537B	10/2015	• The document title is updated • Figure 1-1 and Figure 1-2 are updated • New Section 2.2 is added • Section 3.2 is updated • Section 3.3 is updated • Figure 3-2 is updated • New Section 3.4 is added
42537A	09/2015	Initial document release.

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