PCN Number:	20170125000	PCN Date:	Jan. 26, 2017
Title:	Datasheet for ADS54J20, ADS54J40, ADS54J60, ADS54J69		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:			

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.

The product datasheet(s) is being updated as summarized below.

The following change history provides further details.

TEXAS INSTRUMENTS

ADS54J20

SBAS766B – MAY 2016 – REVISED JANUARY 2017

Changes from Revision A (May 2016) to Revision B	Page
• Changed the *Device Comparison Table*	3
• Added the FOVR latency parameter to the *Timing Characteristics* table	12
• Added *SYSREF Not Present (Subclass 0, 2)* section	30
• Changed the number of clock cycles in the *Fast OVR* section	31
• Changed the *Register Map*	45
• Deleted register 39h, 3Ah, and 56h	45
• Changed *Power Supply Recommendations* section	75
• Added the *Power Sequencing and Initialization* section	76
• Added the *Receiving Notification of Documentation Updates* section	79

Changes from Revision A (October 2015) to Revision B **Page**

- Added *Device Comparison Table* ... 4
- Added CDM row to *ESD Ratings* table ... 6
- Changed the minimum value for the input clock frequency in the *Recommended Operating Conditions* table ... 6
- Changed Sample Timing, *Aperture jitter* parameter typical specification in *Timing Characteristics* section ... 12
- Added the FOVR latency parameter to the *Timing Characteristics* table ... 12
- Changed *Overview* section ... 23
- Changed *Functional Block Diagram* section: changed Control and SPI block and added dashed outline to FOVR traces 23
- Changed *SYSREF Signal* section: changed Table 4 and added last paragraph ... 28
- Added *SYSREF Not Present (Subclass 0, 2)* section ... 29
- Changed the number of clock cycles in the *Fast OVR* section ... 30
- Deleted *Lane Enable with Decimation* subsection ... 39
- Added the *Program Summary of DDC Modes and JESD Link Configuration* table ... 41
- Added Figure 80 to *Register Maps* section ... 43
- Changed the *Register Map* ... 44
- Deleted register 39h, 3Ah, and 56h ... 44
- Added Table 53 ... 61
- Changed *Power Supply Recommendations* section ... 75
- Added the *Power Sequencing and Initialization* section ... 76
- Added the *Receiving Notification of Documentation Updates* section ... 79

Changes from Revision B (August 2015) to Revision C **Page**

- Changed the SFDR value in the last sub-bullet of the *Spectral Performance* Features bullet ... 1
- Changed *Device Information* table ... 1
- Added *Device Comparison Table* ... 5
- Added CDM row to *ESD Ratings* table ... 7
- Changed the minimum value for the input clock frequency in the *Recommended Operating Conditions* table ... 7
- Added minimum value to the ADC sampling rate parameter in the *Electrical Characteristics* table ... 8
- Added 720 MHz test condition rows to SNR, NSD, SINAD, SFDR, HD2, HD3, Non HD2, HD3, THD, and SFDR_IL parameters of *AC Characteristics* table ... 9
- Changed typical specification of SFDR parameter in *AC Characteristics* table ... 10
- Changed Sample Timing, *Aperture jitter* parameter typical specification in *Timing Characteristics* section ... 13
- Added the FOVR latency parameter to the *Timing Characteristics* table ... 13
- Added Figure 10 ... 16
- Added *Typical Characteristics: Contour* section ... 24
- Changed *Overview* section ... 26
- Changed *Functional Block Diagram* section: changed Control and SPI block and added dashed outline to FOVR traces 26
- Added Figure 60 and text reference to *Analog Inputs* section ... 28
- Changed *SYSREF Signal* section: changed Table 4 and added last paragraph ... 31
- Added *SYSREF Not Present (Subclass 0, 2)* section ... 32
- Changed the number of clock cycles in the *Fast OVR* section ... 33
- Changed Table 10 and Table 11 ... 41
- Changed Table 12 and Table 13 ... 42
- Deleted *Lane Enable with Decimation* subsection ... 42
- Added the *Program Summary of DDC Modes and JESD Link Configuration* table ... 43

- Added Figure 83 to *Register Maps* section 45
- Changed Table 15 46
- Deleted register 39h, 3Ah, and 56h 46
- Changed *Example Register Writes* section 48
- Updated register descriptions 49
- Added Table 51 62
- Deleted row for bit 1 in Table 60 as bit 1 is included in last table row 67
- Changed Table 65 70
- Changed internal aperture jitter value in *SNR and Clock Jitter* section 73
- Changed Figure 132 73
- Changed *Power Supply Recommendations* section 76
- Added the *Power Sequencing and Initialization* section 77
- Added *Documentation Support* and *Receiving Notification of Documentation Updates* sections 80

Changes from Revision B (February 2016) to Revision C **Page**

- Added *Device Comparison Table* 5
- Added the FOVR latency parameter to the *Timing Characteristics* table 12
- Added *SYSREF Not Present (Subclass 0, 2)* section 27
- Changed the number of clock cycles in the *Fast OVR* section 28
- Changed the *Register Map* 40
- Deleted register 39h, 3Ah, and 56h 40
- Changed the *SNR versus Input Frequency and External Clock Jitter* figure 67
- Changed *Power Supply Recommendations* section 70
- Added the *Power Sequencing and Initialization* section 71
- Added *Documentation Support* and *Receiving Notification of Documentation Updates* sections 74
- Added the *Receiving Notification of Documentation Updates* section 74

The datasheet number will be changing.

Device Family	Change From:	Change To:
ADS54J20	SBAS766A	**SBAS766B**
ADS54J40	SBAS714A	**SBAS714B**
ADS54J60	SBAS706B	**SBAS706C**
ADS54J69	SBAS713B	**SBAS713C**

These changes may be reviewed at the datasheet links provided.
http://www.ti.com/product/ADS54J20
http://www.ti.com/product/ADS54J40
http://www.ti.com/product/ADS54J60
http://www.ti.com/product/ADS54J69

Reason for Change:

To more accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.			
Product Affected:			
ADS54J20IRMP	ADS54J20IRMPT	ADS54J40IRMP	ADS54J40IRMPT
ADS54J60IRMP	ADS54J60IRMPT	ADS54J69IRMP	ADS54J69IRMPT

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

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