PIC18F85J90 Family Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39770**B**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F85J90 family of devices will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Reset

In Register 4-1: RCON: Reset Control Register, on page 46, the register map and description for bit 5 is changed as shown in bold text.

REGISTER 4-1: RCON: RESET CONTROL REGISTER

R/W-0	U-0	**R/W-1**	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	—	**$\overline{\text{CM}}$**	$\overline{\text{RI}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **IPEN:** Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16XXXX Compatibility mode)

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **$\overline{\text{CM}}$: Configuration Mismatch Flag bit**
1 = A Configuration Mismatch Reset has not occurred
0 = A Configuration Mismatch Reset occurred. Must be set in software once the Reset occurs.

bit 4 **$\overline{\text{RI}}$:** RESET Instruction Flag bit
1 = The RESET instruction was not executed (set by firmware only)
0 = The RESET instruction was executed causing a device Reset (must be set in software after a Brown-out Reset occurs)

bit 3 **$\overline{\text{TO}}$:** Watchdog Time-out Flag bit
1 = Set by power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT time-out occurred

bit 2 **$\overline{\text{PD}}$:** Power-Down Detection Flag bit
1 = Set by power-up or by the CLRWDT instruction
0 = Set by execution of the SLEEP instruction

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit
1 = A Power-on Reset has not occurred (set by firmware only)
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit
1 = A Brown-out Reset has not occurred (set by firmware only)
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

2. Module: Reset

The following section is added after **Section 4.4 "Brown-out Reset (BOR)"** on page 47.

4.5 Configuration Mismatch (CM)

The Configuration Mismatch (CM) Reset register is designed to detect and attempt to recover from random, memory corrupting events. This includes Electrostatic Discharge (ESD) events which can cause widespread, single-bit changes throughout the device and result in catastrophic failure.

In PIC18FXXXX Flash devices, the device Configuration registers (located in the configuration memory space) are continuously monitored during operation by comparing their values to complimentary Shadow registers. If a mismatch is detected between the two sets of registers, a CM Reset automatically occurs.

These events are captured by the $\overline{CM}$ bit (RCON<5>). Whenever a CM event occurs, this bit is set to '0'. For any other Reset event, this bit does not change.

A CM Reset behaves similarly to a Master Clear Reset, RESET instruction, WDT time-out or Stack Event Resets. As with all hard and power Reset events, the device Configuration Words are reloaded from the Flash Configuration Words in program memory as the device restarts.

3. Module: Reset

In the second paragraph of **Section 4.6 "Reset State of Registers"**, on page 50, the $\overline{CM}$ bit is added to the parenthetical list of RCON register status bits.

The paragraph is changed as follows, the bold text indicating the added content:

Most registers are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. Status bits from the RCON register, **CM**, $\overline{RI}$, $\overline{TO}$, $\overline{PD}$, $\overline{POR}$ and $\overline{BOR}$, are set or cleared differently in different Reset situations, as indicated in Table 4-1. These bits are used in software to determine the nature of the Reset.

4. Module: Reset

Table 4-1, on page 50, is changed to add a column for the $\overline{CM}$ bit.

The table appears as follows, the bold text indicating the added material:

TABLE 4-1: STATUS BITS, THEIR SIGNIFICANCE AND THE INITIALIZATION CONDITION FOR RCON REGISTER

Condition	Program Counter(1)	RCON Register						STKPTR Register	
		$\overline{CM}$	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$	STKFUL	STKUNF
Power-on Reset	0000h	**1**	1	1	1	0	0	0	0
RESET Instruction	0000h	**u**	0	u	u	u	u	u	u
Brown-out Reset	0000h	**1**	1	1	1	u	0	u	u
$\overline{MCLR}$ during power-managed Run modes	0000h	**u**	u	1	u	u	u	u	u
$\overline{MCLR}$ during power-managed Idle modes and Sleep mode	0000h	**u**	u	1	0	u	u	u	u
WDT time-out during full power or power-managed Run modes	0000h	**u**	u	0	u	u	u	u	u
$\overline{MCLR}$ during full power execution	0000h	**u**	u	u	u	u	u	u	u
Stack Full Reset (STVREN = 1)	0000h	**u**	u	u	u	u	u	1	u
Stack Underflow Reset (STVREN = 1)	0000h	**u**	u	u	u	u	u	u	1
Stack Underflow Error (not an actual Reset, STVREN = 0)	0000h	**u**	u	u	u	u	u	u	1
WDT time-out during power-managed Idle or Sleep modes	PC + 2	**u**	u	0	0	u	u	u	u
Interrupt exit from power-managed modes	PC + 2	**u**	u	u	0	u	u	u	u

Legend: u = unchanged

Note 1: When the wake-up is due to an interrupt and the GIEH or GIEL bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

5. Module: Reset

In Table 4-2, on page 51, $\overline{CM}$ Resets are added to the title of the fourth column. The table's heading row appears as shown.

TABLE 4-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices	Power-on Reset, Brown-out Reset	**$\overline{MCLR}$ Resets WDT Reset RESET Instruction Stack Resets CM Resets**	Wake-up via WDT or Interrupt

6. Module: Memory Organization

In Table 5-3, on page 70, the $\overline{CM}$ bit is added to the row for the RCON register. The row appears as shown with the change indicated in bold text.

TABLE 5-3: PIC18F85J90 FAMILY REGISTER FILE SUMMARY (CONTINUED)

Filename	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page
RCON	IPEN	—	**$\overline{CM}$**	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$	0-11 11q0	46, 52

7. Module: Interrupts

In Register 8-13: RCON: Reset Control Register, on page 107, bit 5 is changed to include the $\overline{CM}$ bit.

The table appears as shown with the changes highlighted in bold text.

REGISTER 8-13: RCON: RESET CONTROL REGISTER

R/W-0	U-0	**R/W-1**	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	—	**$\overline{CM}$**	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **IPEN:** Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **$\overline{CM}$: Configuration Mismatch Flag bit**
For details of bit operation, see Register 4-1.

bit 4 **$\overline{RI}$:** RESET Instruction Flag bit
For details of bit operation, see Register 4-1.

bit 3 **$\overline{TO}$:** Watchdog Timer Time-out Flag bit
For details of bit operation, see Register 4-1.

bit 2 **$\overline{PD}$:** Power-Down Detection Flag bit
For details of bit operation, see Register 4-1.

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
For details of bit operation, see Register 4-1.

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
For details of bit operation, see Register 4-1.

8. Module: I/O Ports

In Table 9-4, on page 111, the footer row is changed to add “x = Don’t care” and Note 1 is changed to make the “X” into a lowercase “x”.

The table appears as shown, the changes indicated in bold text.

TABLE 9-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTA	RA7(1)	RA6(1)	RA5	RA4	RA3	RA2	RA1	RA0	55
LATA	LATA7(1)	LATA6(1)	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	54
TRISA	TRISA7(1)	TRISA6(1)	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	54
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	53
LCDSE1	SE15	SE14	SE13	SE12	SE11	SE10	SE09	SE08	53
LCDSE2	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	53

Legend: — = unimplemented, read as ‘0’, **x = Don’t care.** Shaded cells are not used by PORTA.

Note 1: These bits are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read as ‘**x**’.

9. Module: Electrical Characteristics

In **Section 25-1 “DC Characteristics: Supply Voltage”**, on page 351, the Brown-out Reset (BOR) voltage for parameter D005 is changed to 1.9V.

The table is changed as shown with the change indicated in bold text.

25.1 DC Characteristics: Supply Voltage PIC18F85J90 Family (Industrial)

PIC18F85J90 Family (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	VDDCORE 2.0	— —	3.6 3.6	V V	ENVREG tied to VSS ENVREG tied to VDD
D001B	VDDCORE	**External Supply for Microcontroller Core**	2.0	—	2.70	V	ENVREG tied to VSS
D001C	AVDD	**Analog Supply Voltage**	VDD – 0.3	—	VDD + 0.3	V	
D001D	AVSS	**Analog Ground Potential**	VSS – 0.3	—	VSS + 0.3	V	
D002	VDR	**RAM Data Retention Voltage(1)**	1.5	—	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	—	0.7	V	See **Section 4.3 “Power-on Reset (POR)”** for details
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See **Section 4.3 “Power-on Reset (POR)”** for details
D005	VBOR	**Brown-out Reset Voltage**	—	**1.9**	—	V	

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

10. Module: Electrical Characteristics

In **Section 25.2 "DC Characteristics: Power-Down and Supply Current"**, on page 357, the values and unit of measurement are changed for the rows related to FOSC = 4 MHz, PRI_IDLE mode with VDD = 3.3V.

The table is changed as shown, with the altered values indicated in bold text.

25.2 DC Characteristics: Power-Down and Supply Current PIC18F85J90 Family (Industrial)

PIC18F85J90 Family (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
	Power-Down Current (IDD)(1)						
	All devices	307	850	µA	-40°C	VDD = 2.0V, VDDCORE = 2.0V(4)	FOSC = 4 MHz (**PRI_IDLE** mode, EC oscillator)
		200	850	µA	+25°C		
		202	800	µA	+85°C		
	All devices	483	950	µA	-40°C	VDD = 2.5V, VDDCORE = 2.5V(4)	
		318	950	µA	+25°C		
		343	900	µA	+85°C		
	All devices	**0.52**	1.3	mA	-40°C	VDD = 3.3V(5)	
		0.48	1.2	mA	+25°C		
		0.47	1.2	mA	+85°C		

11. Module: Electrical Characteristics

The title of **Section 25.3 "DC Characteristics: PIC18F84J90 Family (Industrial)"**, on page 360, is changed to indicate the correct product family.

The title now reads **Section 25.3 "DC Characteristics: PIC18F85J90 Family (Industrial)"**.

12. Module: Electrical Characteristic

In **Section 25.3 "DC Characteristics: PIC18F84J90 Family (Industrial)"**, on page 361, the footnote is removed for parameter 100.

The table's row is changed as shown, with strike through indicating the removed footnote.

25.3 DC Characteristics: PIC18F85J90 Family (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
D100(4)	COSC2	**Capacitive Loading Specs on Output Pins** OSC2 pin	—	15	pF	In HS mode when external clock is used to drive OSC1

13. Module: Migration Between High-End Device Families

In Table B-1, on page 393, the value for the PIC18F85J90 family's Program Memory Endurance is changed to 1,000 Write/Erase Cycles (typical).

The table is changed as shown with bold text indicating the altered content.

TABLE B-1: NOTABLE DIFFERENCES BETWEEN PIC18F8490 AND PIC18F85J90 FAMILIES

Characteristic	PIC18F85J90 Family	PIC18F8490 Family
Operating Frequency	40 MHz @ 2.15V	40 MHz @ 4.2V
Supply Voltage	2.0V-3.6V	2.0V-5.5V
Power-Down Current	Low	Lower
Program Memory Size (maximum)	32 Kbytes	16 Kbytes
Program Memory Endurance	**1,000** Write/Erase Cycles (typical)	100,000 Write/Erase Cycles (typical)
Program Memory Retention	20 Years (minimum)	40 Years (minimum)
Programming Time (Normalized)	43.8 μs/byte (2.8 ms/64-byte block)	15.6 μs/byte (1 ms/64-byte block)
I/O Sink/Source at 25 mA	PORTB and PORTC Only	All Ports
Input Voltage Tolerance on I/O Pins	5.5V on Digital Only Pins	V_{DD} on All I/O Pins
I/O	67	66
LCD Outputs (maximum pixels, segments x commons)	192	192
LCD Bias Generation	4 Modes	1 Mode
LCD Voltage Regulator	Implemented; Includes Voltage Boost	Not Available
Pull-ups	PORTB, PORTD, PORTE and PORTJ	PORTB
Open-Drain Output Option	Available on USARTs, SPI and CCP Output Pins	Not Available
Oscillator Options	Limited Primary Options (EC, HS, PLL); Flexible Internal Oscillator (INTOSC and INTRC)	More Primary Options (EC, HS, XT, LP, RC, PLL); Flexible Internal Oscillator (INTOSC and INTRC)
Programming Entry	Low Voltage, Key Sequence	V_{PP} and LVP
Code Protection	Single Block, All or Nothing	Multiple Code Protection Blocks
Configuration Words	Stored in Last 4 Words of Program Memory space	Stored in Configuration Space, Starting at 300000h
Start-up Time from Sleep	200 μs (typical)	10 μs (typical)
	10 μs (typical) with Voltage Regulator Disabled	
Power-up Timer	Always on	Configurable
Data EEPROM	Not Available	Available
BOR	Simple BOR with Voltage Regulator	Separate Programmable BOR
LVD	Integrated with Voltage Regulator	Separate Programmable Module
A/D Channels	12	12
A/D Calibration	Required	Not Required
In-Circuit Emulation	Not available	Available

14. Module: EUSART

Changes in the BAUDCONx registers are made in the following sections:

- In Register 17-3: BAUDCON1: Baud Rate Control Register 1, bit 6 is renamed and bits 5 and 4 are changed and renamed, as shown in bold text.

REGISTER 17-3: BAUDCON1: BAUD RATE CONTROL REGISTER 1

R/W-0	R-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ABDOVF**: Auto-Baud Acquisition Rollover Status bit
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL**: Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is active

bit 5 **RXDTP**: **Data/Receive Polarity Select bit**
Asynchronous mode:
1 = Receive data (RXx) is inverted (active-low)
0 = Receive data (RXx) is not inverted (active-high)
Synchronous mode:
1 = Data (DTx) is inverted (active-low)
0 = Data (DTx) is not inverted (active-high)

bit 4 **TXCKP**: Synchronous Clock Polarity Select bit
Asynchronous mode:
1 = Idle state for transmit (TXx) is a low level
0 = Idle state for transmit (TXx) is a high level
Synchronous mode:
1 = Idle state for clock (CKx) is a high level
0 = Idle state for clock (CKx) is a low level

bit 3 **BRG16:** 16-Bit Baud Rate Register Enable bit
1 = 16-bit Baud Rate Generator – SPBRGH1 and SPBRG1
0 = 8-bit Baud Rate Generator – SPBRG1 only (Compatible mode), SPBRGH1 value ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
1 = EUSART will continue to sample the RX1 pin – interrupt generated on falling edge; bit cleared in hardware on following rising edge
0 = RX1 pin not monitored or rising edge detected
Synchronous mode:
Unused in this mode.

bit 0 **ABDEN**: Auto-Baud Detect Enable bit
Asynchronous mode:
1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.
0 = Baud rate measurement disabled or completed
Synchronous mode:
Unused in this mode.

- Bits 6, 5 and 4 are renamed In the following tables:
  - Table 17-2: Registers Associated with the Baud Rate Generator
  - Table 17-5: Registers Associated with Asynchronous Transmission
  - Table 17-6: Registers Associated with Asynchronous Reception

TABLE 17-2: REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	53
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	53
BAUDCON1	ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN	55
SPBRGH1	EUSART Baud Rate Generator Register High Byte								55
SPBRG1	EUSART Baud Rate Generator Register Low Byte								53

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the BRG.

TABLE 17-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
PIR1	—	ADIF	RC1IF	TX1IF	SSPIF	—	TMR2IF	TMR1IF	54
PIE1	—	ADIE	RC1IE	TX1IE	SSPIE	—	TMR2IE	TMR1IE	54
IPR1	—	ADIP	RC1IP	TX1IP	SSPIP	—	TMR2IP	TMR1IP	54
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	53
TXREG1	EUSART Transmit Register								53
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	53
BAUDCON1	ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	**ABDEN**	55
SPBRGH1	EUSART Baud Rate Generator Register High Byte								55
SPBRG1	EUSART Baud Rate Generator Register Low Byte								53
LATG	U2OD	U1OD	—	LATG4	LATG3	LATG2	LATG1	LATG0	54

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

TABLE 17-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
PIR1	—	ADIF	RC1IF	TX1IF	SSPIF	—	TMR2IF	TMR1IF	54
PIE1	—	ADIE	RC1IE	TX1IE	SSPIE	—	TMR2IE	TMR1IE	54
IPR1	—	ADIP	RC1IP	TX1IP	SSPIP	—	TMR2IP	TMR1IP	54
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	53
RCREG1	EUSART Receive Register								53
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	53
BAUDCON1	ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN	55
SPBRGH1	EUSART Baud Rate Generator Register High Byte								55
SPBRG1	EUSART Baud Rate Generator Register Low Byte								53

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

- The values for the Resets and WDT wake-up and interrupt are changed in the fourth page of Table 4-2: Initialization Conditions for All Registers, as shown by bold text.

TABLE 4-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets WDT Reset RESET Instruction Stack Resets CM Resets	Wake-up via WDT or Interrupt
...					
SPBRGH1	PIC18F6XJ11	PIC18F8XJ11	0000 0000	0000 0000	uuuu uuuu
BAUDCON1	PIC18F6XJ11	PIC18F8XJ11	**0100 0-00**	**0100 0-00**	**uuuu u-uu**
CCPR1H	PIC18F6XJ11	PIC18F8XJ11	xxxx xxxx	uuuu uuuu	uuuu uuuu
...					

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 4-1 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read as '0'.

- Bits 6, 5 and 4 are renamed and the POR/BOR value changed in the last page of Table 5-3: PIC18F85J90 Family Register File Summary, as shown in bold text.

TABLE 5-3: PIC18F85J90 FAMILY REGISTER FILE SUMMARY

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page
SPBRGH1	EUSART Baud Rate Generator High Byte								0000 0000	55, 233
BAUDCON1	ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN	**0100 0-00**	55, 232
LCDDATA23(2)	S47C3	S46C3	S45C3	S44C3	S43C3	S42C3	S41C3	S40C3	xxxx xxxx	55, 161

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition, r = reserved, do not modify

Note 1: Bit 21 of the PC is only available in Test mode and Serial Programming modes.

2: These registers and/or bits are available only on 80-pin devices; otherwise, they are unimplemented and read as '0'. Reset states shown are for the 80-pin devices.

3: Alternate names and definitions for these bits when the MSSP module is operating in I^2C™ Slave mode. See Section 16.4.3.2 "Address Masking" for details.

4: The PLLEN bit is only available in specific oscillator configurations; otherwise, it is disabled and reads as '0'. See Section 2.4.3 "PLL Frequency Multiplier" for details.

5: RA6/RA7 and their associated latch and direction bits are configured as port pins only when the internal oscillator is selected as the default clock source (FOSC2 Configuration bit = 0); otherwise, they are disabled and these bits read as '0'.

15. Module: Table 25-1: Memory Programming Requirements

On page 362, the parameter, D132, which provides the minimum voltage levels of the Self-Timed Erase or Write is changed. The parameter number is assigned for TWE and its conditions column has changed. A new parameter, D133B, is added. The changed content is indicated in bold text in the following table:

TABLE 25-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	100	1K	—	E/W	-40°C to +85°C
D131	VPR	VDDcore for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132	VPEW	Voltage for Self-Timed Erase or Write					
		VDD	**2.35**	—	3.6	V	ENVREG tied to VDD
		VDDCORE	2.25	—	2.7	V	ENVREG tied to VSS
D133A	TIW	Self-Timed Write Cycle Time	—	2.8	—	ms	—
D133B	**TIE**	**Self-Timed Page Erase Cycle Time**	**—**	**33.0**	**—**	**ms**	**—**
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	3	7	mA	—
D1**40**	TWE	Writes per Erase Cycle	—	—	1	—	**For each physical address**

† Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

16. Module: Table 25-2: Comparator Specifications

In Table 25-2, page 363, the maximum Input Offset Voltage (Param No. D300) is changed from ±10 mV to ±25 mV. The parameter numbers for TRESP and TMC2OV are renamed to D303 and D304, respectively. Parameter D305 for VIRV is added. The maximum value of parameter, VIOFF (D300), is changed. The changed content is indicated in bold text in Table 25-2. The note stating "* These parameters are characterized but not tested." is removed from the note section of the table.

TABLE 25-2: Comparator Specifications

Operating Conditions: 3.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	± 5.0	± **25**	mV	
D301	VICM	Input Common Mode Voltage	0	—	AVDD – 1.5	V	
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	
D303	TRESP	Response Time(1)	—	150	400	ns	
D304	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	µs	
D305	**VIRV**	**Internal Reference Voltage**	**—**	**1.2**	**—**	**V**	

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

17. Module: Table 25-4: Internal Voltage Regulator Specifications

On page 363, the comment for the External Filter Capacitor value, CEFC, is changed. The note stating "* These parameters are characterized but not tested. Parameter numbers are not yet assigned for these specifications." is removed. The changed content is indicated in bold text in the following table:

TABLE 25-4: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	VRGOUT	Regulator Output Voltage*	—	2.5	—	V	
	CEFC	External Filter Capacitor Value*	4.7	10	—	µF	**Capacitor must be low series resistance (<5 Ohms)**

18. Module: Section 25-3 "DC Characteristics: PIC18F85J90 Family (Industrial)"

On page 360, the Input Leakage Current is changed. The Analog (D060) has been edited and a new parameter has been added to the Digital (D060A) I/O ports. The changed values are indicated in bold text in the following table.

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
		All I/O ports:				
D030		with TTL buffer	VSS	0.15 VDD	V	
D031		with Schmitt Trigger buffer	VSS	0.2 VDD	V	
D032		$\overline{MCLR}$	VSS	0.2 VDD	V	
D033		OSC1	VSS	0.3 VDD	V	HS, HSPLL modes
D033A		OSC1	VSS	0.2 VDD	V	EC, ECPLL modes(1)
D034		T13CKI	VSS	0.3	V	
	VIH	**Input High Voltage**				
		I/O ports with non 5.5V tolerance:(2)				
D040		with TTL buffer	0.25 VDD + 0.8V	VDD	V	VDD < 3.3V
D041		with Schmitt Trigger buffer	0.8 VDD	VDD	V	
		I/O ports with 5.5V tolerance:(2)				
Dxxx		with TTL buffer	0.25 VDD + 0.8V	5.5	V	VDD < 3.3V
DxxxA			2.0	5.5	V	3.3V ≤ VDD ≤ 3.6V
Dxxx		with Schmitt Trigger buffer	0.8 VDD	5.5	V	
D042		$\overline{MCLR}$	0.8 VDD	VDD	V	
D043		OSC1	0.7 VDD	VDD	V	HS, HSPLL modes
D043A		OSC1	0.8 VDD	VDD	V	EC, ECPLL modes
D044		T13CKI	1.6	VDD	V	
	IIL	**Input Leakage Current(1)**				
D060		**I/O ports with non 5.5V tolerance:(2)**	—	±1	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
D060A		**I/O ports with 5.5V tolerance:(2)**	—	±1	µA	**VSS ≤ VPIN ≤ 5.5V, pin at high-impedance**
D061		$\overline{MCLR}$	—	±1	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	±1	µA	VSS ≤ VPIN ≤ VDD
	IPU	**Weak Pull-up Current**				
D070	IPURB	PORTB weak pull-up current	30	240	µA	VDD = 3.3V, VPIN = VSS

Note 1: Negative current is defined as current sourced by the pin.

2: Refer to Table 9-1 for the pins that have corresponding tolerance limits.

19. Module: Section 9-5 “PORTD, TRISD and LATD Registers”

On page 118, the content in the third paragraph is changed. The changed portion is indicated in bold text in the following section:

Each of the PORTD pins has a weak internal pull-up. A single control bit can turn off all the pull-ups. This is performed by **clearing** bit RDPU (PORTG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on all device Resets.

20. Module: Section 16.3 “SPI Mode” and Section 16.4 “I²C™ Mode”

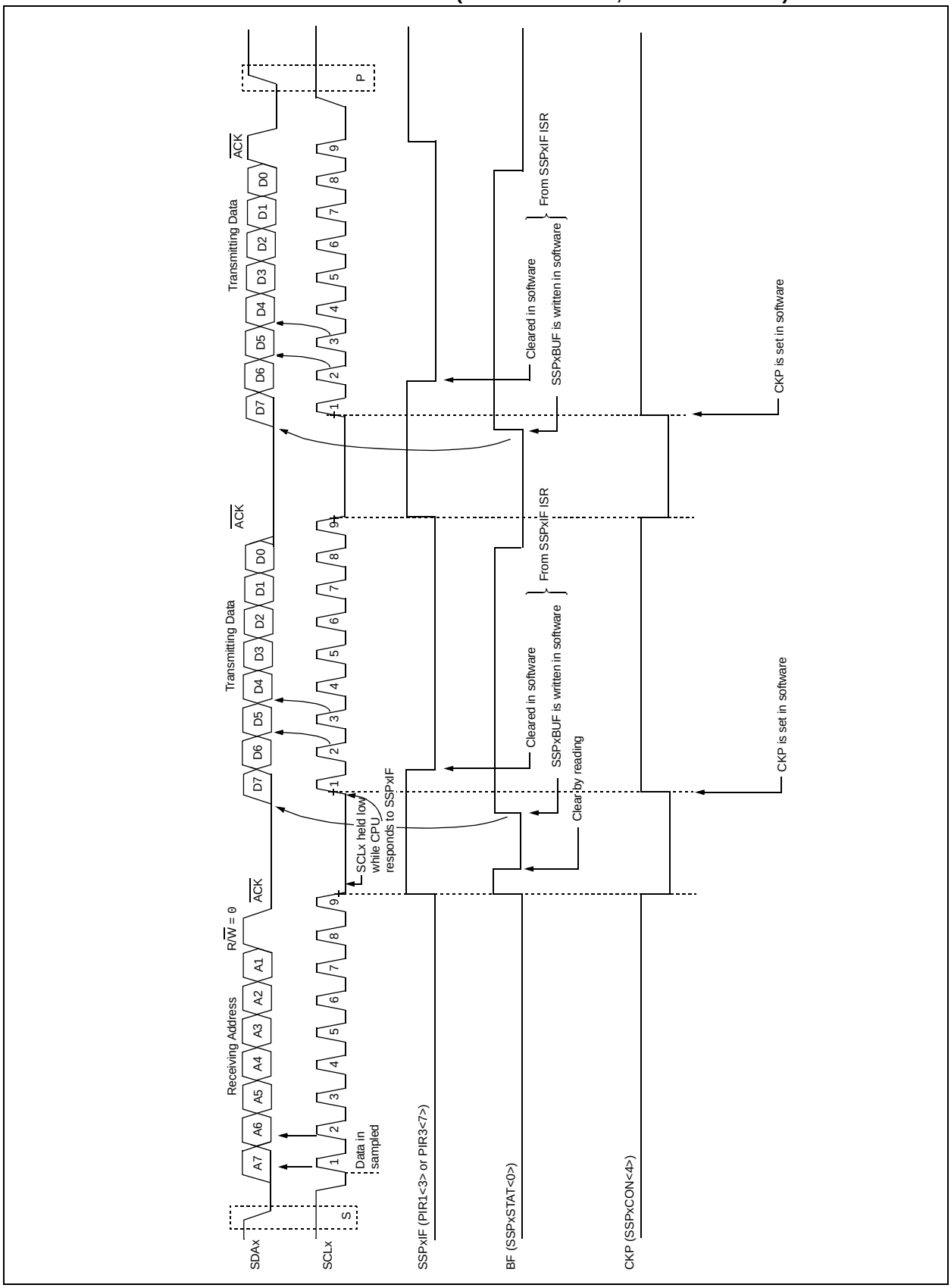
In **Section 16.3 “SPI Mode”** on page 185 and **Section 16.4 “I²C Mode”** on page 194, the following new note is included to describe the necessary procedure to disable the MSSP module:

Note:	Disabling the MSSP module by clearing the SSPEN (SSPCON1<5>) bit may not reset the module. It is recommended to clear the SSPSTAT, SSPCON1 and SSPCON2 registers and select the mode prior to setting the SSPEN bit to enable the MSSP module.

21. Module: Figure 16-10: I²C™ Slave Mode Timing (Transmission, 7-Bit Address)

On page 204,the figure is replaced with the new timing diagram provided in Figure 16-10.

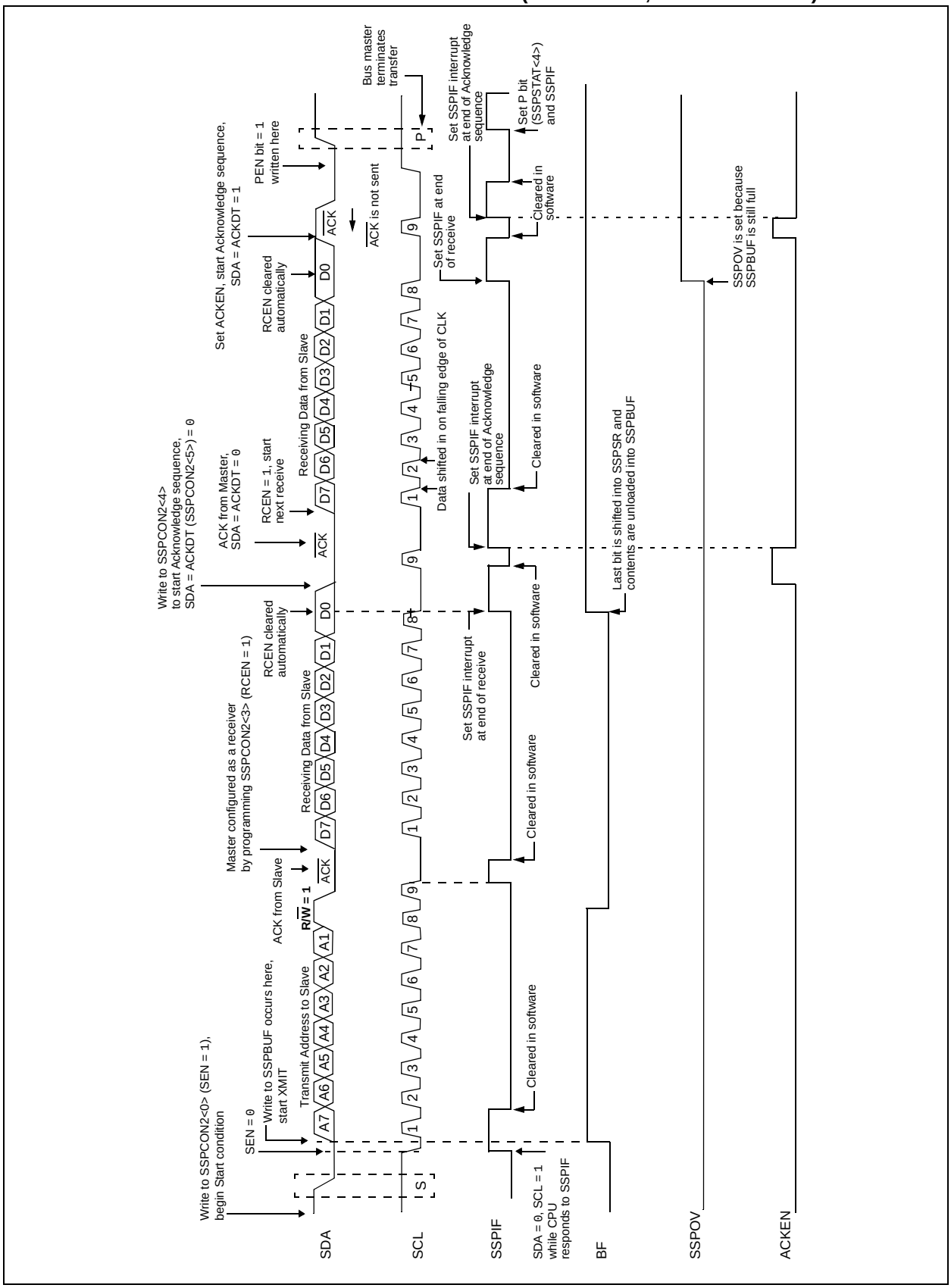
FIGURE 16-10: I²C™ SLAVE MODE TIMING (TRANSMISSION, 7-BIT ADDRESS)



22. Module: Figure 16-24: I²C™ Master Mode Waveform (Reception, 7-Bit Address)

On page 221, the condition (R/$\overline{W}$) when the Acknowledge signal (ACK) is received from the slave, after transmitting the address to the slave, is changed to '1'. The changed value is indicated in bold text in Figure 16-24.

FIGURE 16-24: I²C™ MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)



23. Module: Register 8-12: IPR3

In Register 8-12, on page 106, the POR conditions for the below interrupt priority bits of the Peripheral Interrupt Priority Register 3 (IPR3) have been changed.

LCD Interrupt Priority Bit (LCDIP): The POR condition should be changed to R/W-1 instead of R/W-0.

AUSART Receive Priority Flag Bit (RC2IP): The POR condition should be changed to R-1 instead of R-0.

AUSART Transmit Interrupt Priority Bit (TX2IP): The POR condition should be changed to R-1 instead of R-0.

The modified value is indicated in bold text in the below table.

REGISTER 8-12: IPR3: PERIPHERAL INTERRUPT PRIORITY REGISTER 3

U-0	**R/W-1**	**R-1**	**R-1**	U-0	R/W-1	R/W-1	U-0
—	LCDIP	RC2IP	TX2IP	—	CCP2IP	CCP1IP	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REVISION HISTORY

Rev A Document (8/2006)
Original version of this document. Includes Data Sheet Clarification 1 (Electrical Specifications).

Rev B Document (4/2007)
Removed original Data Sheet Clarification 1 (Electrical Specifications). Added Data Sheet Clarifications 1-5 (Reset), 6 (Memory Organization), 7 (Interrupts), 8 (I/O Ports), 9-13 (Electrical Characteristics) and 14 (Migration Between High-End Device Families).

Rev C Document (7/2008)
Added Data Sheet Clarifications 15 (EUSART) and 16 (Electrical Characteristics). Changed Data Sheet Clarification 11 (Electrical Characteristics).

Rev D Document (10/2008)

Removed Data Sheet Clarification 11 and 16 (Electrical Characteristics). Added Data Sheet Clarifications 15 (Table 25-1: Memory Programming Requirements), 16 (Table 25-2: Comparator Specifications), 17 (Table 25-4: Internal Voltage Regulator Specifications), 18 (Section 25-3 “DC Characteristics: PIC18F85J90 Family – Industrial), 19 (Section 9-5 “PORTD, TRISD and LATD Registers), 20 (Section 16.3 “SPI Mode and Section 16.4 “I^2C™ Mode”), 21 (Figure 16-10: I^2C™ Slave Mode Timing – Transmission, 7-Bit Address), 22 (Figure 16-24: I^2C™ Master Mode Waveform – Reception, 7-Bit Address) and 23 (Register 8-12: IPR3).

Rev E Document (12/2008)
Edits were made to Data Sheet Clarification 18 (Section 25-3 “DC Characteristics: PIC18F85J90 Family – Industrial).

NOTES:

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