A product Line of Diodes Incorporated

PI6C4911506-06

Low Skew, 1-To-6, Crystal/LVCMOS/Differential - 3.3V, 2.5V LVPECL Fanout Buffer

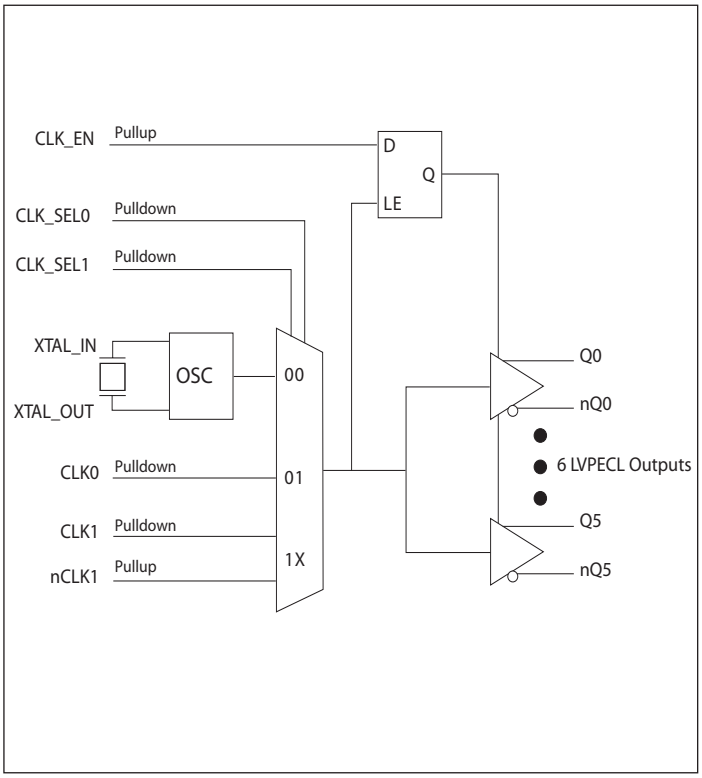
Features

- 6 LVPECL outputs
- Up to 1.5GHz output frequency
- Ultra low additive phase jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Selectable reference inputs support either single-ended or differential or Xtal
- Low skew between outputs (<80ps)
- Low delay from input to output (Tpd typ. 1.5ns)
- Separate Input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- TSSOP-24 package

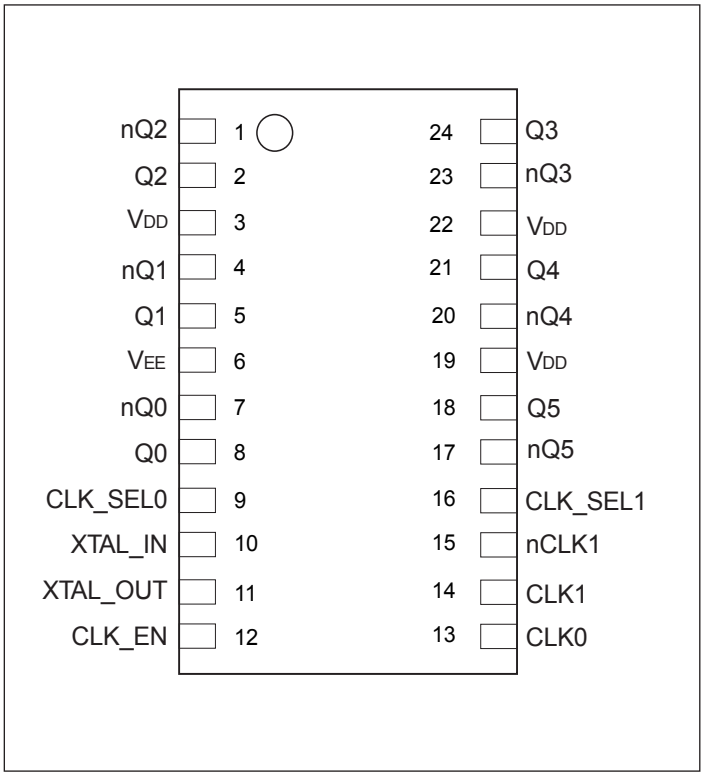
Description

The PI6C4911506-06 is a high performance LVPECL fanout buffer device that accepts crystal, single ended and differential inputs. The part supports up to 1.5GHz frequency. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

Block Diagram



Pin Configuration (24-Pin TSSOP)



Pinout Table

Pin #	Pin Name	Type		Description
1, 2	nQ2, Q2	Output		Differential output pair. LVPECL interface levels
3, 19, 22	V_{DD}	Power		Power supply pins
4, 5	nQ1, Q1	Output		Differential output pair. LVPECL interface levels
6	V_{EE}	Power		Negative supply pin
7, 8	nQ0, Q0	Output		Differential output pair. LVPECL interface levels
9, 16	CLK_SEL0, CLK_SEL1	Input	Pulldown	Clock select pins. LVCMOS/LVTTL interface levels. See Table 3B
10	XTAL_IN	Input		Parallel resonant crystal interface. XTAL_IN is the input
11	XTAL_OUT	Output		Parallel resonant crystal interface. XTAL_OUT is the output
12	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input When LOW, the outputs are disabled LVCMOS / LVTTL interface levels. See Table 3A
13	CLK0	Input	Pulldown	LVCMOS/LVTTL clock input
14	CLK1	Input	Pulldown	Non-inverting differential clock input
15	nCLK1	Input	Pullup	Inverting differential clock input
17, 18	nQ5, Q5	Output		Differential output pair. LVPECL interface levels
20, 21	nQ4, Q4	Output		Differential output pair. LVPECL interface levels
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL interface levels

Note:

1. Pullup and Pulldown refer to internal input resistors. See Table "Pin Characteristics" on page 6, for typical values.

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....-55 to +150°C
Supply Voltage to Ground Potential (VDD) ..... -0.5 to +4.6V
Inputs (Referenced to GND) .....-0.5 to VDD+0.5V
Clock Output (Referenced to GND).....-0.5 to VDD+0.5V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		3.135		3.465	V
			2.375		2.625	V
I_{DD}	Core Power Supply Current	Outputs unloaded			150	mA
T_A	Ambient Operating Temperature		-40		85	°C

LVCMOS / LVTTL DC Characteristics (V_{DD} = 3.3V±5% or 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C)

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD}+0.3	V
			V_{DD} = 2.5V	1.7		V_{DD}+0.3	
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	
			V_{DD} = 2.5V	-0.3		0.7	
I_{IH}	Input High Current	CLK0, CLK_SEL0:1	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
		CLK_EN	V_{DD} = V_{IN} = 3.465V or 2.625V			20	
I_{IL}	Input Low Current	CLK0, CLK_SEL0:1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-15			
		CLK_EN	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			

Differential DC Characteristics (V_{DD} = 3.3V±5% or 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C)

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Units
V_{CMR}	Common Mode Input Voltage [1,2]			V_{EE}+0.5		V_{DD}-0.85	V
V_{PP}	Peak-to-Peak Input Voltage [1]			0.15		1.3	
I_{IL}	Input Low Current	nCLK1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		CLK1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			
I_{IH}	Input High Current	nCLK1	V_{DD} = V_{IN} = 3.465V or 2.625V			5	
		CLK1	V_{DD} = V_{IN} = 3.465V			150	

Note:

1. V_{IL} should not be less than -0.3V.
2. Common mode voltage is defined as V_{CMR} .

DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage	V_{DD}=3.3V	2.1		2.6	V
		V_{DD}=2.5V	1.3		1.6	
V_{OL}	Output Low voltage	V_{DD}=3.3V	1.3		1.8	V
		V_{DD}=2.5V	0.5		0.8	

Crystal Characteristics

Parameter	Test Condition	Min.	Typ.	Max.	Units
Mode of Oscillation		Fundamental			
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

Note:

1. Characterized using an 18pF parallel resonant crystal.

AC Characteristics (V_{DD} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C to 85°C)

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Units
f_{MAX}	Output Frequency	CLK1/nCLK1				1500	MHz
		CLK0				300	
t_{PD}	Propagation Delay [1A, 1B]				1.5		ns
tjit	Buffer Additive Jitter, RMS		CLK1/nCLK1, 156.25MHz, Integration Range: 12kHz - 20MHz		0.03		ps
tsk(o)	Output Skew [2]					80	ps
tsk(pp)	Part-to-Part Skew [3]					450	ps
t_R / t_P	Output Rise/Fall Time		20% to 80%	120		350	ps
odc	Output Duty Cycle			48		52	%

AC Characteristics (V_{DD} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C)

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Units
f_{MAX}	Output Frequency	CLK1/nCLK1				1500	MHz
		CLK0				300	
t_{PD}	Propagation Delay [1A, 1B]				1.5		ns
tjit	Buffer Additive Jitter, RMS		CLK1/nCLK1, 156.25MHz, Integration Range: 12kHz - 20MHz		0.03		ps
tsk(o)	Output Skew [2]					80	ps
tsk(pp)	Part-to-Part Skew [3]					450	ps
t_R / t_P	Output Rise/Fall Time		20% to 80%	120		350	ps
odc	Output Duty Cycle			48		52	%

Note:

1A. Measured from the differential input crossing point to the differential output crossing point.

1B. Measured from V_{DD}/2 input crossing point to the differential output crossing point.

2. Defined as skew between outputs at the same supply voltage and with equal load conditions.

3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions.

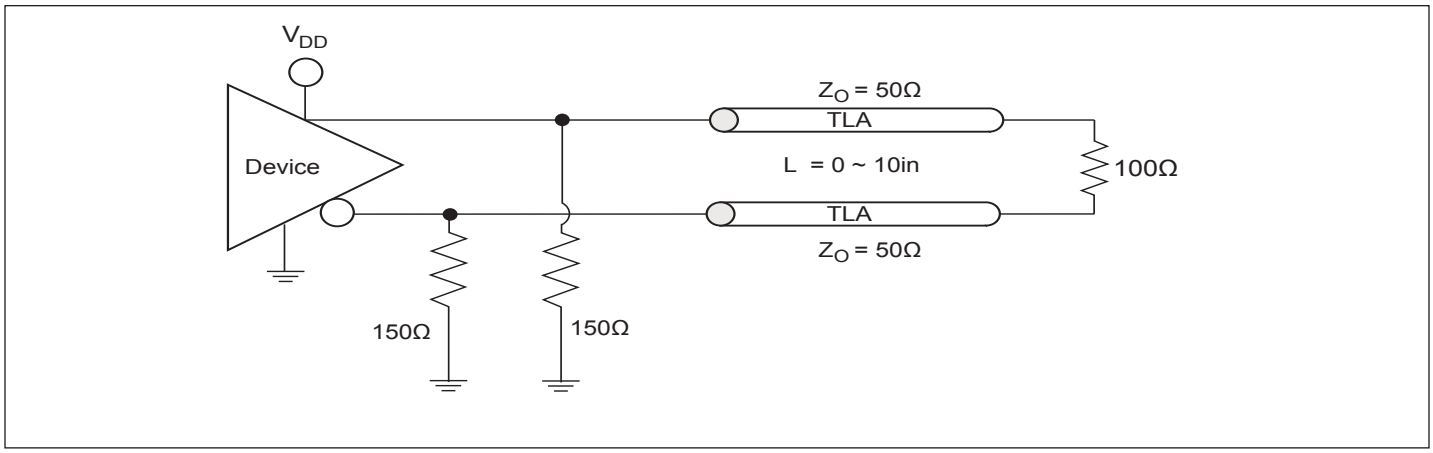
Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor	CLK0, CLK1		51		kΩ
R_{PULLUP}	Input Pulup Resistor	nCLK1		51		kΩ

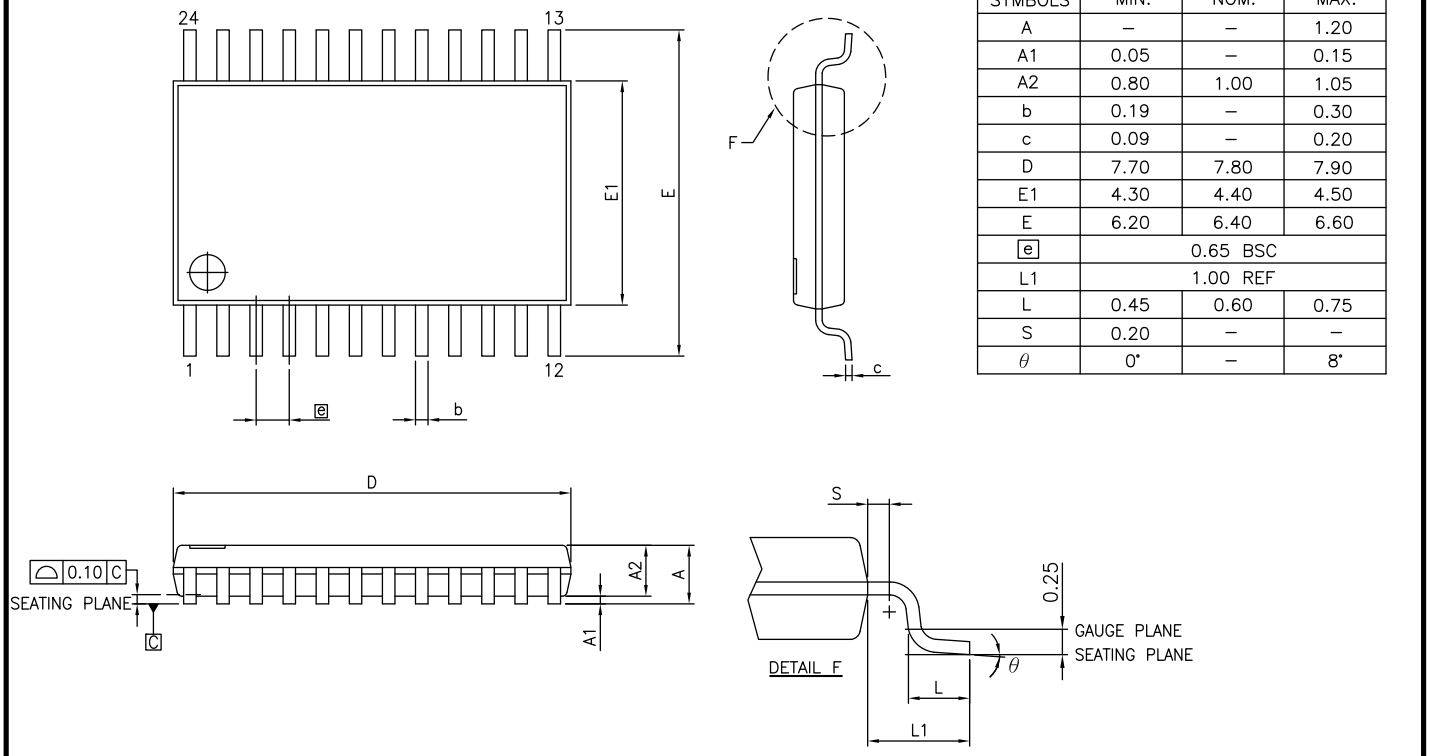
Control Input Function Table

Inputs				Outputs	
CLK_EN	CLK_SEL1	CLK_SEL0	Selected Source	Q0:Q5	nQ0:nQ5
0	0	0	XTAL	Low	High
0	0	1	CLK0	Low	High
0	1	X	CLK1/ nCLK1	Low	High
1	0	0	XTAL	Enabled	Enabled
1	0	1	CLK0	Enabled	Enabled
1	1	X	CLK1/ nCLK1	Enabled	Enabled

Configuration Test Load Board Termination for LVPECL



Packaging Mechanical: 24-Contact TSSOP (L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity — DATE: 03/31/16

DESCRIPTION: 24-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L24)

DOCUMENT CONTROL #: PD-1312 — REVISION: G

16-0075

Note: For latest package info, please check: http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C4911506-06LIE	L	24-pin, 173mil Wide (TSSOP)	-40°C to 85°C
PI6C4911506-06LIEX	L	24-pin, 173mil Wide (TSSOP), Tape & Reel	-40°C to 85°C

Note:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. “E” denotes Pb-free and Green
3. Adding an “X” at the end of the ordering code denotes tape and Reel packaging