DS21448 DALLAS / 1 / X / / 3.3V E1/T1/J1 Quad Line Interface

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GENERAL DESCRIPTION

The DS21448 is a quad-port E1 or T1 line interface unit (LIU) for short-haul and long-haul applications. It incorporates four independent transmitters and four independent receivers in a single 144-pin PBGA or 128-pin LQFP package. The transmit drivers generate the necessary G.703 E1 waveshapes in 75Ω or 120Ω applications and the DSX-1 or CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB for T1 applications.

APPLICATIONS

Integrated Multiservice Access Platforms T1/E1 Cross-Connects, Multiplexers, and Channel **Banks**

Central-Office Switches and PBX Interfaces T1/E1 LAN/WAN Routers Wireless Base Stations

ORDERING INFORMATION

+ Denotes lead-free/RoHS-compliant package.

**All devices rated at 3.3V.*

Pin Configurations appear in Sectio[n 11.](#page-55-0)

FEATURES

- Four Complete E1, T1, or J1 LIUs
- Supports Long- and Short-Haul Trunks
- Internal Software-Selectable Receive-Side Termination for 75Ω/100Ω/120Ω
- 3.3V Power Supply
- 32-Bit or 128-Bit Crystal-Less Jitter Attenuator Requires Only a 2.048MHz Master Clock for E1 and T1, with the Option to Use 1.544MHz for T1
- Generates the Appropriate Line Build-Outs With and Without Return Loss for E1, and DSX-1 and CSU Line Build-Outs for T1
- AMI, HDB3, and B8ZS Encoding/Decoding
- 16.384MHz, 8.192MHz, 4.096MHz, or 2.048MHz Clock Output Synthesized to Recovered Clock
- Programmable Monitor Mode for Receiver
- Loopbacks and PRBS Pattern Generation Detection with Output for Received Errors
- Generates/Detects In-Band Loop Codes, 1 to 16 Bits, Including CSU Loop Codes
- 8-Bit Parallel or Serial Interface with Optional Hardware Mode
- Muxed and Nonmuxed Parallel Bus Supports Intel or Motorola
- Detects/Generates Blue (AIS) Alarms
- NRZ/Bipolar Interface for Tx/Rx Data I/O
- **Transmit Open-Circuit Detection**
- Receive Carrier Loss (RCL) Indication (G.775)
- **High-Z State for TTIP and TRING**
- 50mA_{RMS} Transmit Current Limiter
- **JTAG Boundary Scan Test Port per IEEE 1149.1**
- Meets Latest E1 and T1 Specifications Including ANSI.403-1999, ANSI T1.408, AT&T TR 62411, ITU G.703, G.704, G.706, G.736, G.775, G.823, I.431, O.151, O.161, ETSI ETS 300 166, JTG.703, JTI.431, TBR12, TBR13, and CTR4

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click her[e: www.maxim-ic.com/errata.](http://www.maxim-ic.com/errata)

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2. PIN DESCRIPTION

The DS21448 can be controlled in parallel port mode, serial port mode, or hardware mode. The bus interface select bits 0 and 1 (BIS0, BIS1) determine the device mode and pin assignments [\(Table 2-A](#page-6-1)).

Table 2-B. Pin Assignments

Note 1: The VSM signal is not available with the BGA package option.

Note 2: The LQFP no-connect pin numbers are 4, 5, 37, 67, 69, 70, and 99–101.

Note 3: The BGA no-connect pin numbers are A3, A6, A9, A12, B1, B4, B7, B10, C1–C12, E5–E8, F5–F8, G4–G8, G10, H5–H8, J11, J12, K6, and L4.

Table 2-C. Parallel Interface Mode Pin Description

Table 2-D. Serial Interface Mode Pin Description

Table 2-E. Hardware Interface Mode Pin Description

Note 1: G.703 requires an accuracy of ±50ppm for T1 and E1. TR62411 and ANSI specs require ±32ppm accuracy for T1 interfaces.

3. DETAILED DESCRIPTION

The DS21448 has a usable receiver sensitivity of 0 to -43dB for E1 applications and 0 to -36dB for T1 that allows it to operate on 0.63mm (22AWG) cables up to 2.5km (E1) and 6000ft (T1) in length. The user has the option to use internal receive termination, software selectable for 75Ω, 100Ω, and 120Ω applications, or external termination. The on-board crystal-less jitter attenuator can be placed in either the transmit or the receive data path, and requires only a 2.048MHz MCLK for both E1 and T1 applications (with the option of using a 1.544MHz MCLK in T1 applications).

The DS21448 has diagnostic capabilities such as loopbacks and PRBS pattern generation and detection. 16-bit loop-up and loop-down codes can be generated and detected. A single input pin can power down all transmitters to allow the implementation of hitless protection switching (HPS) for 1+1 redundancy without the use of relays. The device can be controlled through an 8-bit parallel port (muxed or nonmuxed) or a serial port, and it can be used in hardware mode. A standard boundary scan interface supports board-level testing.

The DS21448 contains four independent LIUs that share a common interface for configuration and status. The user can choose between three different means of accessing the device: a parallel microprocessor interface, a serial interface, and a hardwired mode, which configures the device by setting levels on the device's pins. The DS21448's four chip selects (CS1, CS2, CS3, and CS4) determine which LIU is accessed when using the parallel or serial interface modes. Four sets of identical register maps exist, one for each channel. Using the appropriate chip select accesses a channel's register map.

The analog AMI/HDB3 waveform off the E1 line or the AMI/B8ZS waveform off the T1 line is transformer-coupled into the RTIP and RRING pins of the DS21448. The user has the option to use internal termination, software selectable for 75Ω/100Ω/120Ω applications, or external termination. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux, outputting the received line clock at RCLK and bipolar or NRZ data at RPOS and RNEG. The DS21448 contains an active filter that reconstructs the analogreceived signal for the nonlinear losses that occur in transmission. The receive circuitry is also configurable for various monitor applications. The device has a usable receive sensitivity of 0 to -43dB for E1 and 0 to -36dB for T1 that allows the device to operate on 0.63mm (22AWG) cables up to 2.5km (E1) and 6k feet (T1) in length. Data input at TPOS and TNEG is sent through the jitter attenuation mux to the waveshaping circuitry and line driver. The DS21448 drives the E1 or T1 line from the TTIP and TRING pins through a coupling transformer. The line driver can handle both CEPT 30/ISDN-PRI lines for E1 and long-haul (CSU) or short-haul (DSX-1) lines for T1.

3.1 DS21448 and DS21Q348 Differences

The DS21448 BGA is a monolithic quad-port LIU that is a replacement for the DS21Q348. The additional features of JTAG, transmit driver disable, and the serial interface in the DS21448 have changed the function of several pins, as shown in [Table 3-A.](#page-12-2)

Table 3-A. DS21448 vs. DS21Q348 Pin Differences

**DS21448 pin is internally pulled up.*

4. PORT OPERATION

4.1 Hardware Mode

The DS21448 supports a hardware configuration mode that allows the user to configure the device by setting levels on the device's pins. This mode allows the DS21448 configuration without the use of a microprocessor, simplifying designs. Not all of the device features are supported in the hardware mode.

In hardware mode (BIS0 = 1, BIS1 = 1) several pins have been redefined so they can be used for initializing the DS21448. Refer to [Table 2-B](#page-6-2) and [Table 2-E](#page-10-0) for pin assignment and definition. Because of limited pin count, several functions have been combined and affect all four channels in the device and/or treat the receive and transmit paths as one block. Restrictions when using the hardware mode include the following:

- BPCLK pins only output a 16.384MHz signal.
- The RCL/LOTC pins are designated to RCL.
- The RHBE and THBE control bits are combined and controlled by HBE.
- RSCLKE and TSCLKE bits are combined and controlled by SCLKE.
- TCES and RCES are combined and controlled by CES.
- The transmitter functions are combined and controlled by TX1 and TX0.
- Loopback functions are controlled by LOOP1 and LOOP0.
- JABDS defaults to 128-bit buffer depth.
- All other control bits default to logic 0.

Table 4-A. Loopback Control in Hardware Mode

Table 4-B. Transmit Data Control in Hardware Mode

Table 4-C. Receive Sensitivity Settings in Hardware Mode

Table 4-D. Monitor Gain Settings in Hardware Mode

Table 4-E. Internal Rx Termination Select in Hardware Mode

Table 4-F. MCLK Selection in Hardware Mode

4.2 Serial Port Operation

Setting BIS1 = 1 and BIS0 = 0 enables the serial bus interface on the DS21448 [\(Table 2-A](#page-6-1)). Serial port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads or writes by the host. See Section [10](#page-48-0) for the AC timing of the serial port. All serial port accesses are LSB first. See [Figure 4-1,](#page-15-0) [Figure 4-2,](#page-15-1) [Figure 4-3,](#page-15-2) [Figure 4-4](#page-16-0), [Figure 4-5,](#page-16-1) and [Figure 4-6](#page-16-2) for additional details.

A serial bus access requires the use of four signals: serial clock (SCLK), one of the four chip selects (\overline{CS}) , serial data input (SDI), and serial data output (SDO). The DS21448 uses SCLK to sample data that is present on SDI and output data onto SDO. Input clock-edge select (ICES) allows the user to choose which SCLK edge input data is sampled on. Output clock-edge select (OCES) allows the user to choose which SCLK edge output data changes on. When ICES is low, input data is latched on the rising edge of SCLK, and when ICES is high, input data is latched on the falling edge of SCLK. When OCES is low, data is output on the falling edge of SCLK, and when OCES is high, data is output on the rising edge of SCLK. Data is held until the next falling or rising edge of SCLK. All data transfers are initiated by driving the appropriate port's \overline{CS} input low and ends with \overline{CS} going inactive. \overline{CS} must go inactive between data transfers. See the serial bus timing information in Section [10](#page-48-0) for details. All data transfers are terminated if the port's \overline{CS} input transitions high. Port control logic is disabled, and SDO is tri-stated when all $\overline{\text{CS}}$ pins are inactive.

Reading from or writing to the internal registers requires writing one address/command byte prior to the transferring register data. Two types of serial bus transfers exist, standard and burst. The standard serial bus access always consists of two bytes, an address/command byte that is always supplied by the user on SDI, and a data byte that can either be written to the DS21448 using SDI (write operation) or output by the DS21448 on SDO (read operation). The burst serial bus access consists of a single address/command byte followed either by 22 read or 22 write data bytes.

The first bit written (LSB) of the address/command byte specifies whether the access is to be a read (1) or a write (0). The next 5 bits identify the register address. Valid register addresses are 00h through 15h. Bit 7 is reserved and must be set to 0 for proper operation. Bit 8, the last bit (MSB) of the address/command byte, is the burst modeenable bit. When the burst bit is enabled (set to 0) and a READ operation is performed, the DS21448 automatically outputs the contents of registers 00h through 15h sequentially, starting with register address 00h. When the burst bit is enabled and a WRITE operation is performed, data supplied on SDI is sequentially written into the DS21448's register space starting at address 00h. Burst operation is stopped once address 15h is read or \overline{CS} goes inactive. For both burst read and burst write transfers, the address/command byte's register address bits must be set to 0.

The user can broadcast register write accesses to multiple ports simultaneously by enabling the desired channels' chip selects at the same time. However, only one port can be read at a time. Any attempt to read multiple ports simultaneously results in invalid data being returned on SDO.

Figure 4-2. Serial Port Operation for Read Access (R = 1) Mode 2

Figure 4-3. Serial Port Operation for Read Access (R = 1) Mode 3

Figure 4-4. Serial Port Operation for Read Access (R = 1) Mode 4

Figure 4-5. Serial Port Operation for Write Access (R = 0) Modes 1 and 2

Figure 4-6. Serial Port Operation for Write Access (R = 0) Modes 3 and 4

4.3 Parallel Port Operation

The option for either multiplexed bus operation (BIS0 = 0) or nonmultiplexed bus operation (BIS0 = 1) is available when using the parallel interface. The DS21448 can operate with either Intel or Motorola bus timing configurations. If the PBTS pin is wired low, Intel timing is selected; if wired high, Motorola timing is selected. All Motorola bus signals are listed in parentheses (). Four sets of identical register maps exist, one for each channel. See [Table 4-H](#page-17-4) for register names and addresses. Use the appropriate chip select $(\overline{CS1}, \overline{CS2}, \overline{CS3}, \overline{CS4})$ to access a channel's register map. See the timing diagrams in Section [10](#page-48-0) for more details. Hardware and serial port modes are not supported when using parallel port operation.

4.3.1 Device Power-Up and Reset

The DS21448 resets itself upon power-up, setting all writeable registers to 00h and clearing the status and information registers. CCR3.7 (TUA1) = 0 results in the LIU transmitting unframed all ones. After the power supplies have settled, initialize all control registers to the desired settings, then toggle the LIRST bit (CCR3.2). The DS21448 can at any time be reset to the default settings by bringing HRST low (level triggered) or by powering down and powering up again.

Table 4-G. Parallel Port Mode Selection

4.3.2 Register Map

[Table 4-H](#page-17-4) shows the typical register map for all four ports. Use the appropriate chip select (CS1, CS2, CS3, or CS4) to access a channel's register map.

Note 1: Register addresses 16h–1Fh do not exist.

4.3.3 Control Registers

CCR1 (00H): Common Control Register 1

CCR2 (01H): Common Control Register 2

CCR3 (02H): Common Control Register 3

CCR4 (03H): Common Control Register 4

Table 4-I. Receive Sensitivity Settings

CCR5 (04H): Common Control Register 5

Table 4-J. Backplane Clock Select

Table 4-K. Monitor Gain Settings

Table 4-L. Internal Rx Termination Select

CCR6 (05H): Common Control Register 6

5. STATUS REGISTERS

The three registers that contain information about the device's real-time status are the status register (SR) and receive information registers 1 and 2 (RIR1/RIR2). When a particular event has occurred (or is occurring), the appropriate bit in one of these registers is set to 1. Some bits in SR, RIR1, and RIR2 are latched bits and some are real-time bits (denoted in the following register descriptions). For latched status bits, when an event or an alarm occurs, the bit is set to 1 and remains set until the user reads that bit. The bit is cleared when it is read, and it is not set until the event has occurred again. Two of the latched status bits (RUA1 and RCL) remain set after reading if the alarm is still present.

The user always precedes a read of any of the three status registers with a write. The byte written to the register informs the DS21448 which bits the user wishes to read and have cleared. The user writes a byte to one of these registers with a 1 in the bit positions to be read and a 0 in the other bit positions. When a 1 is written to a bit location, that location is updated with the latest information. When a 0 is written to a bit position, that bit position is not updated, and the previous value is held. A write to the status and information registers is immediately followed by a read of the same register. The read result should be logically ANDed with the mask byte that was just written, and this value should be written back into the same register to ensure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously with respect to their access through the parallel port. This write-read-write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21448 with higher-order software languages.

The bits in the SR register have the unique ability to initiate a hardware interrupt through the \overline{INT} output pin. Each of the alarms and events in the SR can be either masked or unmasked from the interrupt pin through the interrupt mask register (IMR). The interrupts caused by the RCL, RUA1, and LOTC bits in the SR act differently than the interrupts caused by the other status bits in the SR. The RCL, RUA1, and LOTC bits forces the $\overline{\text{INT}}$ pin low whenever they change state (i.e., go active or inactive). The \overline{INT} pin is allowed to return high (if no other interrupts are present) when the user reads the alarm bit that caused the interrupt to occur, even if the alarm is still present. The other status bits in the SR can force the $\overline{\text{INT}}$ pin low when they are set. The $\overline{\text{INT}}$ pin is allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

The host can quickly determine which of the four LIU channels is generating an interrupt by reading one of the unused addresses in the 16h–1Fh range in any LIU channel. See the following LIU channel interrupt status description for additional information.

LIU Channel Interrupt Status

SR (06H): Status Register

Table 5-A. Received Alarm Criteria

Note 1: RCL is also known as a loss of signal (LOS) or Red Alarm in T1. **Note 2:** See CCR1.5 for details.

IMR (07H): Interrupt Mask Register

RIR1 (08H): Receive Information Register 1

RIR2 (09H): Receive Information Register 2

Table 5-B. Receive Level Indication

6. DIAGNOSTICS

6.1 In-Band Loop-Code Generation and Detection

The DS21448 can generate and detect a repeating bit pattern from 1 to 8 or 16 bits in length. To transmit a pattern, the user loads the pattern into the transmit code definition (TCD1 and TCD2) registers and selects the proper length of the pattern by setting the TC0 and TC1 bits in the in-band code control (IBCC) register. When generating a 1-, 2-, 4-, 8-, or 16-bit pattern, the transmit code registers (TCD1 and TCD2) must be filled with the proper code. Generation of a 1-, 3-, 5-, or 7-bit pattern only requires TCD1 to be filled. Once this is accomplished, the pattern is transmitted, as long as the TLCE control bit (CCR3.3) is enabled. For example, if the user wished to transmit the standard loop-up code for CSUs, which is a repeating pattern of ...10000100001..., then 80h would be loaded into TCD1, and the length would set using TC1 and TC0 in the IBCC register to 5 bits.

The DS21448 can detect two separate repeating patterns to allow for a loop-up code and a loop-down code to be detected. The user programs the codes in the receive-up code definition (RUPCD1 and RUPCD2) registers and the receive-down code definition (RDNCD1 and RDNCD2) registers; the length of each pattern is selected through the IBCC register. The DS21448 detects repeating pattern codes with bit-error rates as high as 1 x 10⁻². The code detector has a nominal integration period of 48ms, so after approximately 48ms of receiving either code, the proper status bit (LUP at SR.7 and LDN at SR.6) is set to 1. Normally codes are sent for a period of 5 seconds. It is recommended that the software poll the DS21448 every 100ms to 1000ms until 5 seconds has elapsed to ensure the code is continuously present.

IBCC (0AH): In-Band Code Control Register

Table 6-A. Transmit Code Length

Table 6-B. Receive Code Length

TCD1 (0BH): Transmit Code Definition Register 1

TCD2 (0CH): Transmit Code Definition Register 2

RUPCD1 (0DH): Receive-Up Code Definition Register 1

RUPCD2 (0EH): Receive-Up Code Definition Register 2

RDNCD1 (0FH): Receive-Down Code Definition Register 1

RDNCD2 (10H): Receive-Down Code Definition Register 2

6.2 Loopbacks

6.2.1 Remote Loopback (RLB)

When RLB (CCR6.6) is enabled, the DS21448 is placed into remote loopback. In this loopback, data from the clock/data recovery state machine is looped back to the transmit path, passing through the jitter attenuator if it is enabled. The data at the RPOS and RNEG pins is valid, while data presented at TPOS and TNEG is ignored. See [Figure 1-1](#page-4-1) for more details.

If the automatic RLB enable (CCR6.5) is set to 1, the DS21448 automatically goes into remote loopback when it detects the loop-up code programmed in the receive-up code definition registers (RUPCD1 and RUPCD2) for a minimum of 5 seconds. When the DS21448 detects the loop-down code programmed in the receive loop-down code definition registers (RDNCD1 and RDNCD2) for a minimum of 5 seconds, the DS21448 comes out of remote loopback. Setting ARLBE to 0 can also disable the ARLB.

6.2.2 Local Loopback (LLB)

When LLB (CCR6.7) is set to 1, the DS21448 is placed into local loopback. In this loopback, data on the transmit side is transmitted as normal. TCLK and TPOS/TNEG pass through the jitter attenuator (if enabled) and are output at RCLK and RPOS/RNEG. Incoming data from the line at RTIP and RRING is ignored. If transmit unframed all ones (CCR3.7) is set to 1 while in LLB, TTIP and TRING transmit all ones while TCLK and TPOS/TNEG are looped back to RCLK and RPOS/RNEG. See [Figure 1-1](#page-4-1) for more details.

6.2.3 Analog Loopback (LLB)

Setting ALB (CCR6.4) to 1 puts the DS21448 in analog loopback. Signals at TTIP and TRING are internally connected to RTIP and RRING. The incoming signals at RTIP and RRING are ignored. The signals at TTIP and TRING are transmitted as normal. See [Figure 1-1](#page-4-1) for more details.

6.2.4 Dual Loopback (DLB)

Setting CCR6.7 and CCR6.6 (LLB and RLB, respectively) to 1 puts the DS21448 into dual loopback operation. The TCLK and TPOS/TNEG signals are looped back through the jitter attenuator (if enabled) and output at RCLK and RPOS/RNEG. Clock and data recovered from RTIP and RRING are looped back to the transmit side and output at TTIP and TRING. This mode of operation is not available when implementing hardware operation. See [Figure 1-1](#page-4-1) more details.

6.3 PRBS Generation and Detection

Setting TPRBSE (CCR3.4) = 1 enables the DS21448 to transmit a 2^{15} - 1 (E1) or a QRSS (T1) PRBS, depending on the ETS bit setting in CCR1.7. The DS21448's receive side always searches for these PRBS patterns independently of CCR3.4. The PRBS bit-error output (PBEO) remains high until the receiver has synchronized to one of the two patterns (64 bits received without an error), at which time PBEO goes low, and the PRBSD bit in the SR is set. Once synchronized, any bit errors received cause a positive-going pulse at PBEO, synchronous with RCLK. This output can be used with external circuitry track bit-error rates during the PRBS testing. Setting CCR6.2 (ECRS2) = 1 allows the PRBS errors to be accumulated in the 16-bit counter in registers ECR1 and ECR2. The PRBS synchronizer remains in sync until it experiences six bit errors or more within a 64-bit span. Both PRBS patterns comply with the ITU-T O.151 specifications.

6.4 Error Counter

Error count register 1 (ECR1) is the most significant word and ECR2 is the least significant word of a userselectable 16-bit counter that records incoming errors, including BPVs, code violations (CVs), excessive zero violations (EXZs), and/or PRBS errors. See [Table 6-C,](#page-31-2) [Table 6-D,](#page-31-3) and [Figure 1-2](#page-5-0) for details.

Table 6-C. Definition of Received Errors

Table 6-D. Function of ECRS Bits and RNEG Pin

Note 1: RNEG outputs error data only when in NRZ mode (CCR1.6 = 1).

Note 2: PRBS errors are always output at PBEO, independent of ECR control bits and NRZ mode, and are not present at RNEG.

6.5 Error Counter Update

A 0-to-1 transition of the ECUE (CCR1.4) control bit updates the ECR registers with the current values and resets the counters. ECUE must be set back to 0 and another 0-to-1 transition must occur for subsequent reads/resets of the ECR registers. Note that the DS21448 can report errors at RNEG when in NRZ mode (CCR1.6 = 1) by outputting a pulse for each error occurrence. The counter saturates at 65,535 and does not roll over.

ECR1 (11H): Upper Error Count Register 1/ECR2 (12H): Lower Error Count Register 2

6.6 Error Insertion

When IBPV (CCR3.1) is transitioned from 0 to 1, the device waits for the next occurrence of three consecutive 1s to insert a BPV. IBPV must be cleared and set again for another BPV error insertion. See [Figure 1-3](#page-5-1) for details on the insertion of the BPV into the data stream.

When IBE (CCR3.0) is transitioned from 0 to 1, the device inserts a logic error. IBE must be cleared and set again for another logic error insertion. See [Figure 1-2](#page-5-0) and [Figure 1-3](#page-5-1) for details about the logic error insertion into the data steam.

7. ANALOG INTERFACE

7.1 Receiver

The DS21448 contains a digital clock recovery system. The DS21448 couples to the receive E1 or T1 twisted pair (or coaxial cable in 75 Ω E1 applications) through a 1:1 transformer. See [Table 7-C](#page-34-0) for transformer details. [Figure 7-1,](#page-35-0) [Figure 7-2,](#page-36-0) [Figure 7-3,](#page-37-0) and [Table 4-L](#page-21-3) show the receive termination requirements. The DS21448 has the option of using internal termination resistors.

The DS21448 is designed to be fully software selectable for E1 and T1 without the need to change any external resistors for the receive side. The receive side allows user configuration for 75Ω, 100Ω, or 120Ω receive termination by setting the RT1 (CCR5.1) and RT0 (CCR5.0) bits. When using the internal termination feature, the R_r resistors should be 60Ω each. See [Figure 7-1](#page-35-0) for details. If external termination is required, RT1 and RT0 should be set to 0, and both R_r resistors [\(Figure 7-1\)](#page-35-0) should be 37.5Ω, 50Ω, or 60Ω each, depending on the line impedance.

The resultant E1 or T1 clock derived from the 2.048/1.544 PLL (JACLK in [Figure 1-1\)](#page-4-1) is internally multiplied by 16 through another internal PLL and fed to the clock recovery system. The clock recovery system uses the clock from the PLL circuit to form a 16-times oversampler used to recover the clock and data. This oversampling technique offers outstanding performance to meet jitter tolerance specifications, as shown in [Figure 7-7](#page-41-0).

Normally, the clock that is output at the RCLK pin is the recovered clock from the E1 AMI/HDB3 or T1 AMI/B8ZS waveform presented at the RTIP and RRING inputs. When no signal is present at RTIP and RRING, an RCL condition occurs, and the RCLK is derived from the JACLK source. See [Figure 1-1](#page-4-1) for more details. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to an approximate 50% duty cycle. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLK output can exhibit slightly shorter high cycles of the clock. This is because of the highly oversampled digital clock recovery circuitry. See the receive-side AC timing characteristics in Section [10](#page-48-0) for more details.

The receive-side circuitry also contains a clock synthesizer that outputs a user-configurable clock (up to 16.384MHz) synthesized from RCLK at BPCLK (pin 31). See [Table 4-J](#page-21-1) for details about output clock frequencies at BPCLK. In hardware mode, BPCLK defaults to a 16.384MHz output.

The DS21448 has a bypass mode for the receive-side clock and data. This allows the BPCLK to be derived from RCLK after the jitter attenuator, while the clock and data presented at RCLK, RPOS, and RNEG go unaltered. This is intended for applications where the receive-side jitter attenuation is done after the LIU. Setting RJAB (CCR6.3) to logic 1 enables the bypass. Ensure the jitter attenuator is in the receive path (CCR4.3 = 0). See [Figure 1-1](#page-4-1) for more details.

The DS21448 reports the signal strength at RTIP and RRING in 2.5dB increments through RL3–RL0 located in the receive information register 2. This feature is helpful when troubleshooting line performance problems [\(Table 5-B](#page-26-0)).

E1 and T1 monitor applications require various flat-gain settings for the receive-side circuitry. The DS21448 can be programmed to support these applications through the monitor mode control bits MM1 and MM0. When the monitor modes are enabled, the receiver tolerates normal line loss up to -6dB [\(Table 4-K](#page-21-2)).

7.2 Transmitter

The DS21448 uses a set of laser-trimmed delay lines with a precision digital-to-analog converter (DAC) to create the waveforms that are transmitted onto the E1 or T1 line. The waveforms meet the latest ETSI, ITU, ANSI, and AT&T specifications. The user selects which waveform to generate by setting the ETS bit (CCR1.7) for E1 or T1 operation, then programming the L2/L1/L0 bits in common control register 4 for the appropriate application. See [Table 7-A](#page-33-2) and [Table 7-B](#page-33-3) for the proper L2/L1/L0 settings.

A 2.048MHz or 1.544MHz TTL clock is required at TCLK for transmitting data at TPOS and TNEG. ITU specification G.703 requires ±50ppm accuracy for T1 and E1. TR62411 and ANSI specs require ±32ppm accuracy for T1 interfaces. The clock can be sourced internally by RCLK or JACLK. See CCR1.2, CCR1.1, CCR1.0, and [Figure 1-3](#page-5-1) for details. Because of the transmitter's design, very little jitter (less than 0.005UI_{P-P} broadband from 10Hz to 100kHz) is added to the jitter present on TCLK. Also, the waveforms created are independent of the duty cycle of TCLK. The transmitter couples to the E1 or T1 transmit-twisted pair (or coaxial cable in some E1 applications) through a 1:2 step-up transformer. For the device to create the proper waveforms, the transformer used must meet the specifications listed in [Table 7-C.](#page-34-0)

The DS21448 has an automatic short-circuit limiter that limits the source current to 50mA (RMS) into a 1Ω load. This feature can be disabled by setting the SCLD bit (CCR2.5) = 1. When the current limiter is activated, TCLE (SR.2) is set even if the short-circuit limiter is disabled. The TPD bit (CCR4.0) powers down the transmit-line driver and tri-states the TTIP and TRING pins. The DS21448 can also detect when the TTIP or TRING outputs are open circuited. When an open circuit is detected, TOCD (SR.1) is set.

7.3 Jitter Attenuator

The DS21448 contains an on-board jitter attenuator that can be set to a depth of either 32 or 128 bits through the JABDS bit (CCR4.2). The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay-sensitive applications. [Figure 7-8](#page-41-1) shows the attenuation characteristics. The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit (CCR4.3). Also, setting the DJA bit (CCR4.1) can disable the jitter attenuator (in effect, remove it). For the jitter attenuator to operate properly, a 2.048MHz or 1.544MHz clock must be applied at MCLK. ITU specification G.703 requires ±50ppm accuracy for T1 and E1. TR62411 and ANSI specs require ±32ppm accuracy for T1 interfaces. An on-board PLL for the jitter attenuator converts the 2.048MHz clock to a 1.544MHz rate for T1 applications. Setting JAMUX (CCR1.3) to logic 0 bypasses this PLL. On-board circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLK pin to create a smooth jitter-free clock, which is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLK pin if the jitter attenuator is placed on the transmit side. If the incoming jitter exceeds either 120UI_{P-P} (buffer depth is 128 bits) or 28UI_{P-P} (buffer depth is 32 bits), the DS21448 divides the internal nominal 32.768MHz (E1) or 24.704MHz (T1) clock by either 15 or 17 instead of the normal 16 to keep the buffer from overflowing. When the device divides by either 15 or 17, it also sets the JALT bit in the receive information register 1 (RIR1).

7.4 G.703 Synchronization Signal

The DS21448 can receive a 2.048MHz square-wave synchronization clock, as specified in Section 10 of ITU G.703. To use the DS21448 in this mode, set the receive-synchronization-clock enable (CCR5.3) = 1. The DS21448 can also transmit the 2.048MHz square-wave synchronization clock, as specified in Section 10 of G.703. To transmit the 2.048MHz clock, set the transmit-synchronization-clock enable (CCR5.2) = 1.

Table 7-B. Line Build-Out Select for T1 in Register CCR4 (ETS = 1)

Note: See [Figure 7-1](#page-35-0), [Figure 7-2](#page-36-0), and [Figure 7-3.](#page-37-0) N.M. = Not meaningful.

Table 7-C. Line Build-Out Select for E1 in Register CCR4 (ETS = 0) Using Alternate Transformer Configuration

Note: See [Figure 7-4](#page-38-0).

Table 7-D. Transformer Specifications (3.3V Operation)

Figure 7-1. Basic Interface

Figure 7-2. Protected Interface Using Internal Receive Termination

Figure 7-3. Protected Interface Using External Receive Termination

Figure 7-4. Dual Connector-Protected Interface Using Receive Termination

Figure 7-5. E1 Transmit Pulse Template

Figure 7-6. T1 Transmit Pulse Template

Figure 7-7. Jitter Tolerance

Figure 7-8. Jitter Attenuation

8. JTAG BOUNDARY SCAN ARCHITECTURE AND TEST ACCESS PORT

The DS21448 IEEE 1149.1 design supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE [\(Table 8-A](#page-44-1)). The DS21448 contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port (TAP) and Boundary Scan Architecture:

Test Access Port TAP Controller Instruction Register Bypass Register Boundary Scan Register Device Identification Register

The TAP has the necessary interface pins JTRST, JTCLK, JTMS, JTDI, and JTDO. See the pin descriptions in Section [1](#page-6-0) for details. Details on Boundary Scan Architecture and the Test Access Port can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

Figure 8-1. JTAG Block Diagram

8.1 JTAG TAP Controller State Machine

This section covers the operation of the TAP controller state machine. See [Figure 8-2](#page-43-0) for details on each of the states described below. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK [\(Table 8-B](#page-45-1)).

Test-Logic-Reset. Upon power-up, the TAP controller is in test-logic-reset state. The instruction register contains the IDCODE instruction. All system logic of the device operates normally.

Run-Test-Idle. The run-test-idle is used between scan operations or during specific tests. The instruction register and test registers remain idle.

Select-DR-Scan. All test registers retain their previous state. With JTMS LOW, a rising edge of JTCLK moves the controller into the capture-DR state and initiates a scan sequence. JTMS HIGH during a rising edge on JTCLK moves the controller to the select-IR-scan state.

Figure 8-2. TAP Controller State Diagram

Capture-DR. Data can be parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register remains at its current value. On the rising edge of JTCLK, the controller goes to the shift-DR state if JTMS is LOW, or it goes to the exit1-DR state if JTMS is HIGH.

Shift-DR. The test data register selected by the current instruction is connected between JTDI and JTDO, and shifts data one stage toward its serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on JTCLK puts the controller in the update-DR state, which terminates the scanning process, if JTMS is HIGH. A rising edge on JTCLK with JTMS LOW puts the controller in the pause-DR state.

Pause-DR. Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is LOW. A rising edge on JTCLK with JTMS HIGH puts the controller in the exit2-DR state.

Exit2-DR. A rising edge on JTCLK with JTMS HIGH while in this state puts the controller in the update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS LOW enters the shift-DR state.

Update-DR. A falling edge on JTCLK while in the update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register.

Select-IR-Scan. All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS LOW, a rising edge on JTCLK moves the controller into the capture-IR state and initiates a scan sequence for the instruction register. JTMS HIGH during a rising edge on JTCLK puts the controller back into the test-logic-reset state.

Capture-IR. The capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is HIGH on the rising edge of JTCLK, the controller enters the exit1-IR state. If JTMS is LOW on the rising edge of JTCLK, the controller enters the shift-IR state.

Shift-IR. In this state, the shift register in the instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK toward the serial output. The parallel register and all test registers remain at their previous states. A rising edge on JTCLK with JTMS HIGH moves the controller to the exit1-IR state. A rising edge on JTCLK with JTMS LOW keeps the controller in the shift-IR state while moving data one stage through the instruction shift register.

Exit1-IR. A rising edge on JTCLK with JTMS LOW puts the controller in the pause-IR state. If JTMS is HIGH on the rising edge of JTCLK, the controller enters the update-IR state and terminates the scanning process.

Pause-IR. Shifting of the instruction shift register is halted temporarily. With JTMS HIGH, a rising edge on JTCLK puts the controller in the exit2-IR state. The controller remains in the pause-IR state if JTMS is LOW during a rising edge on JTCLK.

Exit2-IR. A rising edge on JTCLK with JTMS HIGH puts the controller in the update-IR state. The controller loops back to shift-IR if JTMS is LOW during a rising edge of JTCLK in this state.

Update-IR. The instruction code shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS LOW puts the controller in the run-test-idle state. With JTMS HIGH, the controller enters the select-DR-scan state.

8.2 Instruction Register

The instruction register contains a shift register, as well as a latched parallel output, and is 3 bits in length. When the TAP controller enters the shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the shift-IR state, a rising edge on JTCLK with JTMS LOW shifts the data one stage toward the serial output at JTDO. A rising edge on JTCLK in the exit1-IR state or the exit2-IR state with JTMS HIGH moves the controller to the update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. [Table 8-A](#page-44-1) shows the instructions supported by the DS21448 and its respective operational binary codes.

SAMPLE/PRELOAD. This is a mandatory instruction for the IEEE 1149.1 specification that supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device by using the capture-DR state. SAMPLE/PRELOAD also allows the device to shift data into the boundary scan register through JTDI using the shift-DR state.

BYPASS. When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the 1-bit bypass test register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

EXTEST. This allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled through the update-IR state, the parallel outputs of all digital output pins are driven. The boundary scan register is connected between JTDI and JTDO. The capture-DR samples all digital inputs into the boundary scan register.

CLAMP. All digital outputs of the device are output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

HIGHZ. All digital outputs of the device are placed in a high-impedance state. The BYPASS register is connected between JTDI and JTDO.

IDCODE. When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code is loaded into the identification register on the rising edge of JTCLK following entry into the capture-DR state. Shift-DR can be used to shift the identification code out serially through JTDO. During test-logic-reset, the identification code is forced into the instruction register's parallel output. The ID code always has a 1 in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version [Table 8-B.](#page-45-1) [Table 8-C](#page-45-2) lists the device ID code for the SCT devices.

Table 8-B. ID Code Structure

Table 8-C. Device ID Codes

8.3 Test Registers

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register, the identification register, has been included with the DS21448 design. It is used with the IDCODE instruction and the test-logic-reset state of the TAP controller.

Bypass Register

The bypass register is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions that provides a short path between JTDI and JTDO.

Identification Register

The identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the test-logic-reset state. See [Table 8-B](#page-45-1) and [Table 8-C](#page-45-2) for more information about bit usage.

Boundary Scan Register

The boundary scan register contains a shift register path and a latched parallel output for all control cells and digital I/O cells, and is n bits in length. See [Table 8-D](#page-46-0) for all cell bit locations and definitions.

Table 8-D. Boundary Scan Control Bits

DS21448 3.3V T1/E1/J1 Quad Line Interface

Note 1: 0 = Dn/ADn are inputs; 1 = Dn/ADn are outputs. **Note 2:** $0 = \overline{INT}$ is an input; $1 = \overline{INT}$ is an output.

9. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground \sim 1.0V to +6.0V to +6.0V Operating Temperature Range for DS21448TN

Storage Temperature Range
 -40° C to +125°C Storage Temperature Range Soldering Temperature Soldering Temperature See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

 $(T_A = -40^{\circ}C \text{ to } +85^{\circ}C)$

CAPACITANCE

 $(T_A = +25^{\circ}C)$

DC CHARACTERISTICS

(V_{DD} = 3.3V \pm 5%, T_A = -40°C to +85°C.)

Note 1: Applies to V_{DD}.

Note 2: 0.0V < V_{IN} < V_{DD} .

Note 3: Applied to INT when tri-stated.

Note 4: TCLK = MCLK = 2.048MHz.

Note 5: Power dissipation with all ports active, TTIP and TRING driving a 30Ω load, for an all-ones data density.

10. AC TIMING PARAMETERS AND DIAGRAMS

Table 10-A. AC Characteristics—Multiplexed Parallel Port (BIS0 = 0)

Figure 10-1. Intel Bus Read Timing (PBTS = 0, BIS0 = 0)

Figure 10-2. Intel Bus Write Timing (PBTS = 0, BIS0 = 0)

Table 10-B. AC Characteristics—Nonmultiplexed Parallel Port (BIS0 = 1)

 $(V_{DD} = 3.3V \pm 5\%, T_A = -40^{\circ}C$ to +85°C.) [\(Figure 10-4](#page-50-0), [Figure 10-5,](#page-51-0) [Figure 10-6,](#page-51-1) and [Figure 10-7\)](#page-51-2)

Figure 10-4. Intel Bus Read Timing (PBTS = 0, BIS0 = 1)

Figure 10-5. Intel Bus Write Timing (PBTS = 0, BIS0 = 1)

Figure 10-6. Motorola Bus Read Timing (PBTS = 1, BIS0 = 1)

Figure 10-7. Motorola Bus Write Timing (PBTS = 1, BIS0 = 1)

Table 10-C. AC Characteristics—Serial Port (BIS1 = 1, BIS0 = 0)

 $(V_{DD} = 3.3V \pm 5\%, T_A = -40^{\circ}C$ to +85°C.) [\(Figure 10-8](#page-52-0))

Figure 10-8. Serial Bus Timing (BIS1 = 1, BIS0 = 0)

Table 10-D. AC Characteristics—Receive Side

 $(V_{DD} = 3.3V \pm 5\%, T_A = -40^{\circ}C$ to +85°C.) [\(Figure 10-9](#page-53-0))

Note 1: E1 mode.

Note 2: T1 or J1 mode.

Note 3: Jitter attenuator enabled in the receive path.

Note 4: Jitter attenuator disabled or enabled in the transmit path.

Figure 10-9. Receive-Side Timing

Table 10-E. AC Characteristics—Transmit Side

 $(V_{DD} = 3.3V \pm 5\%, T_A = -40\degree C$ to +85°C.) [\(Figure 10-10\)](#page-54-0)

Note 5: E1 mode. **Note 6:** T1 or J1 mode.

Figure 10-10. Transmit-Side Timing

11. PIN CONFIGURATIONS

11.1 144-Pin TE-PBGA

ALE (AS)/SCLKE
RRING4 ALE (AS)/SCLKE D2/AD2/LOOP1
D3/AD3/LOOP0 **WR(RW)/NRZE** WR(R/W)/NRZE D3/AD3/LOOP0 D2/AD2/LOOP1 D1/AD1/MM0 TCLK3
D0/AD0/MM1 D1/AD1/MM0 TXDIS/TEST D0/AD0/MM1 D4/AD4/TX1 D5/AD5/TX0 D7/AD7/CES D6/AD6/TPD D4/AD4/TX1 D5/AD5/TX0 RDD_S)/ETS CS3EGL3 RCLK4 TRING3 TVDD3 TVSS3 RT1 / A0/HBE
A1/JAS RTIP4 VSS4 VDD4 TTIP3 VSS4 VDD4 VDD4 VSS4 a
E. d. d. d.
H. z. z. z. N.C. N.C. BIS1 N.C. INT \blacksquare $\sqrt{2}$ A2/OCES/JAMUX TVSS4 \blacksquare 100 90 80 70 TVDD4 A3/ICES/DJA \Box TRING4 A4/SD0/L0 \overline{C} RRING3 **HRST** \Box **BIS0** 60 RTIP3 \Box PBTS/RT0 TNEG4 \Box MCLK \Box RCLK3 PBEO1 CS2EGL2 \mathbf{r} 110 PBEO2 BPCLK3 Γ BPCLK4 TPOS4 \Box VSS3 TCLK4 \Box CS4EGL4 *Dallas Semiconductor* VSS3 \Box VDD1 VSS3 Γ *DS21448* VDD1 VDD3 \Box VDD1 \Box 50 VDD3 VSS1 VDD3 \Box VSS1 JTMS $\overline{}$ VSS1 \Box BPCLK2 120 PBEO3 JTDO $\overline{}$ BPCLK1 \Box JTDI PBEO4 JTCLK \Box RTIP1 TCLK2 \Box RRING1 JTRST \Box RCL1/LOTC1 \Box TRING2 TVDD2 RCLK1 Γ 40 \Box RCL2/LOTC2 \Box $\overline{}$ TVSS2 110 20 30 Ш \Box RCL4/LOTC4
RCL3/LOTC3 TTIP2 RPOS1 RNEG3 N.C. TTIP1 RPOS3 VDD2
CSTEGL1
CSTEGL1
RPOS4
RPOS4 RCL3/LOTC3 RCL4/LOTC4 n.c.
N.c.
N.c. TVSS1 TVDD1 TRING1 RNEG
ROS
RNEG
RNEG VDD2 VSS2 VSS2 VSS2 RNEG4 TPOS1 TNEG1 RTIP2 RRING2 TPOS2 RCLK2 TNEG2 TPOS3 TNEG3 SDI/L1 SCLK/L2

11.2 128-Pin LQFP

12. PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information.)

12.1 144-Ball TE-PBGA ([56-G6020-001\)](http://www.maxim-ic.com/package_drawings/56-G6020-001.pdf)

12.2 128-Pin LQFP ([56-G4011-001\)](http://www.maxim-ic.com/package_drawings/56-G4011-001.pdf)

13. THERMAL INFORMATION

Table 13-A. Thermal Characteristics—BGA

Table 13-B. Theta-JA (θ**JA) vs. Airflow—BGA**

Table 13-C. Thermal Characteristics—LQFP

Table 13-D. Theta-JA (θ**JA) vs. Airflow—LQFP**

Note 1: The package is mounted on a four-layer JEDEC-standard test board.

Note 2: Theta-JA (θ_{JA}) is the junction-to-ambient thermal resistance, when the package is mounted on a four-layer JEDEC-standard test board.

Note 3: While Theta-JC (θ_{JC}) is commonly used as the thermal parameter that provides a correlation between the junction temperature (Tj) and the average temperature on top center of the LQFP package (TC), the proper term is Psi-JT. It is defined by: (Tj - TC) / overall package power.

Note 4: The method of measurement for the thermal parameters is defined in the EIA/JEDEC-standard document EIA-JESD51-2.

14. REVISION HISTORY

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