

STRUCTURE : Silicon Monolithic Integrated Circuit
 PRODUCT SERIES : Power Driver for Compact Disc Player
 TYPE : BA5969FP
 PACKAGE OUTLINES : fig.1 (Plastic Mold)
 POWER DISSIPATION : fig.2
 BLOCK DIAGRAM : fig.3
 APPLICATION : fig.4
 TEST CIRCUIT : fig.5,6

FUNCTION:

- 4 channel BTL driver, 1channel reversible driver.
- Small surface mounting power package (HSOP-28).
- Thermal-shut-down circuit built in.
- Wide dynamic range (6.0V(Typ.) at VCC=8V,RL=8).

 <BTL driver>

- Input pins consist of (+) and (-), therefore various input types are available such as differential input(CH3, 4).

 <Loading driver>

- Brake circuit built in.
- Circuit protection diode built in.
- The output voltage is adjustable by output voltage control terminal. (Only "H" side Voltage)

ABSOLUTE MAXIMUM RATINGS (Ta = 25)

Parameter	Symbol	Limit	Unit
Supply Voltage	Vcc	13.5	V
Power dissipation	Pd	1.7 *1	W
Operating temperature	Topr	-40 ~ 85	
Storage temperature	Tstg	-55 ~ 150	

*1) On less than 3% (percentage occupied by copper foil),70 × 70mm², t=1.6mm, glass epoxy mounting. Reduce power by 13.6mW for each degree above 25 .

GUARANTEED OPERATING RANGES

VCC	4.3 ~ 9V
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Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

ELECTRICAL CHARACTERISTICS

 (Unless otherwise note, $T_a = 25$, $V_{cc}=8V$, $BIAS=2.5V$, $R_L=8$)

Parameter	Symbol	MIN	TYP	MAX	Unit	Condition	test circuit
Quiescent current	ICC	-	24	34	mA	$R_L=$	fig.5
< BTL driver >							
Output offset voltage	VOO	-50	0	50	mV		fig.6
Max. output voltage	VOM	5.4	6.0	-	V		fig.6
Closed loop voltage gain	GVC	14.0	16.1	18.0	dB		fig.6
Mute on voltage	VMTON	-	-	0.5	V		fig.5
Mute off voltage	VMTOFF	1.5	-	-	V		fig.5
Input current for Mute pin	IMUTE	-	180	270	μA	$VMUTE=5V$	fig.5
Bias mute on voltage	VBMUTE ON	-	-	0.5	V		fig.5
Bias mute off voltage	VBMUTE OFF	1.1	-	-	V		fig.5
Input current for Bias pin	IBIAS	-	75	120	μA	$VBIAS=2.5V$	fig.5
< OP-AMP >							
Common mode input voltage range	VICM	0.5	-	6.8	V		fig.6
Input offset voltage	VOFOP	-6	0	6	mV		fig.6
Input bias current	IBOP	-	-	300	nA		fig.6
High level output voltage	VOHOP	7.5	-	-	V		fig.6
Low level output voltage	VOLOP	-	-	0.5	V		fig.6
Output sink current	ISIN	1	-	-	mA	Output to VCC by 50	fig.6
Output source current	ISOU	1	-	-	mA	Output to GND by 50	fig.6
Slew rate	SROP	-	1	-	V/ μs	Input pulse 100KHz, 2Vp-p	fig.6
< Loading driver >							
Output saturation voltage 1	VSAT1	0.6	0.9	1.4	V	Upper+Lower saturation, $I_L=200mA$	fig.6
Output saturation voltage between F&R	VSAT1	-	-	0.1	V	Output saturation voltage 1 between FWD and REV	fig.6
Output saturation voltage 2	VSAT2	0.7	1.2	2.0	V	Upper+Lower saturation, $I_L=500mA$	fig.6
Voltage gain	LGVC	6.6	8.6	10.6	dB	VOLD/ VLDCTL (VLDCTL=2V)	fig.6
< Loading driver input logic >							
Input high level voltage	VIHLD	1.5	-	VCC	V		fig.5
Input low level voltage	VILLD	-0.3	-	0.5	V		fig.5
Input high level current	IIHLD	-	180	270	μA	$VFWD=VREV=5V$	fig.5

This product is not designed for protection against radioactive rays.

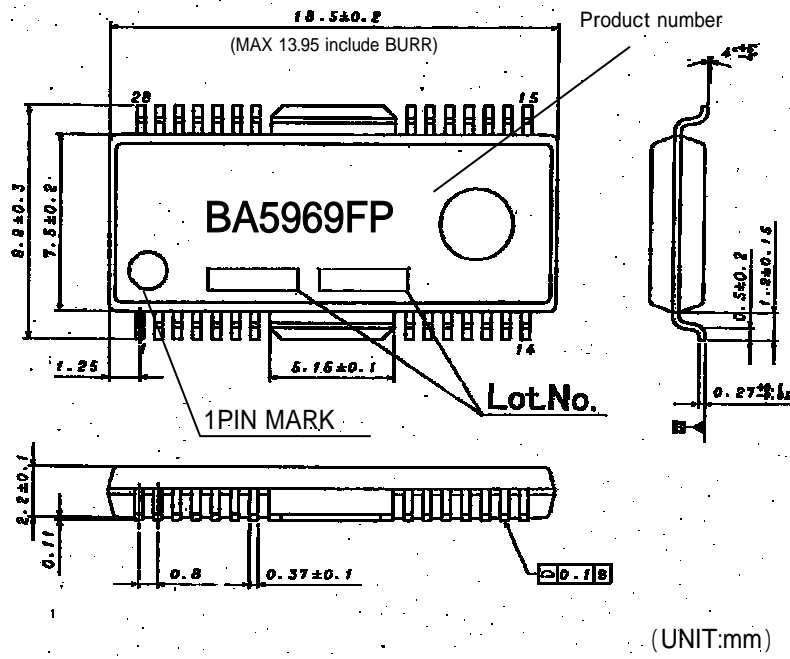
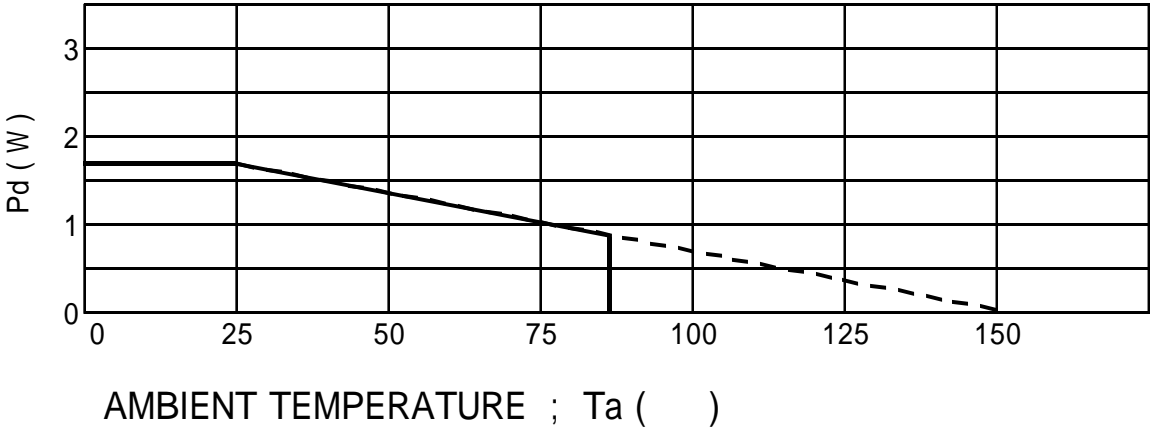


fig.1 PACKAGE OUTLINES

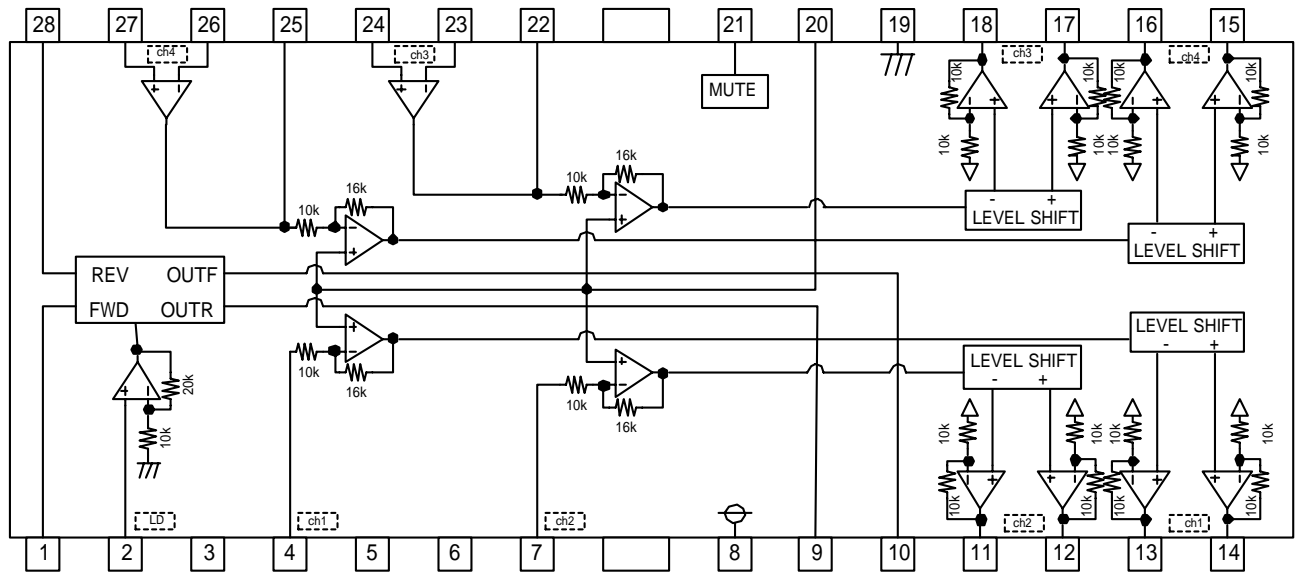
Electrical characteristic curves



Pd ; power dissipation

* On less than 3% (percentage occupied by copper foil),70 × 70mm², t=1.6mm, glass epoxy mounting.

fig.2 POWER DISSIPATION



resistor unit []

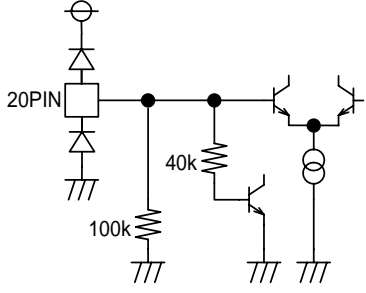
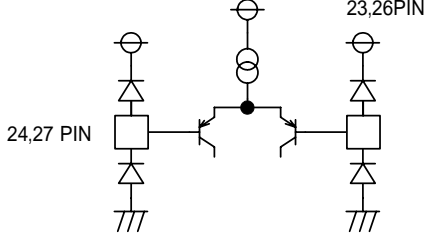
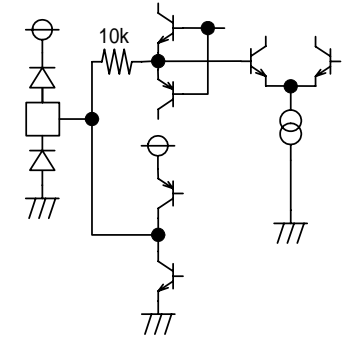
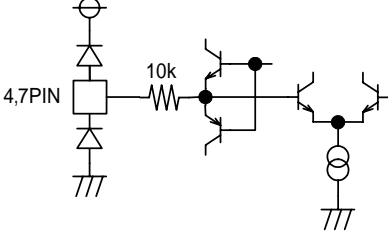
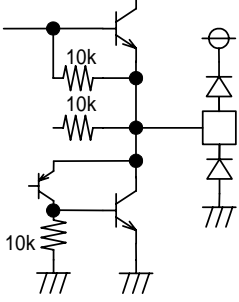
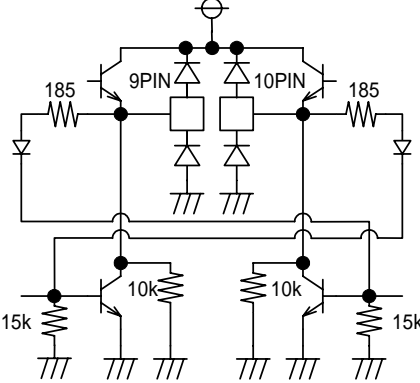
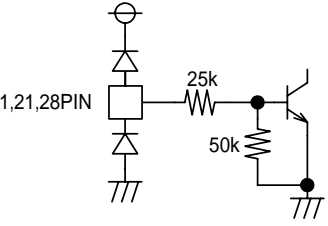
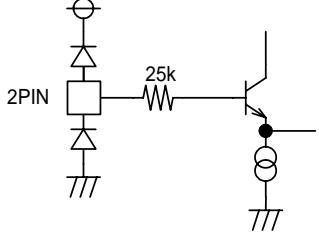
fig.3 BLOCK DIAGRAM

Pin description

No	Symbol	Function	No	Symbol	Function
1	FWD	Input for loading forward	15	VO4(+)	Non inverted output of CH4
2	LDCTL	Loading driver output voltage control terminal	16	VO4(-)	Inverted output of CH4
3	TEST	TEST	17	VO3(+)	Non inverted output of CH3
4	IN1	Input of CH1	18	VO3(-)	Inverted output of CH3
5	TEST	TEST	19	GND	Substrate ground
6	TEST	TEST	20	BIAS	Input for Bias-amplifier
7	IN2	Input of CH2	21	MUTE	Input for mute control
8	VCC	VCC	22	OPOUT3	Output of CH3 OP-AMP
9	VOL(-)	Inverted output of loading	23	OPIN3(-)	Inverting input of CH3 OP-AMP
10	VOL(+)	Non inverted output of loading	24	OPIN3(+)	Non inverting input of CH3 OP-AMP
11	VO2(-)	Inverted output of CH2	25	OPOUT4	Output of CH4 OP-AMP
12	VO2(+)	Non inverted output of CH2	26	OPIN4(-)	Inverting input of CH4 OP-AMP
13	VO1(-)	Inverted output of CH1	27	OPIN4(+)	Non inverting input of CH4 OP-AMP
14	VO1(+)	Non inverted output of CH1	28	REV	Input for loading reverse

notes) Symbol of + and - (output of drivers) means polarity to input pin.
 (For example if voltage of pin4 high, pin14 is high)

EQUIVALENT CIRCUIT OF TERMINALS

<p style="text-align: center;">BIAS</p> 	<p style="text-align: center;">ch3,4 input for OP-AMP</p> 
<p style="text-align: center;">ch3,4 output for OP-AMP & Input for BTL driver</p> <p>22,25 PIN</p> 	<p style="text-align: center;">ch1,2 input for BTL driver</p> <p>4,7PIN</p> 
<p style="text-align: center;">Output for BTL driver</p>  <p style="margin-left: 200px;">Non inverted output 12,14,15,17 PIN</p> <p style="margin-left: 200px;">Inverted output 11,13,16,18 PIN</p>	<p style="text-align: center;">Output for loading driver</p> 
<p style="text-align: center;">Input for Mute·loading driver</p> <p>1,21,28PIN</p> 	<p style="text-align: center;">LDCTL</p> <p>2PIN</p> 

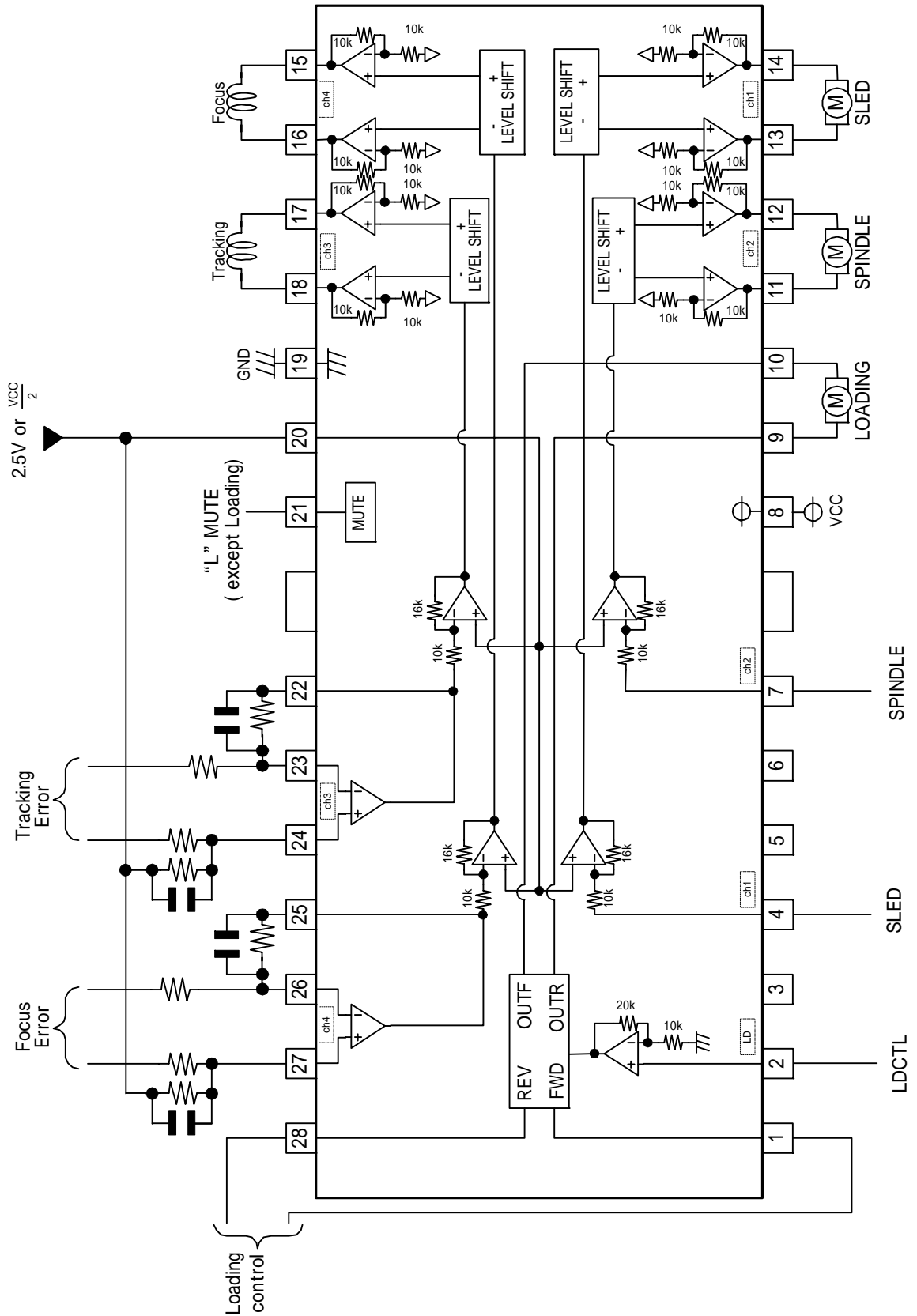


fig.4 APPLICATION

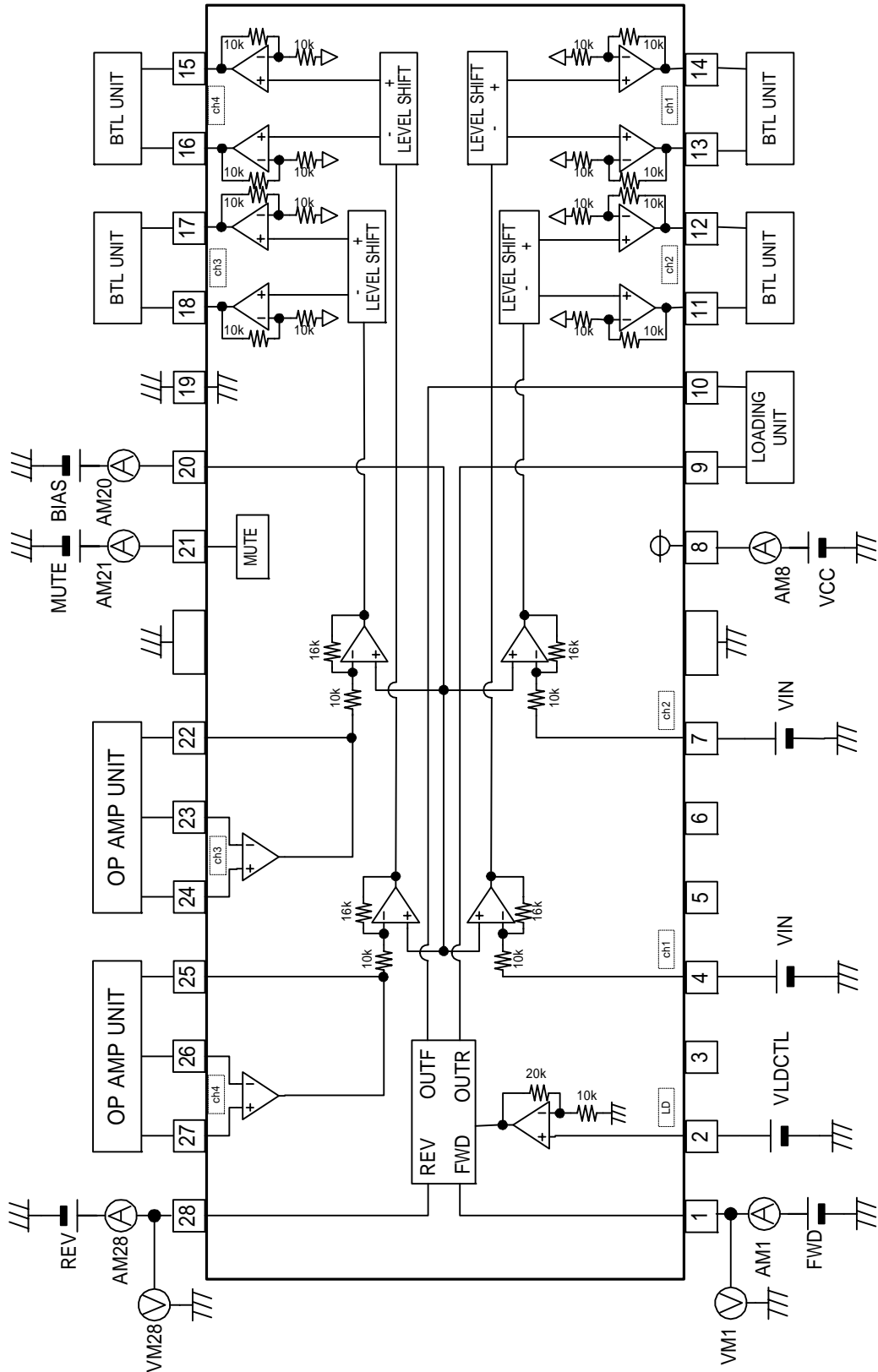


fig.5 Test Circuit (Unit, exclude)

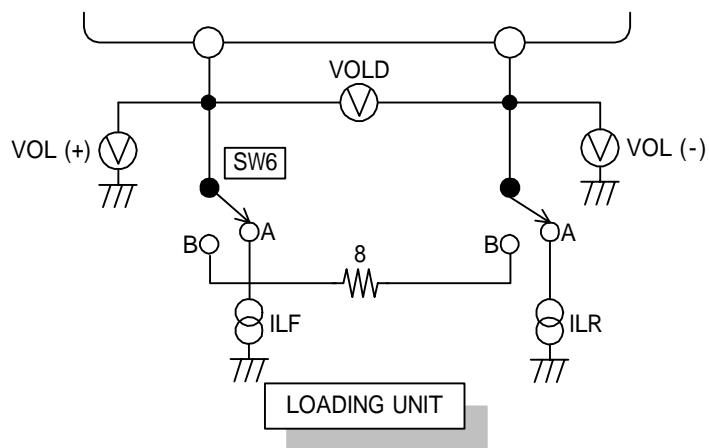
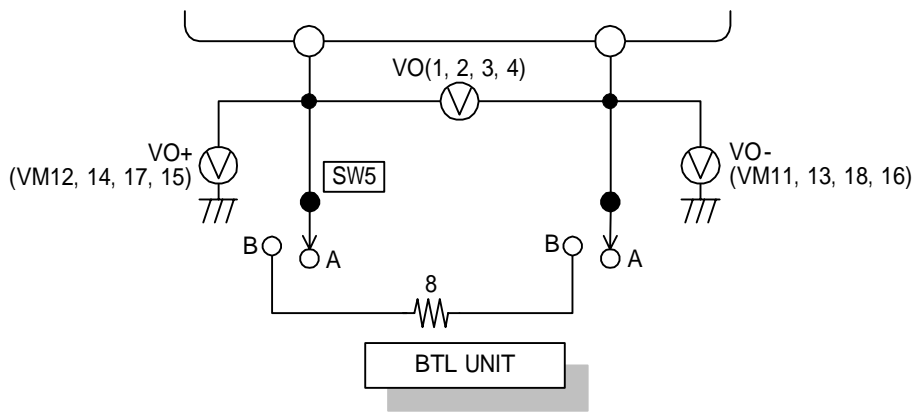
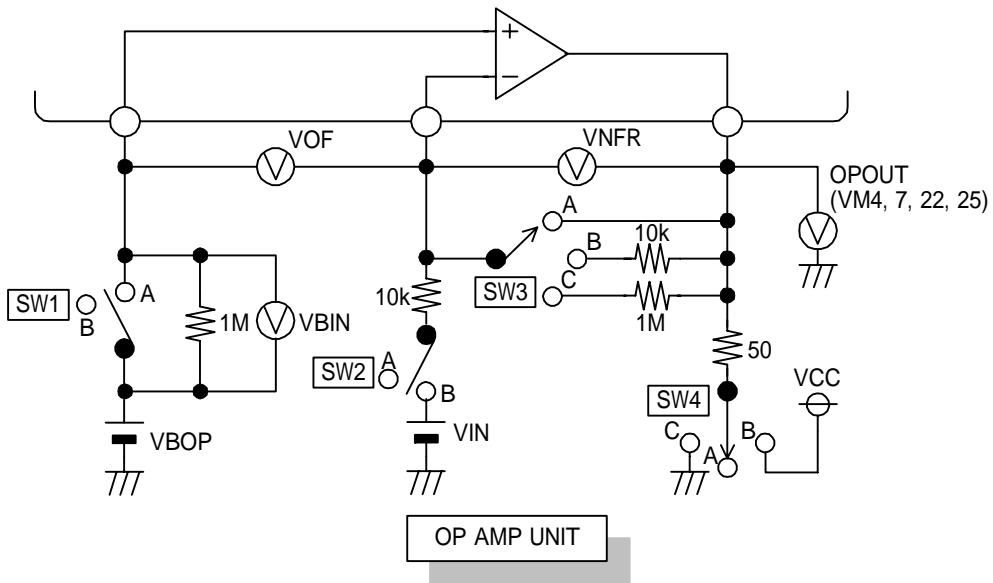


fig.6 Test Circuit (each unit)

SWITCH TABLE

Unless otherwise noted, VCC=8V, BIAS=2.5V, SW ; A position

	Switch						Input Voltage (V), Current (mA)					Conditions	Measure point
	1	2	3	4	5	6							
<Circuit current> (MUTE=3V, VBOP=2.5V)													
Quiescent current													AM8
<BTL DRIVER>	1	2	3	4	5	6	MUTE	BIAS	VBOP	VIN			
Output offset voltage					B		3	2.5	2.5	-			VO
Max. output voltage		B	C							0			VO
										8			VO
Closed loop voltage gain									3	-			VO
									2	-			VO
Mute on voltage							0.5		3	-			VO
Mute off voltage							1.5		3	-			VO
Bias mute on voltage							3	0.5	3	-			VO
Bias mute off voltage								1.1		-			VO
Input current for Mute pin							5		2.5	-	input parameter		AM21
Input current for Bias pin										-	input parameter		AM20
<OP-AMP> (MUTE=3V)	1	2	3	4	5	6			VBOP	VIN			
Common mode input voltage range H									7	-			VOF
Common mode input voltage range L									0.45	-			VOF
Input offset voltage									2.5	-			VOF
Input bias current	B		C						2.5	-			VBIN, VNFR
High level output voltage		B	C							0			OPOUT
Low level output voltage		B	C							8			OPOUT
Output sink current				B						-			(VCC-OPOUT)/50
Output source current				C						-			OPOUT/50
Slew rate										-	input pulse 100kHz, 2Vp-p		OPOUT
<Loading Driver> (MUTE=3V, BIAS=2.5V,VBOP=2.5V)	1	2	3	4	5	6	FWD	REV	ILF	ILR	VLDCTL		
Output saturation voltage 1					B		1.4	0.6	-200	200	3.3		VCC-VOLD
							0.6	1.4	200	-200	3.3		VCC-VOLD
Output saturation voltage 1 F/R												Voltage difference between VSAT1 FWD & REV	
Output saturation voltage 2							1.4	0.6	-500	500	3.3		VCC-VOLD
							0.6	1.4	500	-500	3.3		VCC-VOLD
Voltage gain											3.3		VOL/VCTL
<Loading logic input> (MUTE=3V, VBOP=2.5V)	1	2	3	4	5	6	FWD	REV					
Input high level voltage (1pin)							1.5	-				input parameter	
Input high level voltage (28pin)							-	1.5				input parameter	
Input low level voltage (1pin)							0.5	-				input parameter	
Input low level voltage (28pin)							-	0.5				input parameter	
Input high level current							5	-					AM1
							-	5					AM28

NOTES

1. Thermal-shut-down circuit built in.
When IC chip temperature rise to 175 (Typ.), output current is muted, and when IC chip temperature reaches 150 (Typ.), the driver circuit starts up.
2. When mute-terminal (pin.21) voltage is open or lowered below 0.5V, output current is muted.
Under normal use condition, pull up the mute terminal above 1.5V.
3. When bias-terminal (pin.20) voltage is below 0.5V, driver is muted.
Under normal use condition, set above 1.1V.
4. When supply voltage falls below 3.8V(Typ.), output current is muted.
Next time supply voltage rises to 4.0V(Typ.), the driver circuit start.
5. All drivers are muted by thermal-shut-down. When bias terminal voltage falls and mute is ON, BTL driver except loading driver is muted.
Previous stage operational amplifier is no case muted.
Output terminal of muted BTL driver applies internal bias voltage $(VCC-0.7)/2(V)$

6. Loading driver logic input

FWD (1pin)	REV (28pin)	VOL (+) (10pin)	VOL (-) (9pin)	FUNCTION
L	L	OPEN	OPEN	OPEN MODE
L	H	L	H	REVERSE MODE
H	L	H	L	FORWARD MODE
H	H	L	L	BRAKE MODE

Input circuit of pin1 and pin28 is designed to avoid simultaneous activation of upper and lower output Tr. however, in order to improve reliability, apply motor forward/backward input once through open mode.

We recommend time period for open mode longer than 10msec.

And, the voltage between the outputs can be controlled with the terminal LDCTL (pin.2).

The voltage is set 2.7 times (8.6dB Typ.) LDCTL(pin.2).

7. Insert the by-pass capacitor between Vcc-terminal and GND-terminal of IC as near as possible (approximately 0.1 μ F).
8. Heat dissipation fins are attached to the GND on the inside of the package.
Make sure to be connected to the external GND.
9. In priciple, do not apply voltage below sub-potential of IC to terminal.
Examine in consideration of operation margin, when each driver output falls below sub-voltage of IC (GND) due to counter-electromotive-force of load.
10. Please open the test termind (pin3,5,6).

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