HV9930

Hysteretic Boost-Buck (Ćuk) LED Driver IC

Features

- Constant Output Current LED Driver
- Steps Output Voltage Up or Down
- Low EMI
- Variable Frequency Operation
- Internal 8V to 200V Linear Regulator
- Input and Output Current Sensing
- Input Current Limit
- Enable and Pulse-Width Modulation (PWM) Dimming

Applications

- RGB Backlight Applications
- Battery-Powered LED Lamps
- Other Low-Voltage AC/DC or DC/DC LED Drivers

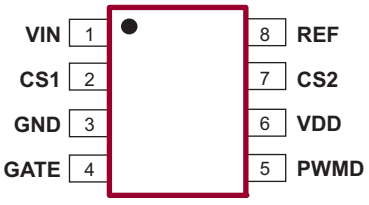
General Description

The HV9930 is a variable frequency PWM controller IC designed to control an LED lamp driver using a low-noise boost-buck (Ćuk) topology. The HV9930 uses a patented Hysteretic Current-mode control to regulate both the input and output currents. This enables superior input surge immunity without the necessity for complex loop compensation. Input current control enables current limiting during Startup, Input Undervoltage, and Output Overload conditions. The HV9930 provides a low-frequency PWM dimming input that can accept an external control signal with a duty cycle of 0% to 100% and a high dimming ratio.

The HV9930-based LED driver is ideal for LED lamps and RGB backlight applications with low-voltage DC inputs. The HV9930-based LED Lamp drivers can achieve efficiency in excess of 80%.

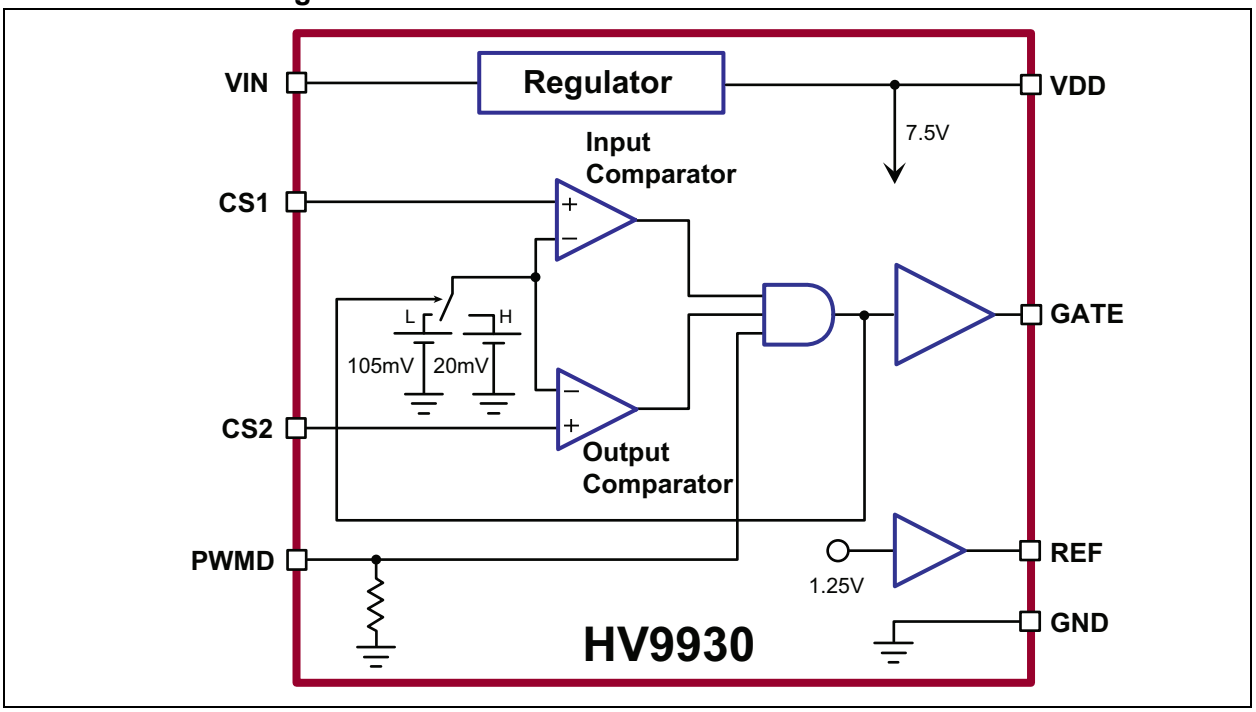
Package Type

8-lead SOIC
(Top view)

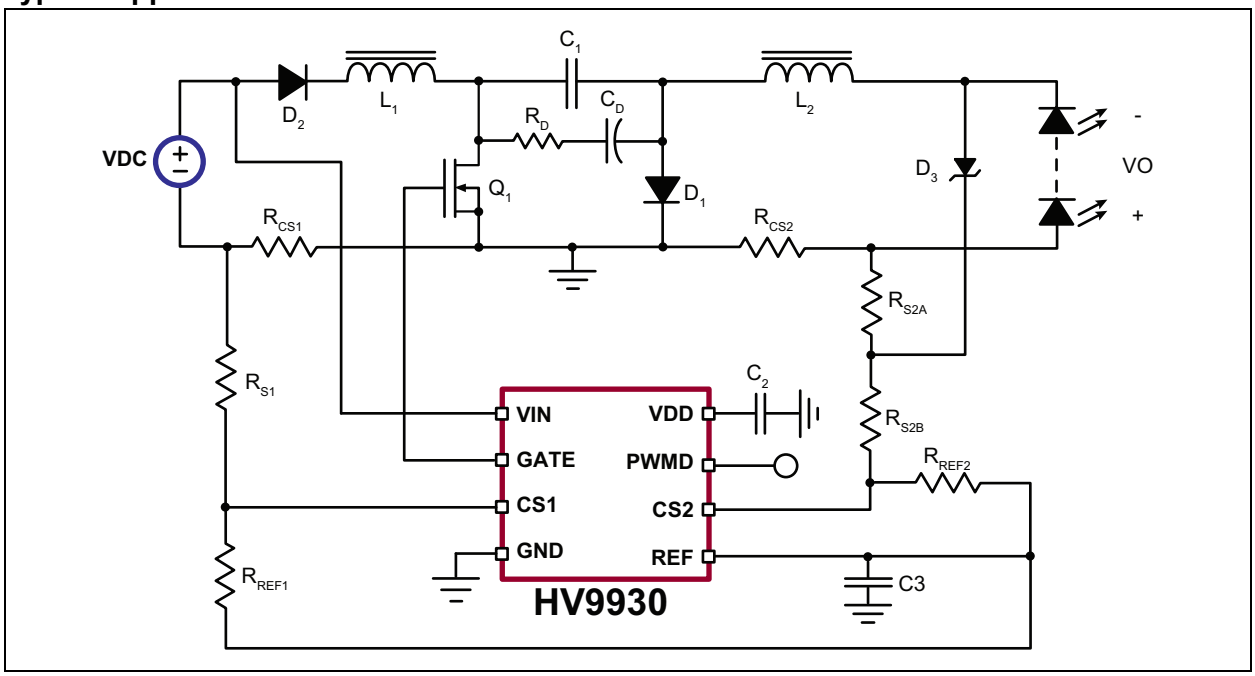


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{IN} to GND .....–0.5V to +200V
V_{DD} to GND.....–0.3V to +12V
CS1, CS2, PWMD, GATE, REF to GND .....–0.3V to (V_{DD} + 0.3V)
Junction Temperature, T_J ..... –40°C to +150°C
Storage Temperature, T_S ..... –65°C to +150°C
Continuous Power Dissipation (T_A = +25°C):
8-lead SOIC ..... 650 mW

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Specifications are at T_A = 25°C. V_{IN} = 12V unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
INPUT						
Input DC Supply Voltage Range	V_{INDC}	8	—	200	V	DC input voltage (**Note 1**)
Shutdown Mode Supply Current	I_{INSD}	—	0.5	1	mA	PWMD connected to GND (**Note 1**)
INTERNAL REGULATOR						
V_{DD} Internally Regulated Voltage	V_{DD}	7	7.5	9	V	V_{IN} = 8V to 200V, $I_{DD(EXT)}$ = 0 mA, GATE open
V_{DD} Current available for External Circuitry	$I_{DD(EXT)}$	—	—	1	mA	V_{IN} = 8V to 200V (**Note 2**)
V_{DD} Undervoltage Lockout Upper Threshold	$UVLO_R$	6.45	6.7	6.95	V	V_{DD} rising
V_{DD} Undervoltage Lockout Hysteresis	ΔUVLO	—	500	—	mV	
Steady State External Voltage which can be applied at the V_{DD} pin	$V_{DD(EXT)}$	—	—	12	V	
REFERENCE						
REF Pin Voltage	V_{REF}	1.212	1.25	1.288	V	REF bypassed with a 0.1 µF capacitor to GND, I_{REF} = 0 µA, V_{DD} = 7.5V, V_{PWMD} = 5V, V_{IN} = open (**Note 1**)
Line Regulation of Reference Voltage	$\Delta V_{REF,LN}$	0	—	20	mV	REF bypassed with a 0.1 µF capacitor to GND, I_{REF} = 0 µA, V_{DD} = 7V to 10V, V_{PWMD} = 5V, V_{IN} = open
Load Regulation of Reference Voltage	$\Delta V_{REF,LD}$	0	—	25	mV	REF bypassed with a 0.1 µF capacitor to GND, I_{REF} = 0 µA to 500 µA, V_{DD} = 7.5V, V_{PWMD} = 5V, V_{IN} = open
PWM DIMMING						
PWMD Input Low Voltage	$V_{PWMD(LO)}$	—	—	0.8	V	V_{IN} = 10V to 200V (**Note 1**)
PWMD Input High Voltage	$V_{PWMD(HI)}$	2	—	—	V	V_{IN} = 10V to 200V (**Note 1**)

Note 1: Specifications apply over the full operating ambient temperature range of –40ºC < T_A < +125ºC.
2: Also limited by package power dissipation limit, whichever is lower

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Specifications are at T_A = 25°C. V_{IN} = 12V unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
PWMD Pull-Down Resistance	R_{PWMD}	50	100	150	kΩ	V_{PWMD} = 5V
GATE DRIVER						
GATE Short Circuit Sourcing Current	I_{SOURCE}	0.165	—	—	A	V_{GATE} = 0V, V_{DD} = 7.5V, V_{IN} = open
GATE Sinking Current	I_{SINK}	0.165	—	—	A	V_{GATE} = V_{DD}, V_{DD} = 7.5V, V_{IN} = open
GATE Output Rise Time	t_{RISE}	—	30	50	ns	C_{GATE} = 500 pF, V_{DD} = 7.5V, V_{IN} = open
GATE Output Fall Time	t_{FALL}	—	30	50	ns	C_{GATE} = 500 pF, V_{DD} = 7.5V, V_{IN} = open
INPUT CURRENT SENSE COMPARATOR						
Voltage Threshold for GATE Turn-On	V_{ON1}	90	105	120	mV	V_{CS2} = 200 mV, V_{CS1} increasing, GATE goes LOW to HIGH (**Note 1**)
Voltage Threshold for GATE Turn-Off	V_{OFF1}	0	20	40	mV	V_{CS2} = 200 mV, V_{CS1} decreasing, GATE goes HIGH to LOW (**Note 1**)
Delay to Output (Turn-On)	$t_{D,ON1}$	—	80	150	ns	V_{CS2} = 200 mV, V_{CS1} = 50 mV to +200 mV step
Delay to Output (Turn-Off)	$t_{D,OFF1}$	—	80	150	ns	V_{CS2} = 200 mV, V_{CS1} = 50 mV to –100 mV step
OUTPUT CURRENT SENSE COMPARATOR						
Voltage Threshold for GATE Turn-On	V_{ON2}	90	105	120	mV	V_{CS1} = 200 mV, V_{CS2} increasing, GATE goes LOW to HIGH (**Note 1**)
Voltage Threshold for GATE Turn-Off	V_{OFF2}	0	20	40	mV	V_{CS1} = 200 mV, V_{CS2} decreasing, GATE goes HIGH to LOW (**Note 1**)
Delay to Output (Turn-On)	$t_{D,ON2}$	—	80	150	ns	V_{CS1} = 200 mV, V_{CS2} = 50 mV to +200 mV step
Delay to Output (Turn-Off)	$t_{D,OFF2}$	—	80	150	ns	V_{CS1} = 200 mV, V_{CS2} = 50 mV to –100 mV step

Note 1: Specifications apply over the full operating ambient temperature range of –40ºC < T_A < +125ºC.

2: Also limited by package power dissipation limit, whichever is lower

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	+125	°C	
Maximum Junction Temperature	$T_{J(ABSMAX)}$	—	—	+150	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
8-lead SOIC	θ_{JA}	—	+101	—	°C/W	

2.0 PIN DESCRIPTION

The details on the pins of HV9930 are listed in Table 2-1. Refer to **Package Type** for the location of the pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VIN	This pin is the input of an 8V to 200V voltage regulator.
2	CS1	This pin is used to sense the input current of the boost-buck converter. It is the non-inverting input of the internal input comparator.
3	GND	This is the ground return for all the internal circuitry. This pin must be electrically connected to the ground of the power train.
4	GATE	This pin is the gate driver output for an external N-channel power Metal-oxide Semiconductor Field-effect Transistor (MOSFET).
5	PWMD	When this pin is left open or pulled to GND, the gate driver is disabled. Pulling the pin to a voltage greater than 2V will enable the gate drive output.
6	VDD	This is a power supply pin for all internal circuits. It must be bypassed to GND with a low-ESR capacitor to GND.
7	CS2	This pin is used to sense the output current of the boost-buck converter. It is the non-inverting input of the internal output comparator.
8	REF	This pin provides accurate reference voltage. It must be bypassed with a 0.01 µF to 0.1 µF capacitor to GND.

3.0 DETAILED DESCRIPTION

3.1 Power Topology

The HV9930 is optimized to drive a Continuous Conduction Mode (CCM) boost-buck DC/DC converter topology commonly referred to as Ćuk converter. (See **Typical Application Circuit**.) This power converter topology offers numerous advantages useful for driving high-brightness light-emitting diodes (HB LED). These advantages include step-up or step-down voltage conversion ratio and low input and output current ripple. The input and output inductors can also share a common core to achieve ripple current cancellation. The output load is decoupled from the input voltage with a capacitor, making the driver inherently failure-safe for the output load.

The HV9930 offers a simple and effective control technique for a boost-buck LED driver. It uses two Hysteretic mode controllers—one for the input and one for the output. The outputs of these two hysteretic comparators are logically being AND together and are used to drive the external FET. This control scheme gives accurate current control and constant output current in the presence of input voltage transients without the need for complicated loop design.

3.2 Input Voltage Regulator

The HV9930 can be powered directly from its V_{IN} pin that takes voltage from 8V up to the maximum of 200V. When voltage is applied to the V_{IN} pin, the HV9930 attempts to regulate a constant 7.5V (typical) at the V_{DD} pin. The regulator also has a built-in undervoltage lockout which shuts off the IC when the voltage at the V_{DD} pin falls below the UVLO lower threshold.

The V_{DD} pin must be bypassed by a low-ESR capacitor (≥0.1 µF) to provide a low-impedance path for the high-frequency current of the output gate driver.

The IC can also be operated by supplying a voltage at the V_{DD} pin greater than the internally regulated voltage. This will turn off the internal linear regulator and the IC will function by drawing power from the external voltage source connected to the V_{DD} pin.

In case of input transients that reduce the input voltage below 8V (e.g. Cold Crank condition in an automotive system), the V_{IN} pin of the HV9930 can be connected to the external MOSFET drain through a diode. Since the drain of the FET is at a voltage equal to the sum of the input and output voltages, the IC will still be operational when the input goes below 8V. In these cases, a larger capacitor is needed for the V_{DD} pin to supply power to the IC when the MOSFET switches on.

3.3 Reference

An internally trimmed voltage reference of 1.25V (± 3%) is provided at the REF pin. The reference can supply a maximum output current of 1 mA to drive external circuitry. This reference can be used to set the current-sense voltage thresholds of the two comparators as shown in the **Typical Application Circuit**.

3.4 Current Comparators

The HV9930 features two identical comparators with a built-in 85 mV hysteresis. When the GATE is low, the inverting terminal is connected to 105 mV, but when the GATE is high, it is connected to 20 mV. One comparator is used for the input current control and the other is used for the output current control.

The input side hysteretic controller is in operation only during Start-up and Overload conditions. This ensures that the input current never exceeds the designed value. During normal operation, the input current will be less than the programmed current. Therefore, the output of the input side comparator will be high. The output of the AND gate will then be dictated by the output current controller.

The output side hysteretic comparator will be in operation during the Steady state operation of the circuit. This comparator turns the MOSFET on and off based on the LED current.

The use of these comparators in a boost-buck topology is a patented technique, which eliminates the need for compensation components.

3.5 PWM Dimming

PWM dimming can be achieved by applying a PWM signal to the PWMD pin. When the PWMD pin is pulled high, the gate driver is enabled and the circuit operates normally. When the PWMD pin is left open or connected to GND, the gate driver is disabled and the external MOSFET turns off. The signal at the PWMD pin inhibits the driver only and the IC need not go through the entire start-up cycle each time, ensuring a quick response time for the output current.

The flying capacitor in the Ćuk converter (C1) is initially charged to the input voltage V_{DC} (through diodes D_1 and D_2). When the circuit is turned on and reaches Steady state, the voltage across C1 will be $V_{DC}+V_O$. In the absence of diode D_2, when the circuit is turned off, capacitor C_1 will discharge through the LEDs and the input voltage source V_{DC}. Thus, during PWM dimming, if capacitor C_1 has to be charged and discharged each cycle, the transient response of the circuit will be limited. By adding diode D_2, the voltage across capacitor C_1 is held at $V_{DC}+V_O$ even when the circuit is turned off, enabling the circuit to return quickly to its Steady state (and bypassing the start-up stage) upon being enabled.

4.0 APPLICATION INFORMATION

4.1 Overvoltage Protection

Overvoltage protection can be added by splitting the output side resistor R_{S2} into two components (R_{S2A} and R_{S2B}) and adding a Zener diode D_3. When there is an Open LED condition, the diode D_3 will clamp the output voltage, and the Zener diode current will be sensed by the sum of R_{S2A} and R_{CS2}. The current will also be regulated by the converter.

4.2 Damping Circuit

The Ćuk converter is inherently unstable when the output current is being controlled. An uncontrolled input current will lead to an undamped oscillation between L_1 and C_1, causing excessively high voltages across capacitor C_1. To prevent these oscillations, a damping circuit consisting of R_D and C_D is applied across the capacitor C_1. This damping circuit will stabilize the circuit and help maintain the proper operation of the converter.

The values of the damping network can be computed with Equation 4-1 and Equation 4-2.

EQUATION 4-1:

$$C_D = 9 \times \left(\frac{D_{MAX}}{1 - D_{MAX}}\right)^3 \times L_1 \times \left(\frac{I_O}{V_O}\right)^2$$

Where D_{MAX} is the maximum switching duty cycle, L_1 is the inductance of the input inductor, I_O is the output LED current, and V_O is the voltage across the output LED string.

EQUATION 4-2:

$$R_D = \frac{3 \times D_{MAX}}{(1 - D_{MAX})^2} \times \frac{L_1 \times I_O}{C_D \times V_O}$$

The maximum switching duty cycle is calculated with Equation 4-3.

EQUATION 4-3:

$$D_{MAX} = \frac{V_O}{V_O + \eta_{MIN} \times (V_{IN,MIN} - V_D)}$$

Where η_{MIN} is the minimum efficiency, and $V_{IN,MIN}$ is the minimum input voltage.V_D is the input diode forward voltage.

RMS current of the damping capacitor is determined with Equation 4-4.

EQUATION 4-4:

$$I_{CD(RMS)} = \frac{\Delta V_{C1}}{\sqrt{12} \times R_D}$$

Where ΔV_{C1} is the peak-to-peak ripple voltage of the flying capacitor C_1 and it is 10% of the average voltage across C_1.

The power dissipation in R_D is calculated with Equation 4-5.

EQUATION 4-5:

$$P_{RD} = \frac{(\Delta V_{C1})^2}{12 \times R_D}$$

4.3 Output Current Level and Input Current Limit

The current sense resistor R_{CS2}, combined with the other resistors R_{S2} and R_{REF2}, determines the output current level at undimmed full brightness. On the other hand, the current sense resistor R_{CS1}, combined with the other resistors R_{S1} and R_{REF1}, determines the input average current limit.

Each set of resistors for the output side or the input side can be chosen using Equation 4-6 and Equation 4-7.

EQUATION 4-6:

$$I \times R_{CS} = \left[V_{REF} - \frac{(V_{ON} + V_{OFF})}{2}\right] \times \left(\frac{R_S}{R_{REF}}\right) - \left(\frac{V_{ON} + V_{OFF}}{2}\right)$$

Where I is the average current (either I_O or I_{IN}), V_{REF} (1.25V typical) is the reference voltage, V_{ON} (0.105V typical) is the threshold voltage for the GATE On, and V_{OFF} (0.02V typical) is the threshold voltage for the GATE Off.

EQUATION 4-7:

$$\Delta I \times R_{CS} = (V_{ON} - V_{OFF}) \times \left(\frac{R_S}{R_{REF}}\right) + (V_{ON} - V_{OFF})$$

Where ΔI is the peak-to-peak ripple in the current (either ΔI_O or ΔI_{IN}).

By solving the Equation 4-6 and Equation 4-7, the value of R_S/R_{REF} can be obtained from Equation 4-8.

EQUATION 4-8:

$$\frac{R_S}{R_{REF}} = \frac{\frac{\Delta I}{I} \times \frac{(V_{ON} + V_{OFF})}{2} + (V_{ON} - V_{OFF})}{\frac{\Delta I}{I} \times \left[V_{REF} - \frac{(V_{ON} + V_{OFF})}{2}\right] - (V_{ON} - V_{OFF})}$$

The value of R_{REF} can be set as 10 kΩ for convenience. Then, the value of R_S can be chosen from the calculated value of R_S/R_{REF}. The value of R_{CS} is then computed from Equation 4-9.

EQUATION 4-9:

$$R_{CS} = \frac{\left[V_{REF} - \frac{(V_{ON} + V_{OFF})}{2}\right] \times \frac{R_S}{R_{REF}} - \frac{(V_{ON} + V_{OFF})}{2}}{I}$$

4.4 Design and Operation of the Boost-buck Converter

For details on the design for a boost-buck converter using the HV9930 and the calculation of the damping components, refer to application notes *AN-H51* Designing a Boost-Buck (Ĉuk) Converter with the HV9930/AT9933 and *AN-H58 Improving the Efficiency of a HV9930/AT9933 Controlled Boost-Buck Converter.*

4.5 Design Example

The choice of the resistor dividers to set the input and output current levels is illustrated by means of the design example given below.

The parameters of the power circuit are:

$$V_{IN,MIN} = 9V$$
$$V_{IN,MAX} = 16V$$
$$V_O = 28V$$
$$I_O = 0.35A$$
$$f_{S,MIN} = 300kHz$$

Using these parameters, the values of the power stage inductors and capacitor can be computed. (See figures below.) Refer to Application Note *AN-H51* for more details.

$$L_1 = 82\mu H$$
$$L_2 = 150\mu H$$
$$C_1 = 0.22\mu F$$

The input and output currents for this design are:

$$I_{IN,MAX} = 1.6A$$
$$\Delta I_{IN} = 0.21A$$
$$I_O = 350mA$$
$$\Delta I_O = 87.5mA$$

For the input side, the average current limit level used in the equations should be larger than the operating maximum average input current, so it does not interfere with the normal operation of the circuit. The peak input current can be computed as shown in Equation 4-10.

EQUATION 4-10:

$$I_{IN,PK} = I_{IN,MAX} + \left(\frac{\Delta I_{IN}}{2}\right)$$
$$= 1.705A$$

Assuming a 30% peak-to-peak input current ripple to average input current ratio when the converter is in Input Current Limit mode, the minimum value of the input current in the Input Current Limit mode is calculated as shown in Equation 4-11.

EQUATION 4-11:

Setting

$$I_{LIN,MIN} = 0.85 \times I_{IN,LIM}$$
$$I_{LIN,MIN} = 1.05 \times I_{IN,PK}$$

The average input current limit of the converter can then be computed. See Equation 4-12.

EQUATION 4-12:

$$I_{IN,LIM} = \left(\frac{1.05}{0.85}\right) \times I_{IN,PK}$$
$$= 2.1A$$

Using I_O = 0.35A and $\Delta I_O = 0.25 \times I_O$ = 0.0875A for the output side in Equation 4-8 and Equation 4-9, R_{S2}/R_{REF2} = 0.475 and R_{CS2} = 1.43Ω are obtained.

Before the design of the output side is complete, overvoltage protection has to be included in the design. For this application, choose a 33V Zener diode. This is the voltage at which the output will clamp in case of an Open LED condition. For a 350 mW diode, the maximum current rating at 33V works out to about 10 mA. Using a 2.5 mA current level during Open LED conditions, and assuming the same R_{S2}/R_{REF2} ratio, and splitting R_{S2} into R_{S2A} and R_{S2B}, the Zener current limiting resistor can be determined as illustrated in Equation 4-13.

EQUATION 4-13:

$$R_{CS2,Z} = R_{CS2} + R_{S2A} = 120\Omega$$

Choose the following values for the resistors on the output side:

$$R_{CS2} = 1.43\Omega,\ 1/4W,\ 1\%$$
$$R_{REF2} = 10\ k\Omega,\ 1/8W,\ 1\%$$
$$R_{S2A} = 110\Omega,\ 1/8W,\ 1\%$$
$$R_{S2B} = 4.64\ k\Omega,\ 1/8W,\ 1\%$$

The current sense resistor needs to be at least a 1/4W, 1% resistor. Similarly, using $I_{IN,LIM}$ = 2.1A and $\Delta I_{IN,LIM}$ = 0.3 x $I_{IN,LIM}$ = 0.63A for the input side in Equation 4-8 and Equation 4-9, the following values can be determined:

$$\frac{R_{S1}}{R_{REF1}} = 0.382$$
$$R_{CS1} = 0.187\Omega$$
$$P_{RCS1} = I^2_{IN,LIM} \times R_{CS1}$$
$$= 0.825W$$

Choose the following values for the resistors on the input side:

R_{CS1} = *parallel combination of three 0.56Ω, 1/2W, 5% resistors*

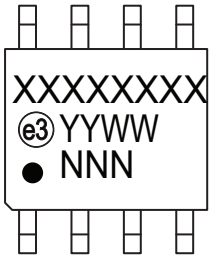
$R_{REF1} = 10k\Omega,\ 1/8W,\ 1\%$

$R_{S1} = 3.82k\Omega,\ 1/8W,\ 1\%$

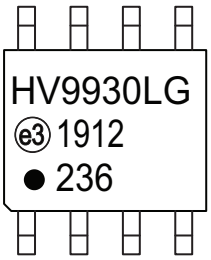
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

8-lead SOIC



Example

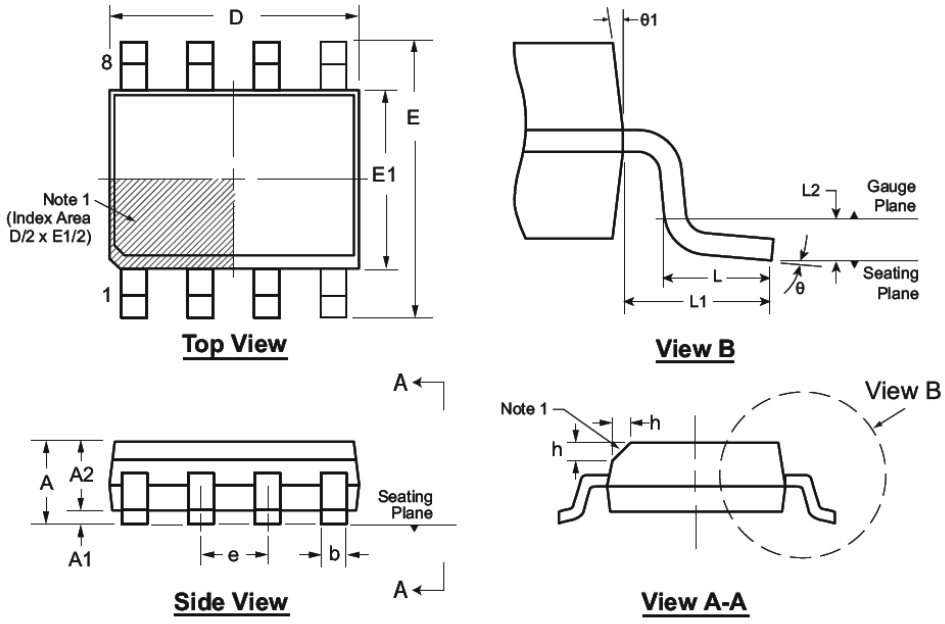


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

** This dimension is not specified in the JEDEC drawing.*

Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (November 2019)

- Converted Supertex Doc# DSFP-HV9930 to Microchip DS20005682A
- Changed the quantity of the 8-lead SOIC LG package from 2500/Reel to 3300/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV9930	=	Hysteretic Boost-Buck (Ćuk) LED Driver IC
Package:	LG	=	8-lead SOIC
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	3300/Reel for an LG Package

Example:

a) HV9930LG-G: Hysteretic Boost-Buck (Ćuk) LED Driver IC, 8-lead SOIC Package, 3300/Reel

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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