Introduction

This document provides the instructions to help programming vendors qualify SST's FlashFlex51 microcontrollers.

Functional Blocks
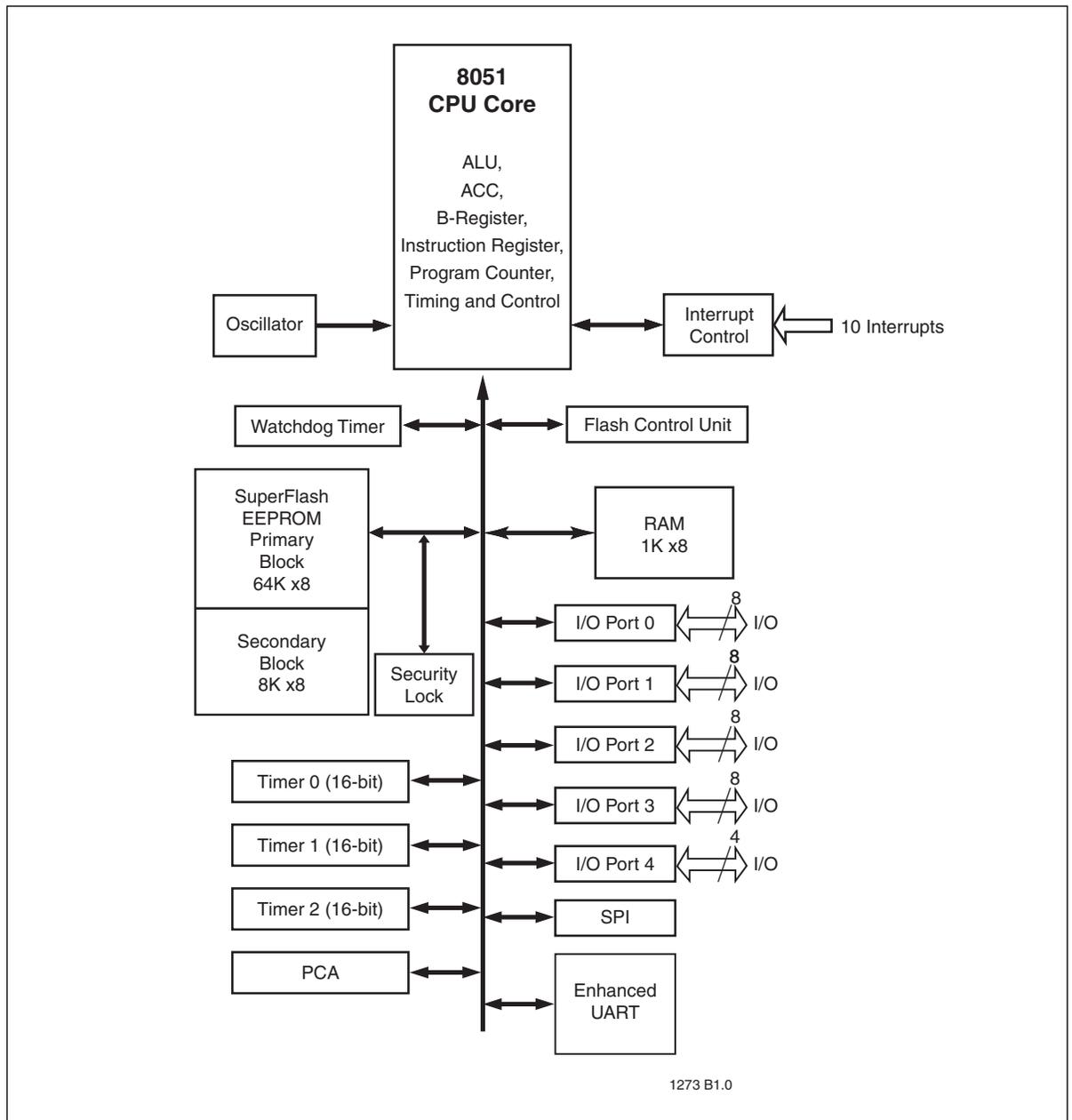
Figure 1: Functional Block Diagram

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Flash Memory Programming

The device internal flash memory can be programmed or erased using the External Host Programming mode.

External Host Programming Mode

External host programming mode allows the user to program the flash memory directly without using the CPU. External host mode is entered by forcing PSEN# from a logic high to a logic low while RST input is being held continuously high. The device will stay in external host mode as long as RST = 1 and PSEN# = 0.

A Read-ID operation is necessary to "arm" the device in external host mode, and no other external host mode commands can be enabled until a Read-ID is performed. In external host mode, the internal flash memory blocks are accessed through the re-assigned I/O port pins (see Figure 2 for details) by an external host, such as a MCU programmer, a PCB tester, or a PC-controlled development board.

Table 1: External Host Mode Commands[1]

Operation	RST	PSEN#	PROG#/ ALE	EA#	P3[7]	P3[6]	P2[7]	P2[6]	P0[7:0]	P3[5:4] P2[5:0]	P1[7:0]
Read-ID	V_{IH1}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	DO	AH	AL
Chip-Erase	V_{IH1}	V_{IL}	$\Downarrow$[2]	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	X
Block-Erase	V_{IH1}	V_{IL}	$\Downarrow$	V_{IH}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	X	X	X
Sector-Erase	V_{IH1}	V_{IL}	$\Downarrow$	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	AH	AL
Byte-Program	V_{IH1}	V_{IL}	$\Downarrow$	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	DI	AH	AL
Byte-Verify (Read)	V_{IH1}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	DO	AH	AL
Select-Block0	V_{IH1}	V_{IL}	$\Downarrow$	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	55H	X
Select-Block1	V_{IH1}	V_{IL}	$\Downarrow$	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	A5H	X
Prog-SC0	V_{IH1}	V_{IL}	$\Downarrow$	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	5AH	X
Prog-SB1	V_{IH1}	V_{IL}	$\Downarrow$	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	X
Prog-SB2	V_{IH1}	V_{IL}	$\Downarrow$	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	X
Prog-SB3	V_{IH1}	V_{IL}	$\Downarrow$	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	X
Enable-Clock-Double	V_{IH1}	V_{IL}	$\Downarrow$	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	X	55H	X

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1. External Host programming mode is guaranteed at 25°C (room temperature) only
2. Symbol $\Downarrow$ signifies a negative pulse and the command is asserted during the low state of PROG#/ALE input. All other combinations of the above input pins are invalid and may result in unexpected behaviors.

Note: V_{IL} = Input Low Voltage; V_{IH} = Input High Voltage; V_{IH1} = Input High Voltage (XTAL, RST); X = Don't care; AL = Address low order byte; AH = Address high order byte; DI = Data Input; DO = Data Output.

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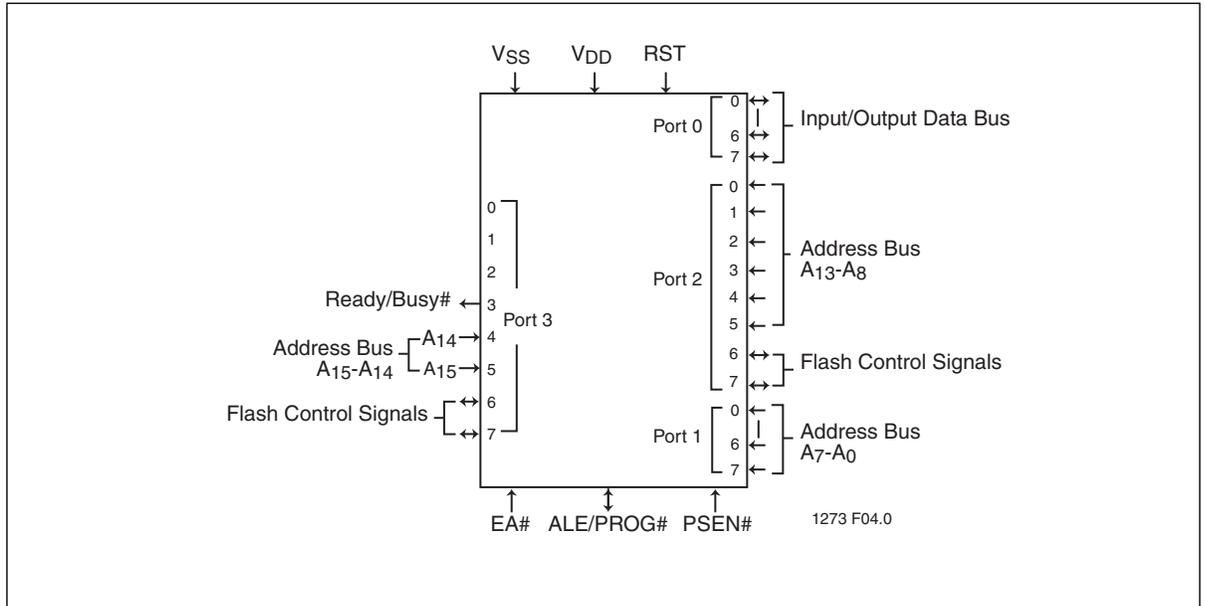
Figure 2: I/O Pin Assignments for External Host Mode

Product Identification

The Read-ID command accesses the signature bytes that identify the device and the manufacturer as SST. External programmers primarily use these signature bytes in the selection of programming algorithms. The Read-ID command is selected by the command code of 0H on P3[7:6] and P2[7:6]. See Figure 3 for timing waveforms.

Table 2: Product Identification

	Address	Data
Manufacturer's ID	30H	BFH
Device ID		
SST89E516RD2/RD	31H	93H
	61H, Bit 7	0
SST89V516RD2/RD	31H	92H
	61H, Bit 7	0

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Arming Command

An arming command sequence must take place before any external host mode sequence command is recognized by the device. This prevents accidental triggering of external host mode commands due to noise or programmer error. The arming command is as follows:

1. PSEN# goes low while RST is high. This will get the machine in external host mode, re-configuring the pins, and turning on the on-chip oscillator.

2. A Read-ID command is issued, and after 1 ms the external host mode commands can be issued.

After the above sequence, all other external host mode commands are enabled. Before the Read-ID command is received, all other external host mode commands received are ignored.

External Host Mode Commands

The external host mode commands are Read-ID, Chip-Erase, Block-Erase, Sector-Erase, Byte-Program, Byte-Verify, Prog-SB1, Prog-SB2, Prog-SB3, Prog-SC0, Select-Block0, Select-Block1. See Table 1 for all signal logic assignments, Figure 2 for I/O pin assignments, and Table 4 for the timing parameters. The critical timing for all Erase and Program commands is generated by an on-chip flash memory controller. The high-to-low transition of the PROG# signal initiates the Erase or Program commands, which are synchronized internally. The Read commands are asynchronous reads, independent of the PROG# signal level.

A detailed description of the external host mode commands follows.

The Select-Block0 command enables Block 0 to be programmed in external host mode. Once this command is executed, all subsequent external host Commands will be directed at Block 0. See Figure 4 for timing waveforms.

The Select-Block1 command enables Block 1 (8 KByte Block) to be programmed. Once this command is executed, all subsequent external host Commands that are directed to the address range below 2000H will be directed at Block 1. The Select-Block1 command only affects the lowest 8 KByte of the program address space. For addresses greater than or equal to 2000H, Block 0 is accessed by default. Upon entering external host mode, Block 1 is selected by default. See Figure 4 for timing waveforms.

The Chip-Erase, Block-Erase, and Sector-Erase commands are used for erasing all or part of the memory array. Erased data bytes in the memory array will be erased to FFH. Memory locations that are to be programmed must be in the erased state prior to programming.

The Chip-Erase command erases all bytes in both memory blocks, regardless of any previous Select-Block0 or Select-Block1 commands. Chip-Erase ignores the Security Lock status and will erase the Security Lock, returning the device to its Unlocked state. The Chip-Erase command will also erase the SC0 bit. Upon completion of Chip-Erase command, Block 1 will be the selected block. See Figure 5 for timing waveforms.

The Block-Erase command erases all bytes in the selected memory blocks. This command will not be executed if the security lock is enabled. The selection of the memory block to be erased is determined by the prior execution Select-Block0 or Select-Block1 command. See Figure 6 for the timing waveforms.

The Sector-Erase command erases all of the bytes in a sector. The sector size for the flash memory is 128 Bytes. This command will not be executed if the Security lock is enabled. See Figure 7 for timing waveforms.

The Byte-Program command is used for programming new data into the memory array. Programming will not take place if any security locks are enabled. See Figure 8 for timing waveforms.

The Byte-Verify command allows the user to verify that the device correctly performed an Erase or Program command. This command will be disabled if any security locks are enabled. See Figure 11 for timing waveforms.

The Prog-SB1, Prog-SB2, Prog-SB3 commands program the security bits, the functions of these bits are described in the Security Lock section and also in Table 9-1. Once programmed, these bits can only be erased through a Chip-Erase command. See Figure 9 for timing waveforms.

Prog-SC0 command programs SC0 bit, which determines the state of SFCF[0] out of reset. Once programmed, SC0 can only be restored to an erased state via a Chip-Erase command. See Figure 10 for timing waveforms.

External Host Mode Clock Source

In external host mode, an internal oscillator will provide clocking for the device, and the oscillator is unaffected by the clock doubler logic. The on-chip oscillator will be turned on as the device enters external host mode; i.e. when PSEN# goes low while RST is high. During external host mode, the CPU core is held in reset. Upon exit from external host mode, the internal oscillator is turned off.

Flash Operation Status Detection Via External Host Handshake

The device provides two methods for an external host to detect the completion of a flash memory operation to optimize the Program or Erase time. The end of a flash memory operation cycle can be detected by:

1. monitoring the Ready/Busy# bit at P3[3];

2. monitoring the Data# Polling bit at P0[3].

Ready/Busy# (P3[3])

The progress of the flash memory programming can be monitored by the Ready/Busy# output signal. P3[3] is driven low, some time after ALE/PROG# goes low during a flash memory operation to indicate the Busy# status of the Flash Control Unit (FCU). P3[3] is driven high when the flash programming operation is completed to indicate the ready status.

Data# Polling (P0[3])

During a Program operation, any attempts to read (Byte-Verify), while the device is busy, will receive the complement of the data of the last byte loaded (logic low, i.e. "0" for an Erase) on P0[3] with the rest of the bits "0". During a Program operation, the Byte-Verify command is reading the data of the last byte loaded, not the data at the address specified.

Instructions to Perform External Host Mode Commands

To program data into the memory array, apply power supply voltage (V_{DD}) to V_{DD} and RST pins, and perform the following steps:

1. Maintain RST high and set PSEN# from logic high to low, in sequence according to the appropriate timing diagram.

2. Raise EA# High (V_{IH}).

3. Issue Read-ID command to enable the external host mode.

4. Verify that the memory blocks or sectors for programming is in the erased state, FFH. If they are not erased, then erase them using the appropriate Erase command.

5. Select the memory location using the address lines (P3[5:4], P2[5:0], P1[7:0]).

6. Present the data in on P0[7:0].

7. Pulse ALE/PROG#, observing minimum pulse width.

8. Wait for low to high transition on Ready/Busy# (P3[3]).

9. Repeat steps 5 - 8 until programming is finished.

10. Verify the flash memory contents.

Additional Read Commands in External Host Mode

The procedure to issue additional read commands, shown in Table 3 below, is the same as the read ID command format, only the address is changed. Here is a short list of useful features:

- Read the status of the security bits (SB1_i, SB2_i, SB3_i).
- Read the configuration bits (SC0_i) status.
- Read the clock mode (EDC_i) status.

Note: Commands shown in Table 3 are not the ARMING type.

Table 3: Additional Read Commands in External Host Mode

Address	Data							
60H	X	X	X	X	SC0_i	SB1_i	SB2_i	SB3_i
61H	X	X	X	X	X	X	EDC_i	X

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Note: X = Don't care

Table 4: External Mode Flash Memory Programming/Verification Parameters[1]

Parameter[2,3]	Symbol	Min	Max	Units
Reset Setup Time	T_{SU}	3		µs
Read-ID Command Width	T_{RD}	1		µs
PSEN# Setup Time	T_{ES}	40		µs
Address, Command, Data Setup Time	T_{ADS}	0		ns
Chip-Erase Time	T_{CE}		150	ms
Block-Erase Time	T_{BE}		100	ms
Sector-Erase Time	T_{SE}		30	ms
Program Setup Time	T_{PROG}	1.2		µs
Address, Command, Data Hold	T_{DH}	0		ns
Byte-Program Time[4]	T_{PB}		50	µs
Select-Block Program Time	T_{PSB}		500	ns
Re-map or Security bit Program Time	T_{PS}		80	µs
Verify Command Delay Time	T_{OA}		50	ns
Verify High Order Address Delay Time	T_{AHA}		50	ns
Verify Low Order Address Delay Time	T_{ALA}		50	ns

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1. For IAP operations, the program execution overhead must be added to the above timing parameters.
2. Program and Erase times will scale inversely proportional to programming clock frequency.
3. All timing measurements are from the 50% of the input to 50% of the output.
4. Each byte must be erased before programming.

Flash Memory Programming Timing Diagrams with External Host Mode
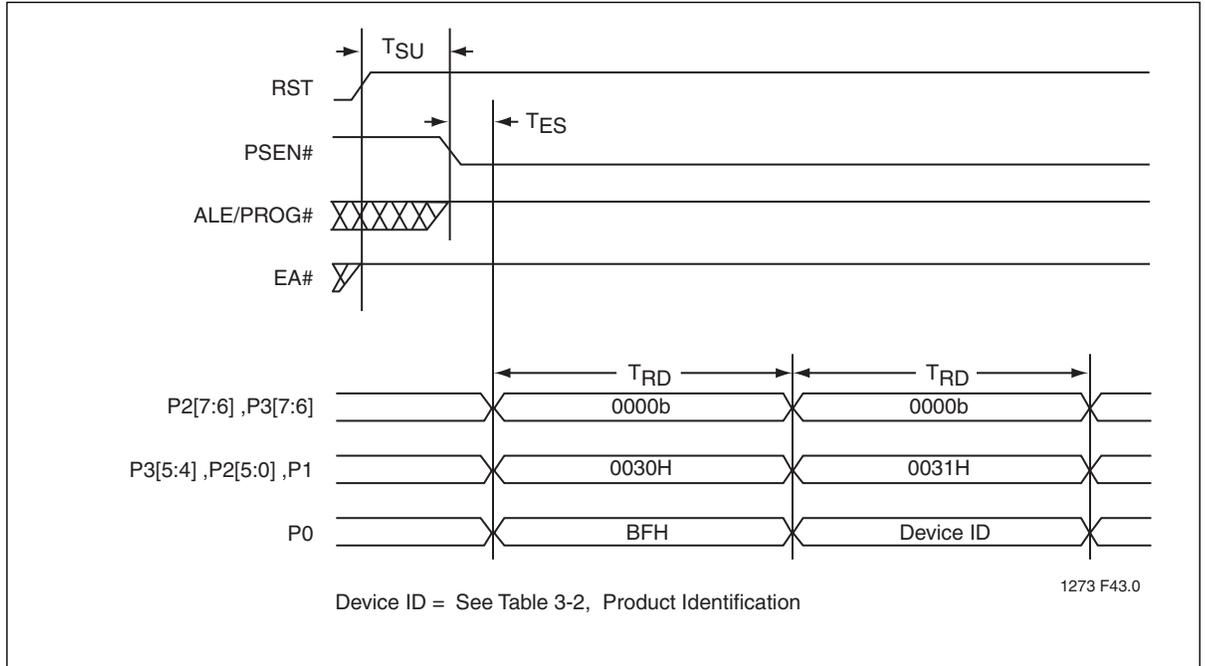
Figure 3: Read-ID

Reads chip signature and identification registers at the addressed location.
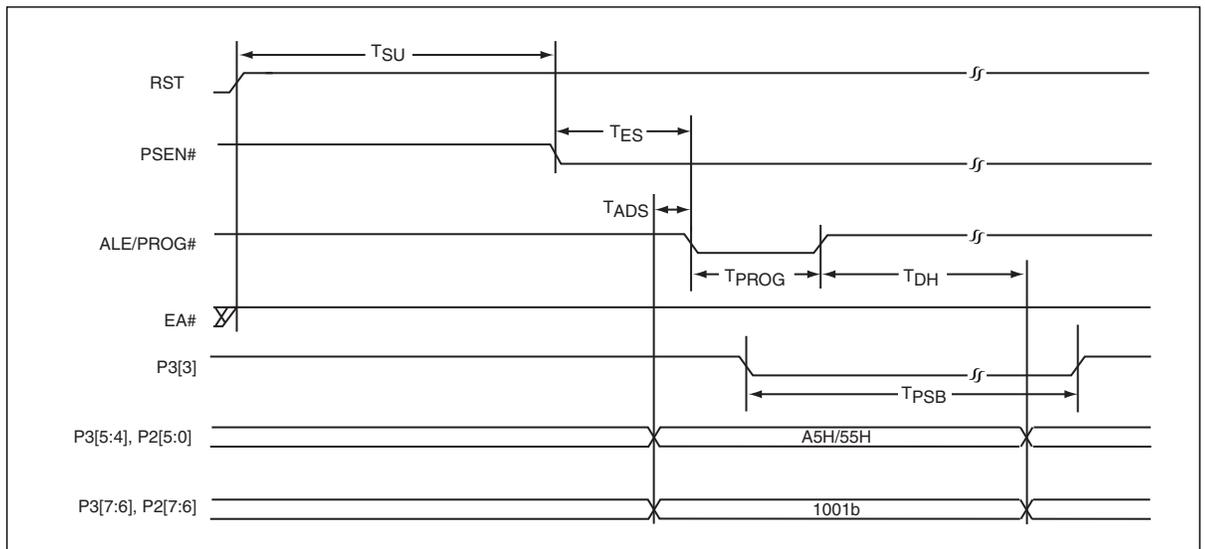
Figure 4: Select-Block1 / Select-Block0

Enables the selection of either of the flash memory blocks prior to issuing a Byte-Verify, Block-Erase, Sector-Erase, or Byte-Program.
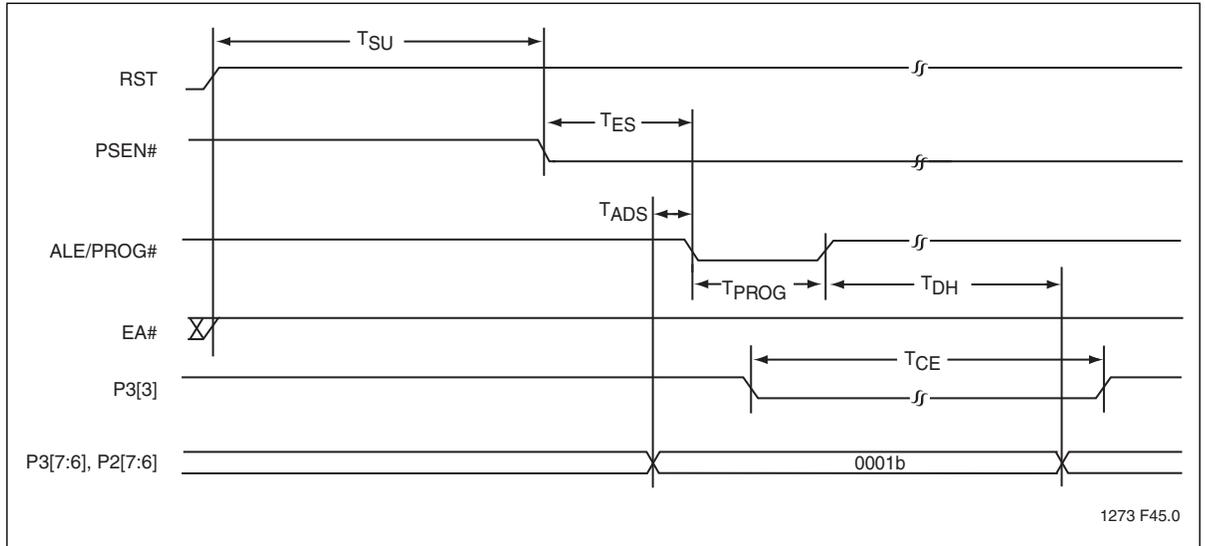
Figure 5: Chip-Erase

Erases both flash memory blocks. Security lock is ignored and the security bits are erased too.
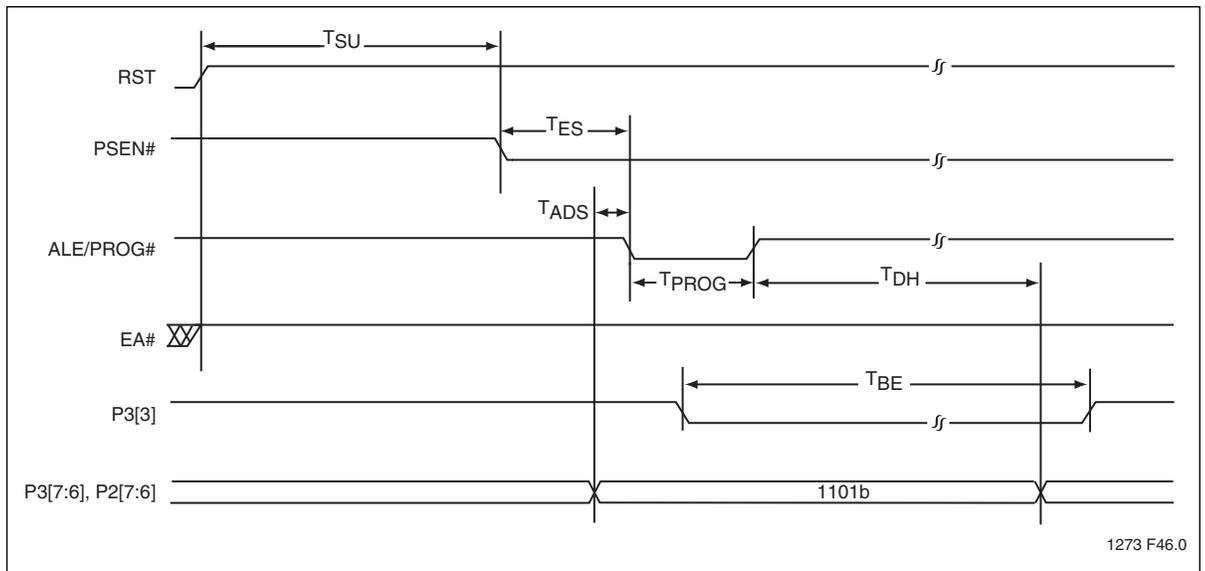
Figure 6: Block-Erase

Erases one of the flash memory blocks, if the security lock is not activated on that flash memory block.
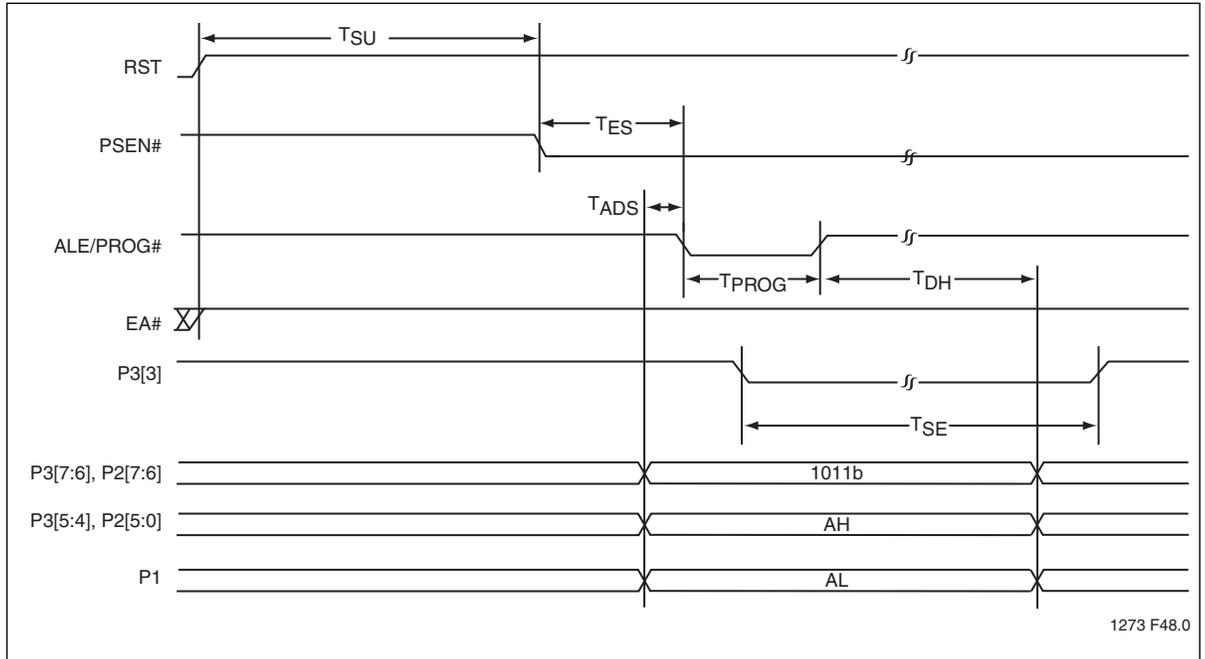
Figure 7: Sector-Erase

Erases the addressed sector if the security lock is not activated on that flash memory block.
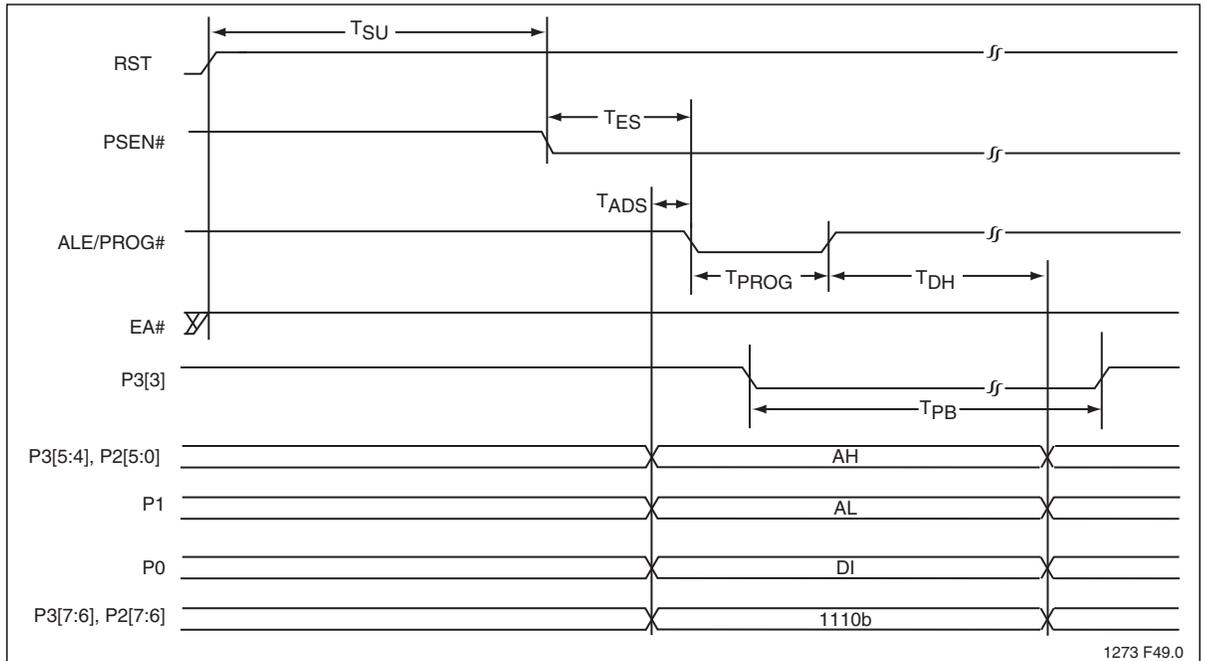
Figure 8: Byte-Program

Programs the addressed code byte if the byte location has been successfully erased and not yet programmed. Byte-Program operation is only allowed when the security lock is not activated on that flash memory block.
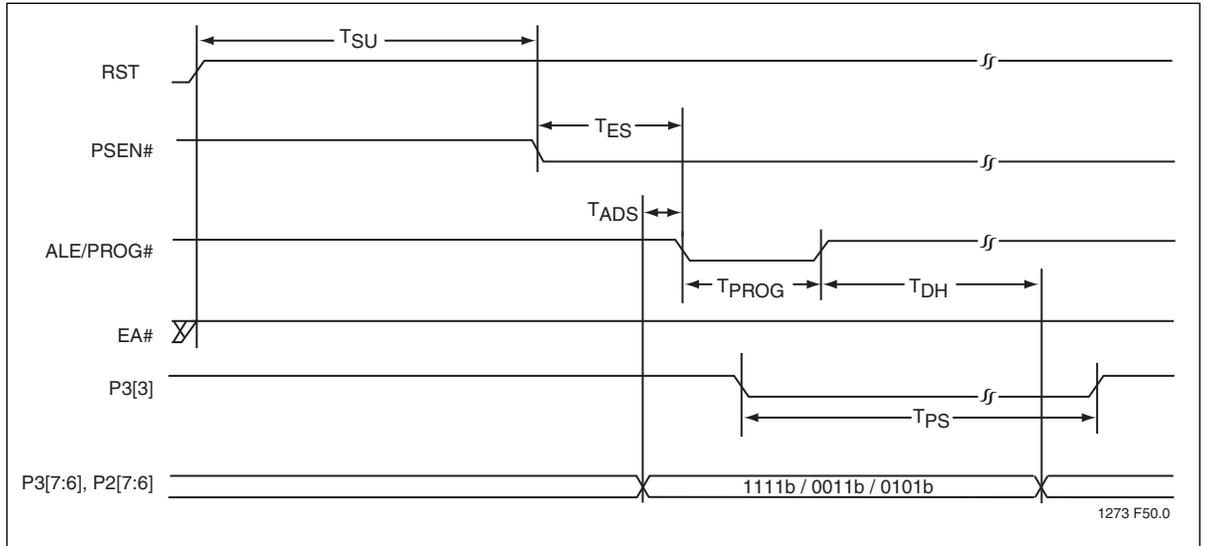
Figure 9: Prog-SB1 / Prog-SB2 / Prog-SB3

Programs the Security bits SB1, SB2 and SB3 respectively. Only a Chip-Erase will erase a programmed security bit.
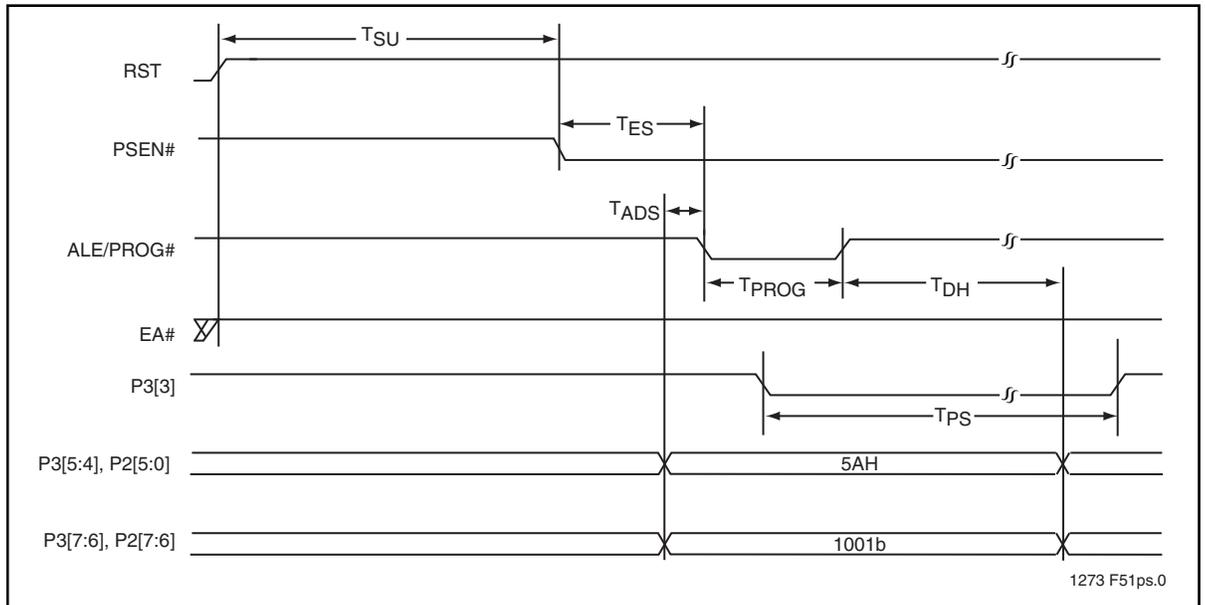
Figure 10: Prog-SC0

Programs the start-up configuration bit SC0. Only a Chip-Erase will erase a programmed SC0 bit.
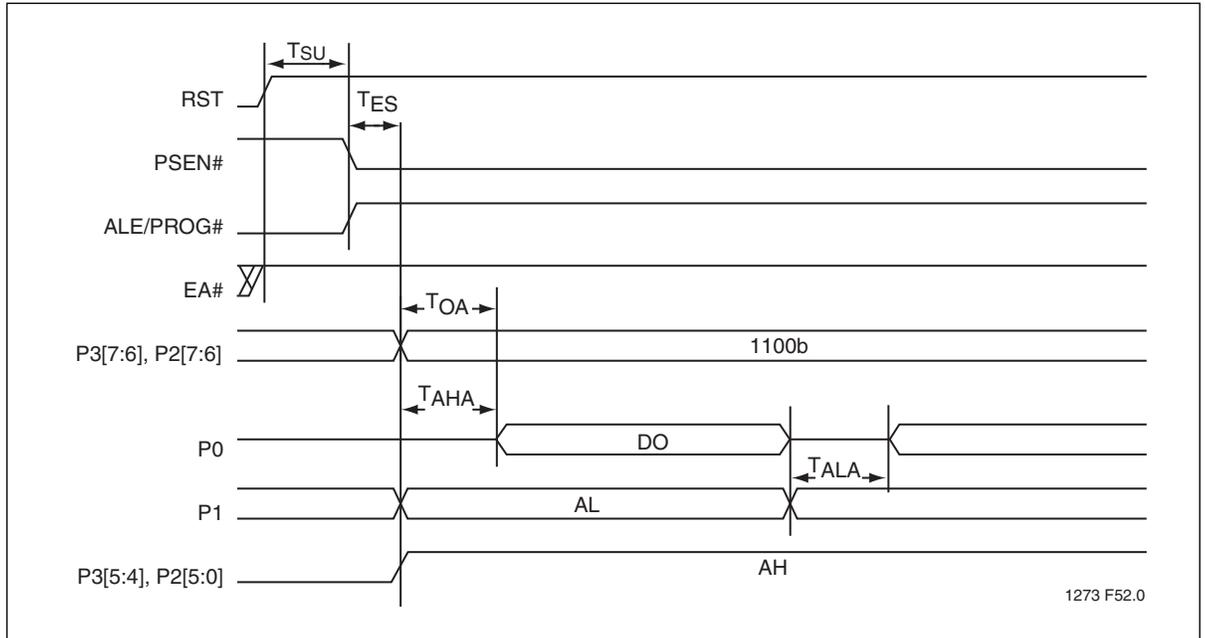
Figure 11: Byte-Verify

Reads the code byte from the addressed flash memory location if the security lock is not activated on that flash memory block.

Table 5: Revision History

Revision	Description	Date
A	• Applied new document format • Released document under the letter revision system • Updated spec number from S71273(02) to DS25094	Nov 2011

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A Microchip Technology Company
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