



System LSI for Event Data Recorder BU1511KV2

●Outline

BU1511KV2 is a system LSI for Event Data Recorder(EDR) which can record/play Audio/Video event data, and can make developing the EDR easier at low cost

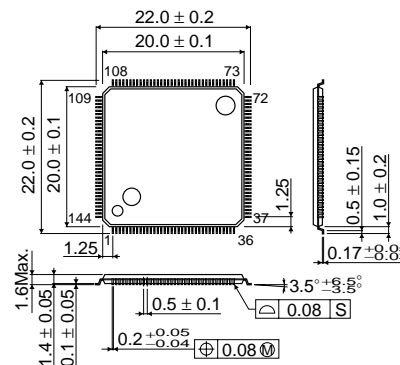
Basic functions for EDR (Camera I/F, JPEG codec, PCM ADPCM codec, SD card controller and 4ch AD converter) are implemented as hardware to reduce internal ARM9's software loads. So the EDR gives safty-drive/economic-drive aided functions of a product.

BU1511KV2 gives the EDR product concept of low cost, safty-drive/economic-drive aided product and its usages without PC

●Features

- 1) ARM946E-S is built-in
- 2) Camera I/F, JPEG/PCM(ADPCM) codec, SD card controller are built-in
And each function block is implemented as hardware block
- 3) TV-encoder is built-in to play the event
- 4) 4ch AD converter is built-in for a 3-axis accelerometer
- 5) Program upload function to internal I-TCM(64KB) from external serial FLASH

●Dimensions (Unit: mm)



VQFP-T144

●Applications

Event Data Recorder(EDR) which can record/play Audio/Video event data

●Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Parameter	Symbol	Rating	Unit
Power supply voltage 1 (DAC)	DAVDD	-0.3~+4.2	V	Input voltage(ADC)	VIN1	-0.3~ADVDD+0.3	V
Power supply voltage 2 (ADC)	ADVDD	-0.3~+4.2	V	Input voltage(I2C-1)	VIN2	-0.3~I1VDD+0.3	V
Power supply voltage 3 (I2C-1)	I1VDD	-0.3~+4.2	V	Input voltage(I2C-2)	VIN3	-0.3~I2VDD+0.3	V
Power supply voltage 4 (I2C-2)	I2VDD	-0.3~+4.2	V	Input voltage(SD-CARD)	VIN4	-0.3~SDVDD+0.3	V
Power supply voltage 5 (SD-CARD)	SDVDD	-0.3~+4.2	V	Input voltage(CAMERA)	VIN5	-0.3~CAVDD+0.3	V
Power supply voltage 6(CAMERA)	CAVDD	-0.3~+4.2	V	Input voltage(Other IO)	VIN6	-0.3~IOVDD+0.3	V
Power supply voltage 7(Other IO)	IOVDD	-0.3~+4.2	V	Storage temperature range	Tstg	-40~+150	°C
Power supply voltage 8(Digital CORE)	DVDD	-0.3~+2.1	V	Power dissipation	PD	1200*1, 1700*2	mW

*1 IC only. In the case of exceeding 25°C, 12.0 mW should be reduced at the rating 1°C.

*2 When packaging a glass epoxy board of 270x70x1.6mm. If exceeding 25°C, 17mW should be reduced at the rating 1°C.

* Has not been designed to withstand radiation.

●Recommended Operating Range (Ta=25°C unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage 1 (DAC)	DAVDD	3.00	3.30	3.60	V
Power supply voltage 2 (ADC)	ADVDD	3.00	3.30	3.60	V
Power supply voltage 3 (I2C-1)	I1VDD	2.40	3.30	3.60	V
Power supply voltage 4 (I2C-2)	I2VDD	2.40	3.30	3.60	V
Power supply voltage 5 (SD-CARD)	SDVDD	2.70	3.30	3.60	V
Power supply voltage 6 (CAMERA)	CAVDD	2.30	2.85	3.30	V
Power supply voltage 7 (Other IO)	IOVDD	1.70	3.30	3.60	V
Power supply voltage 8 (Digital CORE)	DVDD	1.45	1.50	1.55	V
Operating temperature range	Topr	-40	-	85	°C

* Please supply power source in order of CORE(DVDD) → IO(IOVDD,CAVDD,SDVDD,I1VDD,I2VDD,ADVDD,DAVDD)

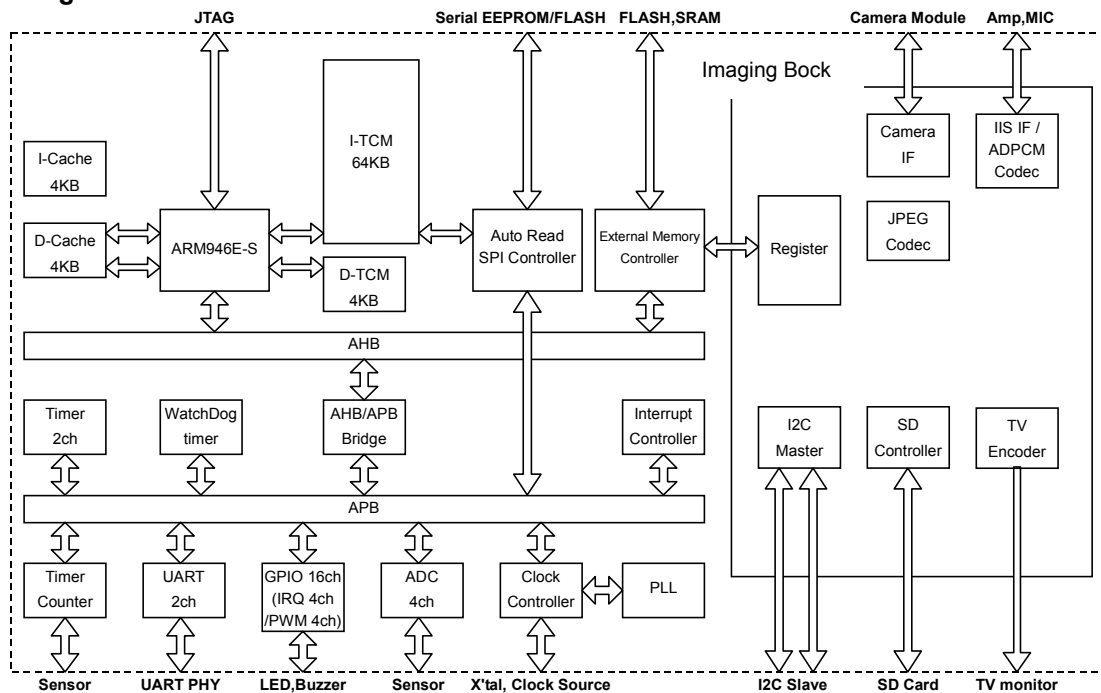
* Please keep RESETB terminal is LOW, until power supply is stable.

●Electrical Characteristics

(Unless otherwise specified, DVDD=1.50V, DAVDD=ADVDD=1VDD=I2VDD=SDVDD=IOVDD=3.30V, CAVDD=2.85V, DAVSS=ADVSS=DVSS=0.0V, Ta=25°C, fXIN=13.5MHz, fAXIN=16.384MHz, fSYS=41.0MHz(Internal Clock with PLL) IOPWR is a generic name of I1VDD,I2VDD,SDVDD,CAVDD,IOVDD.)

Parameter	Symbol	Specification		Unit	Conditions
		Min	Max		
Common					
Input frequency 1	fXIN	5.0	30.0	MHz	XIN (Duty 50±10%), When PLL is ON.
Input frequency 2	fAXIN	8.284	32.768	MHz	AXIN(Duty 50±10%)
Internal clock frequency 1	fSYS	-	41.0	MHz	When PLL is ON, Except I2S Audio Block
Internal clock frequency 2	fAUD	-	32.768	MHz	I2S Audio Block
Static consumption current	IDDST	-	200	μA	When all clock stop
Logic Block					
Input "H" voltage 1	VIH1	IOPWR×0.8	IOPWR+0.3	V	Normal Input
Input "L" voltage 1	VIL1	-0.3	IOPWR×0.2	V	Normal Input
Input "H" voltage 2	VIH2	IOPWR×0.85	IOPWR+0.3	V	Hysteresis input pin
Input "L" voltage 12	VIL2	-0.3	IOPWR×0.15	V	(TIM_TRIG,NTRST,RESETB,BIT_SEL, TCM_SEL,AUTO_READ)
Output "H" voltage 1	VOH1	IOPWR-0.4	IOPWR	V	IOH=-2.0mA(DC), Output except SD_CLK, When CAVDD=3.3V
Output "L" voltage 1	VOL1	0.0	0.4	V	IOL=2.0mA(DC), Output except SD_CLK, When CAVDD=3.3V.
Output "H" voltage 2	VOH2	IOPWR-0.4	IOPWR	V	IOH=-4.0mA(DC), SD_CLK
Output "L" voltage 2	VOL2	0.0	0.4	V	IOL=4.0mA(DC), SD_CLK
DACBlock					
DAC Bit Width	RES_DA	-	10	bits	
DAC Operating current	IDDDA	32	42	mA	R _L =37.5Ω, R _{REF} =2.4kΩ, DAVDD Pin current
DAC Static consumption current	IDDSTDA	-	5	μA	R _L =37.5Ω, R _{REF} =2.4kΩ, DAVDD Pin current
Integral Non-linearity	INL_DA	-8.0	+8.0	LSB	R _L =37.5Ω, R _{REF} =2.4kΩ
Differential Non-linearity	DNL_DA	-2.0	+2.0	LSB	R _L =37.5Ω, R _{REF} =2.4kΩ
Full scale voltage	VFS_DA	1.1	1.4	V	R _L =37.5Ω, R _{REF} =2.4kΩ
ADCBlock					
ADC Bit Width	RES_AD	-	8	bits	
Input voltage (Upper Limit)	VIN_AD_T	ADVDD×0.85	ADVDD×0.95	V	
Input voltage (Lower Limit)	VIN_AD_B	ADVDD×0.05	ADVDD×0.15	V	
Integral Non-linearity	INL_AD	-2.0	+2.0	LSB	
Differential Non-linearity	DNL_AD	-2.0	+2.0	LSB	
Change Standard clock cycle	fADC	4.0	16.0	MHz	
Change cycle	fsps	30.8K	123K	sps	Sample per second Need 130°ADC_CLK for conversion by sweeping

●Block Diagram



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The content specified in this document is correct as of MAY 7, 2009.

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