200324741 Availability of Si5332 Rev1.3 Datasheet, Updated 40/48-LGA Package Designs

PCN Issue Date: 3/24/2020 **Effective Date:** 6/30/2020

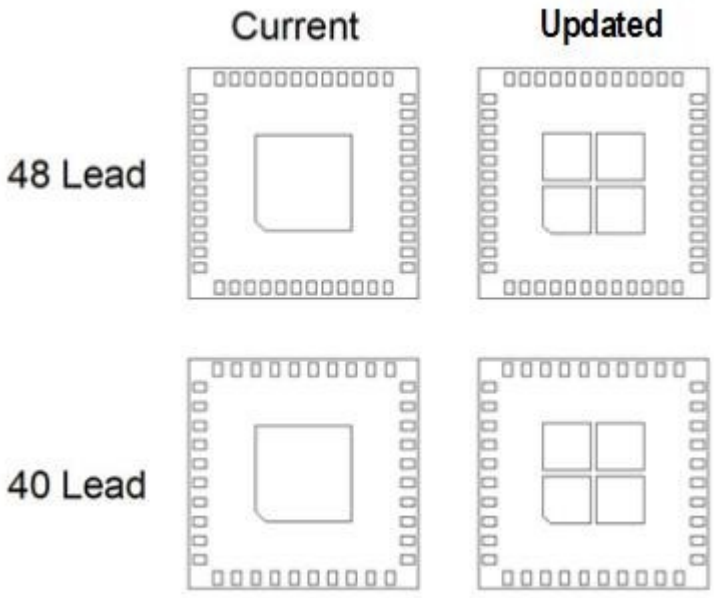
PCN Type: Datasheet; Other

Description of Change

Silicon Labs is pleased to announce the availability of revision 1.3 of the Si5332 datasheet.

Reason for Change

The following changes were made to the datasheet:
- Added new Si5332L ordering option, featuring integrated reference with tighter stability: ±30ppm
- Updated Package Outline Drawing for 40-pin 6x6mm LGA package, partitioning the center ground epad into a 2x2 grid array.
- Updated PCB Land Pattern Drawing stencil design recommendations for 40-pin 6x6mm LGA package.
- Updated Package Outline Drawing for 48-pin 6x6mm LGA package, partitioning the center ground epad into a 2x2 grid array.
- Updated PCB Land Pattern Drawing stencil design recommendations for 48-pin 6x6mm LGA package.



Package Lead Changes

Impact on Form, Fit, Function, Quality, Reliability

There is no impact on fit or function.

Form
In an effort to improve product quality, the 40-pin 6x6mm and 48-pin 6x6mm LGA packages used with Si5332E/F/G/H/L-grade devices are being updated. The single, center ground epad has been partitioned into a 2x2 grid array, divided with solder resist into 4 pads to increase mechanical support to the center of the package. There is no change made to any of the metal layers of the package. Revision 1.3 of the Si5332 datasheet includes the new, updated 40-pin and 48-pin 6x6mm LGA package outline drawings, partitioning the center ground epad into a 2x2 grid array, as shown above.

The PCB land pattern drawing stencil design notes for 40-pin and 48-pin 6x6mm LGA packages have been updated in revision 1.3 of the Si5332 datasheet to reflect the updated 2x2 grid ground pad array.

A review of the SMT stencil apertures on all designs that use Si5332E/F/G/H/L-grade devices in 40-pin and 48-pin LGA packages must be performed. Stencil updates to existing designs may be necessary to match the new 2x2 grid-array package patterns.

Last Date of Unchanged Product:
Silicon Labs will migrate all production orders of Si5332E/F/G/H/L-grade devices in 40-pin and 48-pin LGA packages from the current single-center epad design to the updated, partitioned 2x2 grid array in WW28. All production orders shipped prior to WW28 will use the current single-center epad design. All orders shipped after WW28 will use the new, updated 2x2 grid ground pad array design.

Product Identification

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Existing Part #
Si5332E-D-GM2
Si5332F-D-GM2
Si5332G-D-GM2
Si5332H-D-GM2
Si5332L-D-GM2
Si5332EDxxxxx-GM2
Si5332FDxxxxx-GM2
Si5332GDxxxxx-GM2
Si5332HDxxxxx-GM2
Si5332LDxxxxx-GM2
Si5332E-D-GM3
Si5332F-D-GM3
Si5332G-D-GM3
Si5332H-D-GM3
Si5332L-D-GM2
Si5332EDxxxxx-GM3
Si5332FDxxxxx-GM3
Si5332GDxxxxx-GM3
Si5332HDxxxxx-GM3
Si5332LDxxxxx-GM3
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Last Date of Unchanged Product: 6/30/2020

Qualification Samples

Available upon request.

Customer Response

Lack of acknowledgment of the PCN within 30 days constitutes acceptance of the change, Ref. JEDEC-J-STD-046.

To request further data or inquire about this notification, please contact your Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at http://www.silabs.com.

Customers may approve early PCN acceptance by emailing approval, along with PCN # to PCNEarlyAcceptance@silabs.com

User Registration

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Qualification Data

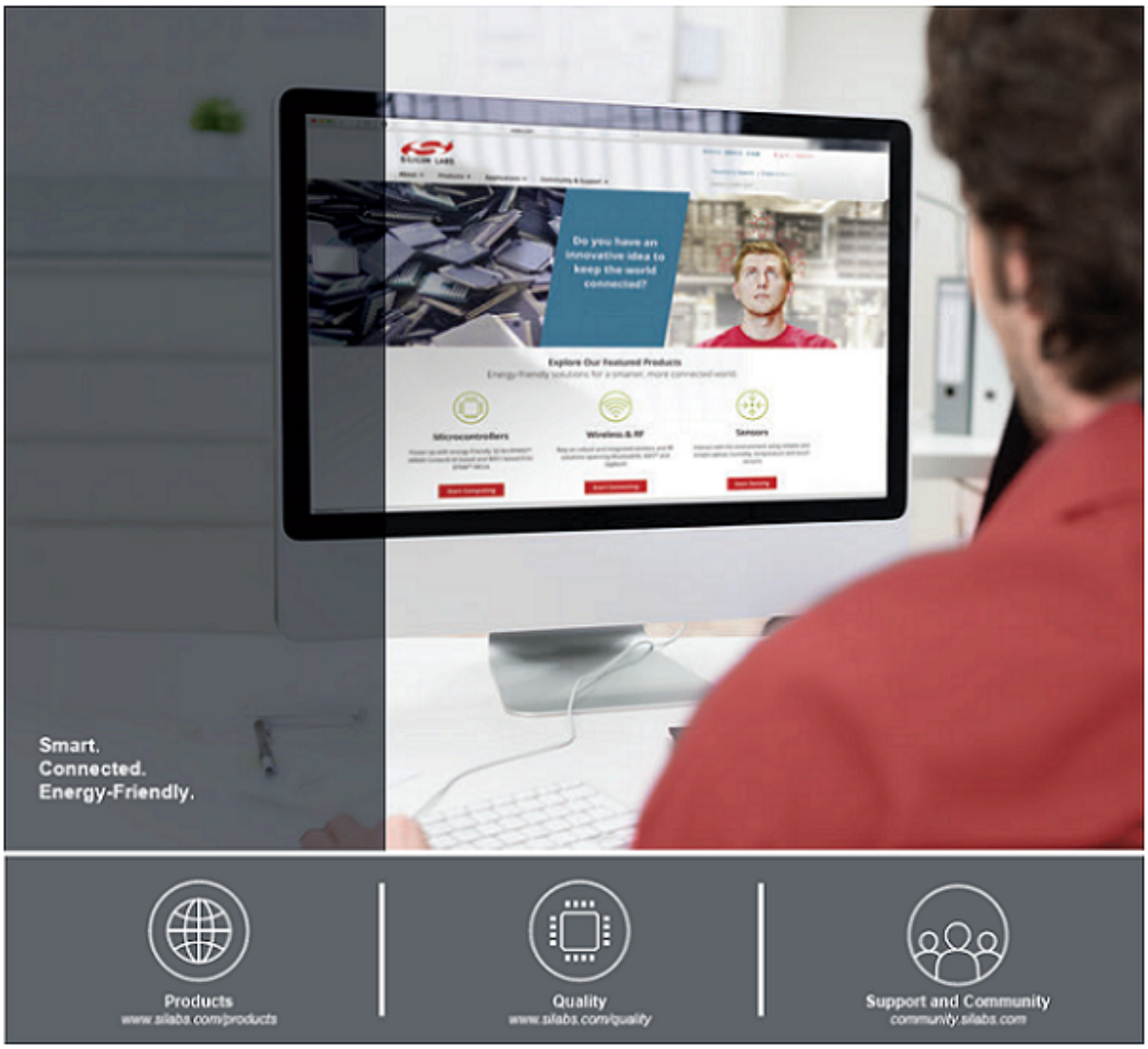
See attached.

Part Rev D, TSMC Fabrication, ASECL Assembly except as noted							
Test Name	**Test Condition**	**Qualification**	**Lot ID or Start**	**Fail/Pass or End**	**Notes**	**Summary**	**Status**
Test Group A – Accelerated Environment Stress Tests - 40/48-Pin 6x6 mm LGA							
HAST	JA110		Q042577	0/25	1		
	110°C, 85%RH	3 lots, N=>25	Q042578	0/25	1	3 lots	Pass
	Vcc=3.3V, 264 hours		Q042579	0/25	1	0/75	
Temp Cycle	JA104		Q045442	0/25	1		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q045443	0/25	1	3 lots	Pass
	500 cycles		Q045444	0/25	1	0/75	
HTSL	JA103		Q042580	0/25	1		
	150°C, 1000hr	3 lots, N=>25	Q042581	0/25	1	3 lots	Pass
			Q042582	0/25	1	0/75	
Test Group A – Accelerated Environment Stress Tests - 32-Pin 5x5 mm LGA							
HAST	JA110		Q042586	0/25	1		
	110°C, 85%RH	3 lots, N=>25	Q042587	0/25	1	3 lots	Pass
	Vcc=3.3V, 264 hours		Q042588	0/25	1	0/75	
Temp Cycle	JA104		Q042592	0/25	1		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q042593	0/25	1	3 lots	Pass
	500 cycles		Q042594	0/25	1	0/75	
HTSL	JA103		Q042589	0/25	1		
	150°C, 1000hr	3 lots, N=>25	Q042590	0/25	1	3 lots	Pass
			Q042591	0/25	1	0/75	
Test Group B – Accelerated Lifetime Simulation Tests							
HTOL	JA108		Q040841	0/80	2		
	T_J ≥ 125°C, Dynamic	3 lots, N=>77	Q041408	0/80	2	3 lots	Pass
	Vcc=3.3V, 1000 hours		Q042772	0/80	2	0/240	
LTOL	JA108						
	T_A = -10°C, Dynamic	1 lot, N=>32	Q035769	0/34	2	1 lots	Pass
	Vcc=3.3V, 1000 hours					0/34	
ELFR	JA108		Q040840	0/504	2		
	T_J ≥ 125°C, Dynamic	3 lots, N=>500	Q041018	0/504	2	3 lots	Pass
	Vcc=3.3V, 48 hours		Q042762	0/504		0/1512	
Test Group C – Package Assembly Integrity Tests - 40/48-Pin 6x6 mm LGA							
Mechanical Shock	JB104		Q042708	0/40			
	Condition B, 1,500g	3 lots, N=>39	Q042711	0/40		3 lots	Pass
			Q042714	0/40		0/120	
Mechanical Vibration	JB103		Q042709	0/40			
	Condition 1, 20g	3 lots, N=>39	Q042712	0/40		3 lots	Pass
			Q042715	0/40		0/120	
Constant Acceleration	M2001		Q042710	0/40			
	Condition B, 10,000g	3 lots, N=>39	Q042713	0/40		3 lots	Pass
			Q042716	0/40		0/120	

Part Rev D, TSMC Fabrication, ASECL Assembly except as noted							
Test Name	**Test Condition**	**Qualification**	**Lot ID or Start**	**Fail/Pass or End**	**Notes**	**Summary**	**Status**
Test Group C – Package Assembly Integrity Tests - 32-Pin 5x5 mm LGA							
Mechanical Shock	JB104 Condition B, 1,500g	3 lots, N=>39	Q042717 Q042720 Q042723	0/40 0/40 0/40		3 lots 0/120	Pass
Mechanical Vibration	JB103 Condition 1, 20g	3 lots, N=>39	Q042718 Q042721 Q042724	0/40 0/40 0/40		3 lots 0/120	Pass
Constant Acceleration	M2001 Condition B, 10,000g	3 lots, N=>39	Q042719 Q042722 Q042725	0/40 0/40 0/40		3 lots 0/120	Pass
Test Group E – Electrical Verification							
ESD-HBM	JS-001	1 lot, N=>3	Q040754		2	3 kV	Class 2
ESD-CDM	JESD22-C101	1 lot, N=>3	Q042509			500 V	Class III
ESD-CDM	JESD22-C101	1 lot, N=>3	Q042527			750 V	Class III
Latch Up	JESD78 ±100mA Overvoltage = 4.95V	1 lot, N=>3	Q040756	85 °C	2		Pass

Notes:
1. Parts are Pre-conditioned at MSL3/260°C
2. Leveraged die family qualification data

This report applies to the following part numbers:				
Si5332E-D-GM1	Si5332E-D-GM1R	Si5332E-D-GM2	Si5332E-D-GM2R	Si5332E-D-GM3
Si5332E-D-GM3R	Si5332F-D-GM1	Si5332F-D-GM1R	Si5332F-D-GM2	Si5332F-D-GM2R
Si5332F-D-GM3	Si5332F-D-GM3R	Si5332G-D-GM1	Si5332G-D-GM1R	Si5332G-D-GM2
Si5332G-D-GM2R	Si5332G-D-GM3	Si5332G-D-GM3R	Si5332H-D-GM1	Si5332H-D-GM1R
Si5332H-D-GM2	Si5332H-D-GM2R	Si5332H-D-GM3	Si5332H-D-GM3R	Si5332EDxxxxx-GM1
Si5332EDxxxxx-GM1R	Si5332EDxxxxx-GM2	Si5332EDxxxxx-GM2R	Si5332EDxxxxx-GM3	Si5332EDxxxxx-GM3R
Si5332FDxxxxx-GM1	Si5332FDxxxxx-GM1R	Si5332FDxxxxx-GM2	Si5332FDxxxxx-GM2R	Si5332FDxxxxx-GM3
Si5332FDxxxxx-GM3R	Si5332GDxxxxx-GM1	Si5332GDxxxxx-GM1R	Si5332GDxxxxx-GM2	Si5332GDxxxxx-GM2 R
Si5332GDxxxxx-GM3	Si5332GDxxxxx-GM3R	Si5332HDxxxxx-GM1	Si5332HDxxxxx-GM1R	Si5332HDxxxxx-GM2
Si5332HDxxxxx-GM2R	Si5332HDxxxxx-GM3	Si5332HDxxxxx-GM3R	Si5357ADxxxxx-GM	Si5357ADxxxxx-GMR
Si5332L-D-GM1	Si5332L-D-GM1R	Si5332L-D-GM2	Si5332L-D-GM2R	Si5332L-D-GM3
Si5332L-D-GM3R	Si5332LDxxxxx-GM1	Si5332LDxxxxx-GM1R	Si5332LDxxxxx-GM2	Si5332LDxxxxx-GM2R
Si5332LDxxxxx-GM3	Si5332LDxxxxx-GM3R			



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