MOSFET – N-Channel, POWERTRENCH®

100 V, 300 A, 2.0 mΩ

FDBL0200N100

Features

- Typical $R_{DS(on)}$ = 1.5 mΩ at V_{GS} = 10 V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 95 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- This Device is Pb−Free and is RoHS Compliant

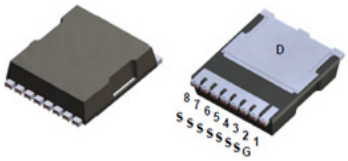
Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated Tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch

ON Semiconductor®

www.onsemi.com

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
100 V	2.0 mΩ @ 10 V	300 A



H−PSOF8L 11.68x9.80
CASE 100CU

MARKING DIAGRAM

$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= 3−Digit Plant Code
&K	= 2−Digits Lot Run Traceability Code
FDBL0200N100	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Rating		Value	Unit
V_{DSS}	Drain−to−Source Voltage		100	V
V_{GS}	Gate−to−Source Voltage		±20	V
I_D	Drain Current − Continuous (V_{GS} = 10) (Note 1)	T_C = 25°C	300	A
	Pulsed Drain Current	T_C = 25°C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)		352	mJ
P_D	Power Dissipation		429	W
	Derate Above 25°C		2.9	W/°C
T_J, T_{STG}	Operating and Storage Temperature		−55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 3)		0.35	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3a)		43	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3b)		62.5	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by silicon.
2. Starting T_J = 25°C, L = 0.1 mH, I_{AS} = 84 A, V_{DD} = 100 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design.
   a. 43°C/W when mounted on a 1 in^2 pad of 2 oz copper
   b. 62.5°C/W when mounted on a minimum pad of 2 oz copper

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
B_{VDSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		100	–	–	V
I_{DSS}	Drain−to−Source Leakage Current	V_{DS} = 100 V, V_{GS} = 0 V	T_J = 25°C	–	–	5	μA
			T_J = 175°C (Note 4)	–	–	2	mA
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA		2.0	3.1	4.5	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 80A, V_{GS}= 10V	T_J = 25°C	–	1.5	2.0	mΩ
			T_J = 175°C (Note 4)	–	3.3	4.3	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		–	6970	9760	pF
C_{oss}	Output Capacitance			–	3950	5530	pF
C_{rss}	Reverse Transfer Capacitance			–	29	41	pF
R_g	Gate Resistance	f = 1 MHz		–	0.45	1	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10 V	V_{GS} = 0 to 10 V, V_{DD} = 80 V, I_D = 80 A		–	95	133	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V, V_{DD} = 80 V, I_D = 80 A		–	13	–	nC
Q_{gs}	Gate−to−Source Gate Charge	V_{DD} = 80 V, I_D = 80 A		–	31	–	nC
Q_{gd}	Gate−to−Drain “Miller“ Charge			–	20	–	nC
SWITCHING CHARACTERISTICS							
t_{on}	Turn−On Time	V_{DD} = 50 V, I_D = 80 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		–	–	73	ns
$t_{d(on)}$	Turn−On Delay			–	31	50	ns
t_r	Rise Time			–	25	40	ns
$t_{d(off)}$	Turn−Off Delay			–	36	58	ns
t_f	Fall Time			–	9	18	ns
t_{off}	Turn−Off Time			–	–	59	ns
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source−to−Drain Diode Voltage	I_{SD} = 80 A, V_{GS} = 0 V		–	–	1.25	V
		I_{SD} = 40 A, V_{GS} = 0 V		–	–	1.2	V
t_{rr}	Reverse−Recovery Time	I_F = 80 A, dI_{SD}/dt = 100 A/μs, V_{DD} = 80 V		–	115	184	ns
Q_{rr}	Reverse−Recovery Charge			–	172	273	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

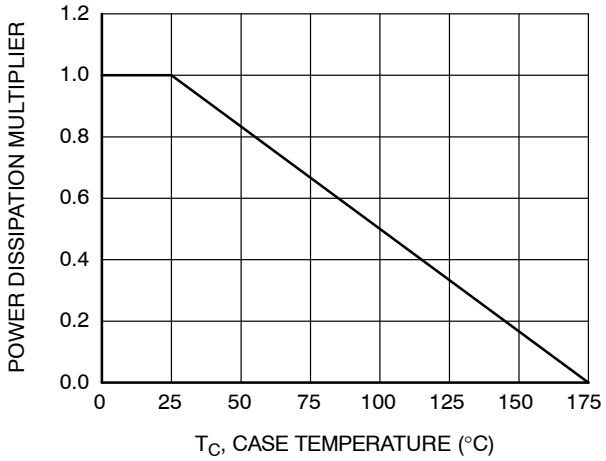


Figure 1. Normalized Power Dissipation vs. Case Temperature

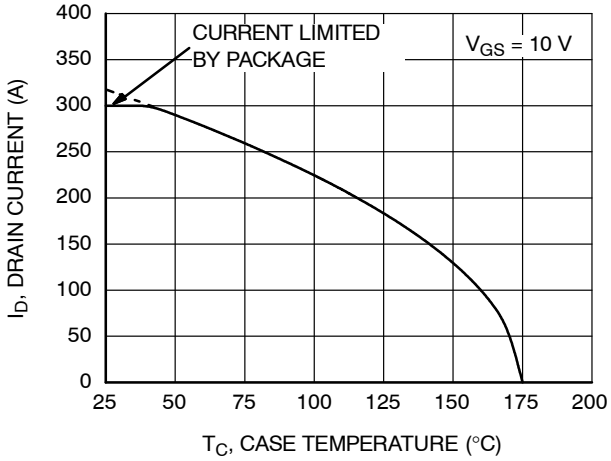


Figure 2. Maximum Drain Current vs. Case Temperature

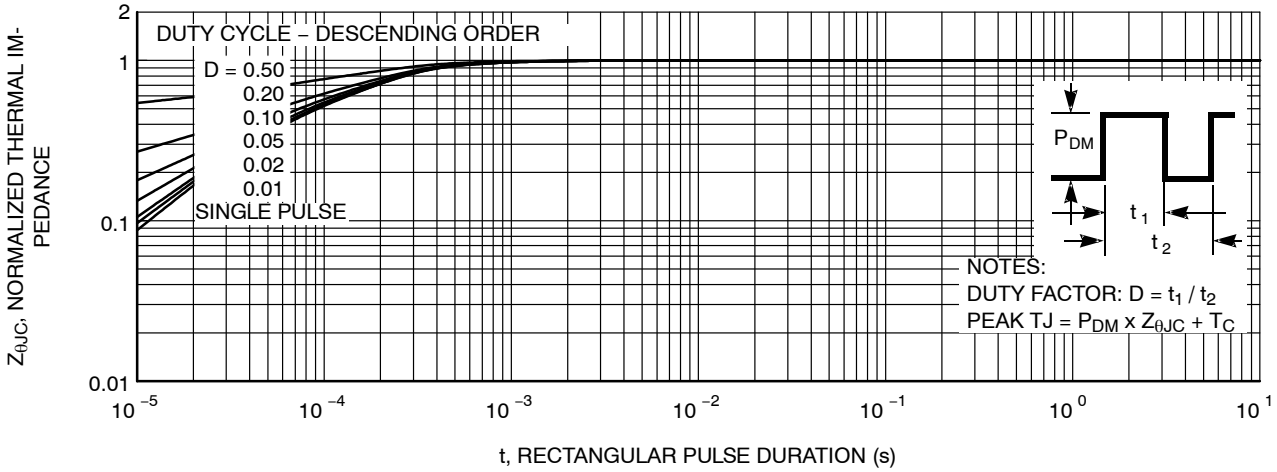


Figure 3. Normalized Maximum Transient Thermal Impedance

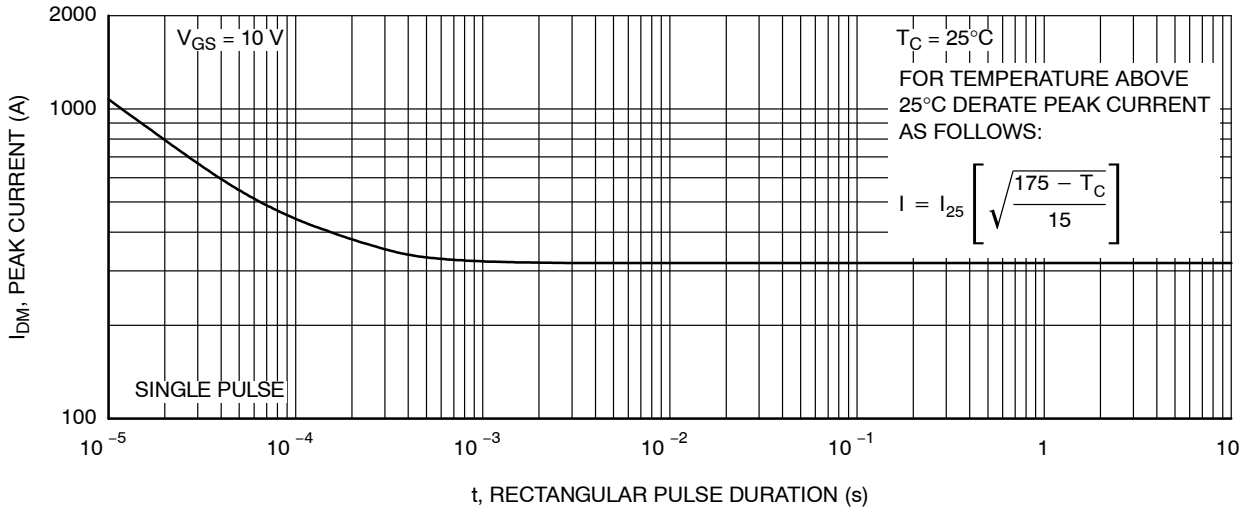


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

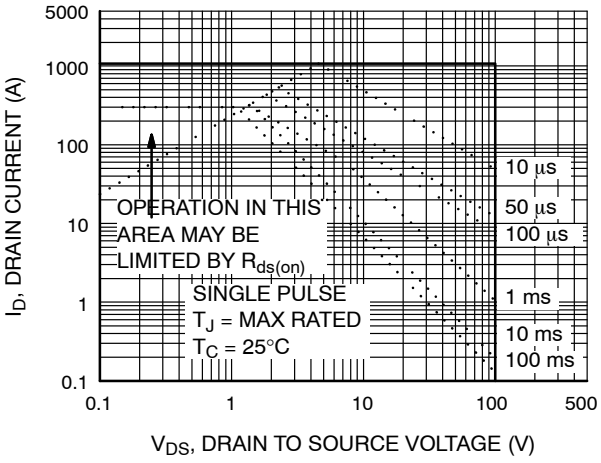
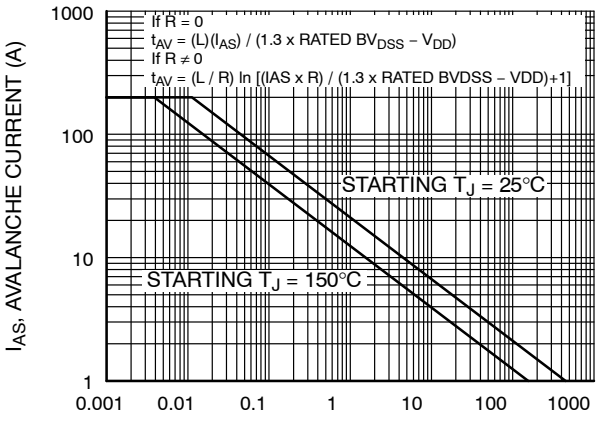


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN−7514 and AN−7515

Figure 6. Unclamped Inductive Switching Capability

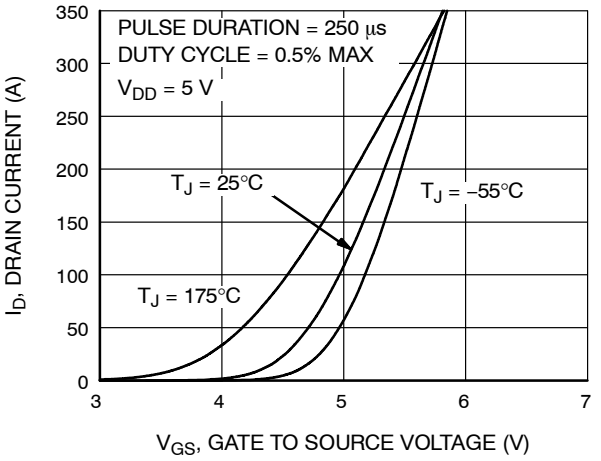


Figure 7. Transfer Characteristics

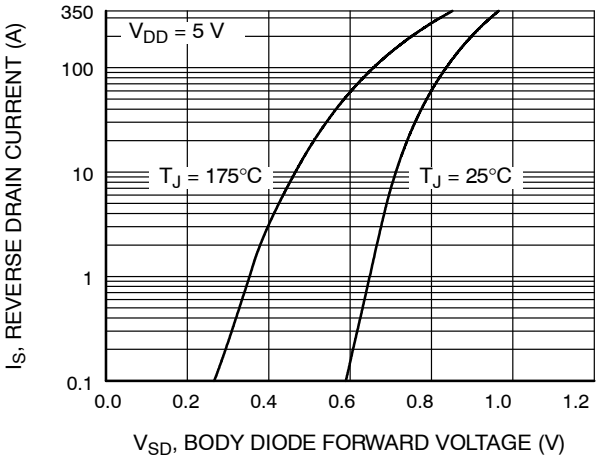


Figure 8. Forward Diode Characteristics

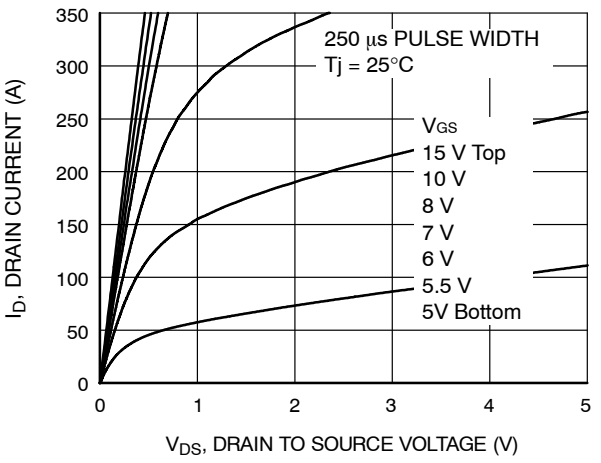


Figure 9. Saturation Characteristics

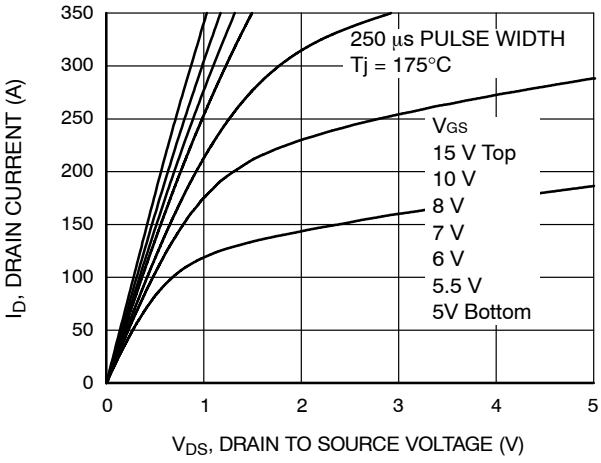


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

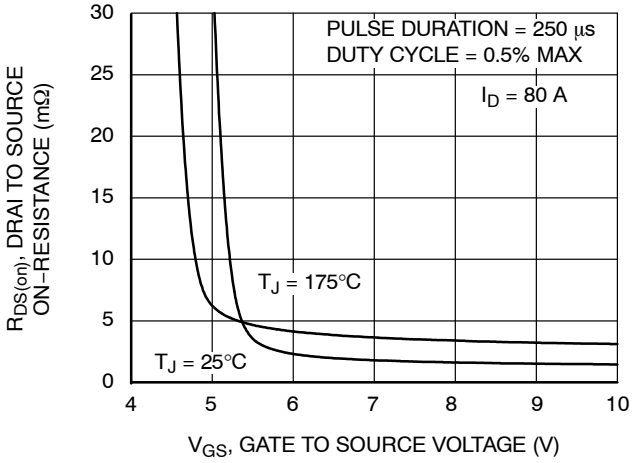


Figure 11. R_{DSON} vs. Gate Voltage

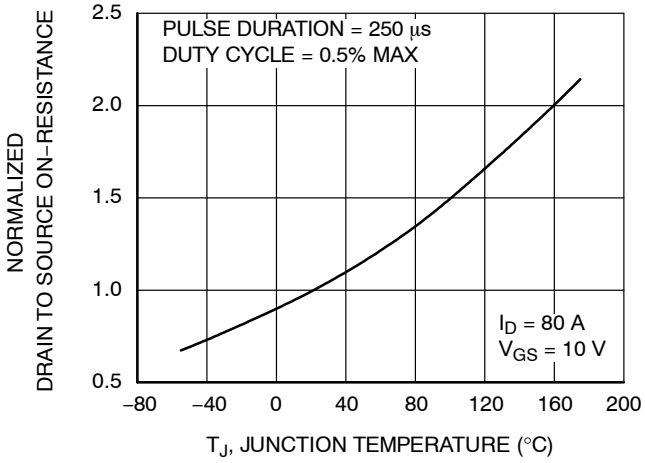


Figure 12. Normalized R_{DSON} vs. Junction Temperature

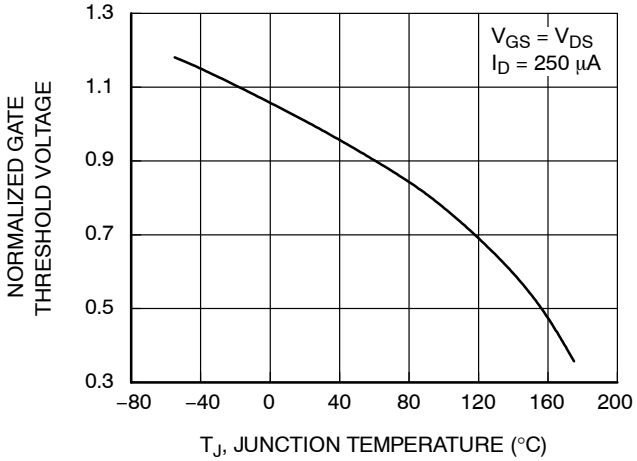


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

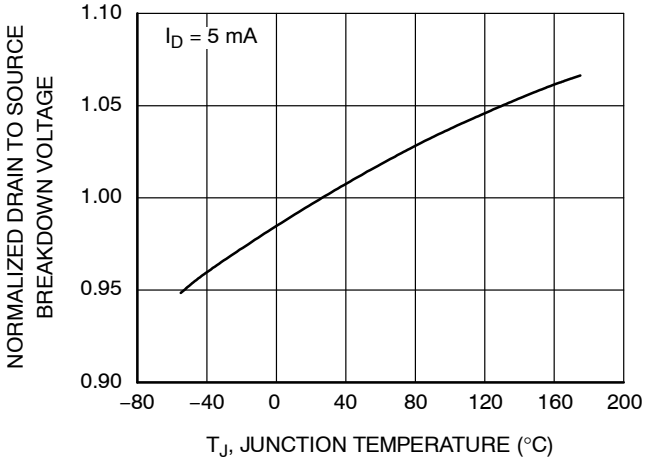


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

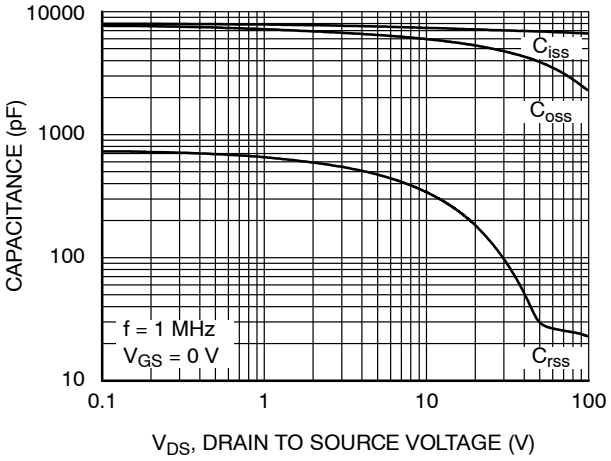


Figure 15. Capacitance vs. Drain to Source Voltage

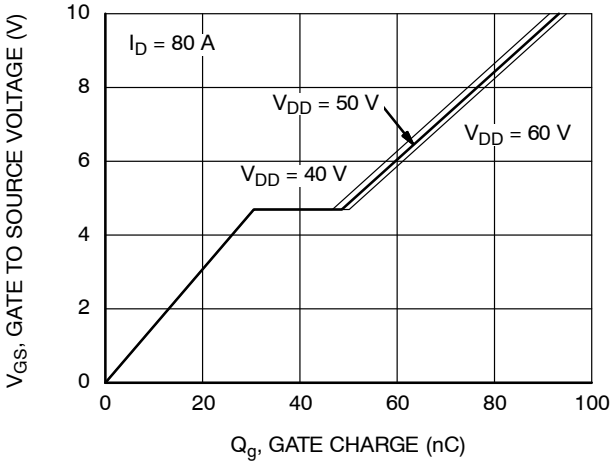


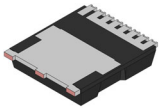
Figure 16. Gate Charge vs. Gate to Source Voltage

ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping†
FDBL0200N100	FDBL0200N100	H−PSOF8L 11.68x9.80 (Pb−Free)	13”	24 mm	2000 / Tape & Reel

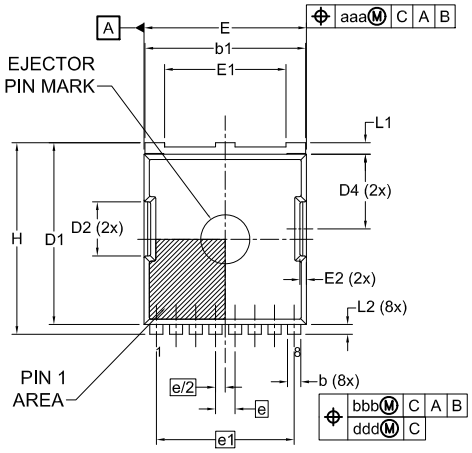
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

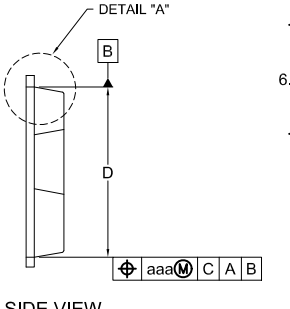


H−PSOF8L 11.68x9.80
CASE 100CU
ISSUE C

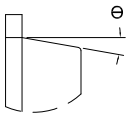
DATE 22 MAY 2023



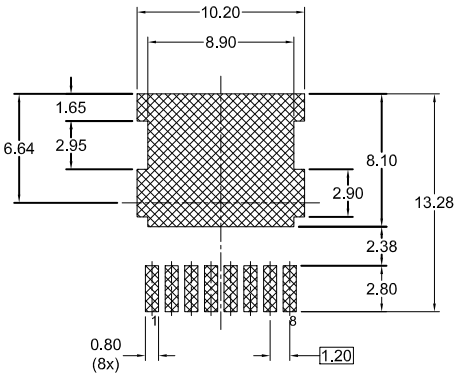
TOP VIEW



SIDE VIEW

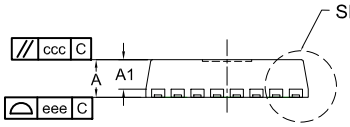


DETAIL "A"
SCALE: 2X

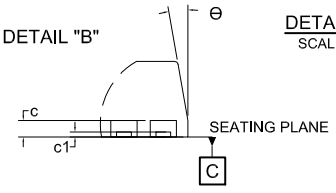


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



FRONT VIEW



DETAIL "B"
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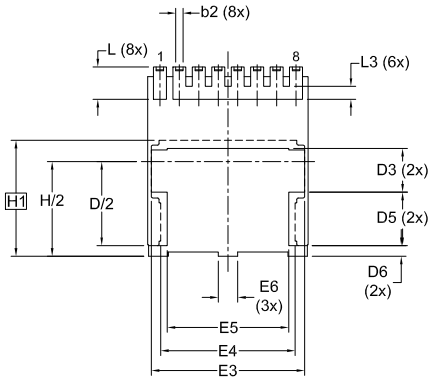


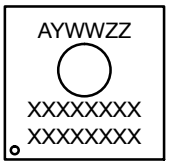
BOTTOM VIEW

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
c1	0.10	—	—
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	9.36	9.46	9.56

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	8.20	8.30	8.40
E5	7.40	7.50	7.60
E6	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	0°	—	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON13813G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**H−PSOF8L 11.68x9.80**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales