ADS5474 14-Bit, 400-MSPS Analog-to-Digital Converter

1 Features

- 400-MSPS Sample Rate
- 14-Bit Resolution, 11.2-Bits ENOB
- 1.4-GHz Input Bandwidth
- 80-dBc SFDR at 230 MHz and 400 MSPS
- 69.8-dBFS SNR at 230 MHz and 400 MSPS
- 2.2-V_{PP} Differential Input Voltage
- LVDS-Compatible Outputs
- 2.5-W Total Power Dissipation
- 50-mW Power-Down Mode
- Offset Binary Output Format
- Output Data Transitions on the Rising and Falling Edges of a Half-Rate Output Clock
- On-Chip Analog Buffer, Track-and-Hold, and Reference Circuit
- HTQFP-80 PowerPAD™ Package (14-mm × 14-mm Footprint)
- Industrial Temperature Range: –40°C to +85°C
- Pin-Similar, -Compatible With 12-, 13-, and 14-Bit Family: ADS5463, ADS5440, ADS5444

2 Applications

- Test and Measurement Instrumentation
- Software-Defined Radio
- Data Acquisition
- Power Amplifier Linearization
- Communication Instrumentation
- Radar

3 Description

The ADS5474 device is a 14-bit, 400-MSPS analog-to-digital converter (ADC) that operates from both a 5-V supply and 3.3-V supply while providing LVDS-compatible digital outputs. This ADC is one of a family of 12-, 13-, and 14-bit ADCs that operate from 210 MSPS to 500 MSPS. The ADS5474 device has an input buffer that isolates the internal switching of the onboard track and hold (T&H) from disturbing the signal source while providing a high-impedance input. An internal reference generator is also provided to simplify the system design.

Designed with a 1.4-GHz input bandwidth for the conversion of wide-bandwidth signals that exceed 400 MHz of input frequency at 400 MSPS, the ADS5474 device has outstanding low-noise performance and spurious-free dynamic range over a large input frequency range.

The ADS5474 device is available in an TQFP-80 PowerPAD package. The device is built on Texas Instruments complementary bipolar process (BiCom3) and is specified over the full industrial temperature range (–40°C to +85°C).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS5474	HTQFP (80)	12.00 mm x 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram

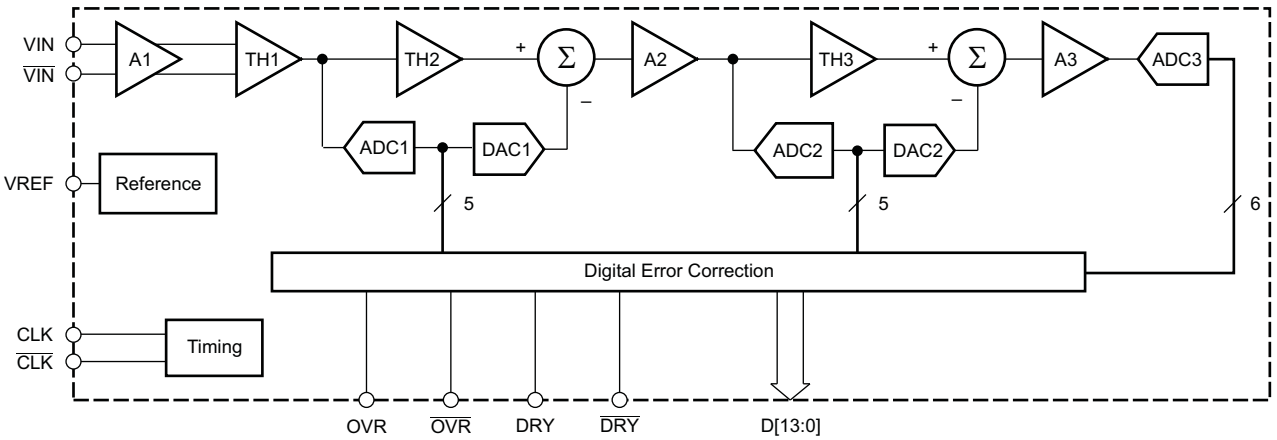


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 6
6.1 Absolute Maximum Ratings ... 6
6.2 ESD Ratings ... 6
6.3 Recommended Operating Conditions ... 6
6.4 Thermal Information ... 7
6.5 Electrical Characteristics ... 7
6.6 Timing Characteristics ... 10
6.7 Typical Characteristics ... 12
7 Detailed Description ... 18
7.1 Overview ... 18
7.2 Functional Block Diagram ... 18
7.3 Feature Description ... 18
7.4 Device Functional Modes ... 21
8 Application and Implementation ... 24
8.1 Application Information ... 24
8.2 Typical Applications ... 24
9 Power Supply Recommendations ... 28
9.1 Power Supplies ... 28
10 Layout ... 29
10.1 Layout Guidelines ... 29
10.2 Layout Example ... 30
10.3 Thermal Considerations ... 30
11 Device and Documentation Support ... 32
11.1 Device Support ... 32
11.2 Documentation Support ... 33
11.3 Receiving Notification of Documentation Updates 33
11.4 Community Resources ... 33
11.5 Trademarks ... 33
11.6 Electrostatic Discharge Caution ... 33
11.7 Glossary ... 34
12 Mechanical, Packaging, and Orderable Information ... 34

4 Revision History

Changes from Revision C (January 2016) to Revision D **Page**

- Changed CLK input sample rate (sine wave) parameter maximum specification from *400 MSPS* to *404 MSPS* ... 6
- Changed max sample rate from 400 MHz to 404 MHz in *Detailed Design Procedure* section ... 25

Changes from Revision B (February 2012) to Revision C **Page**

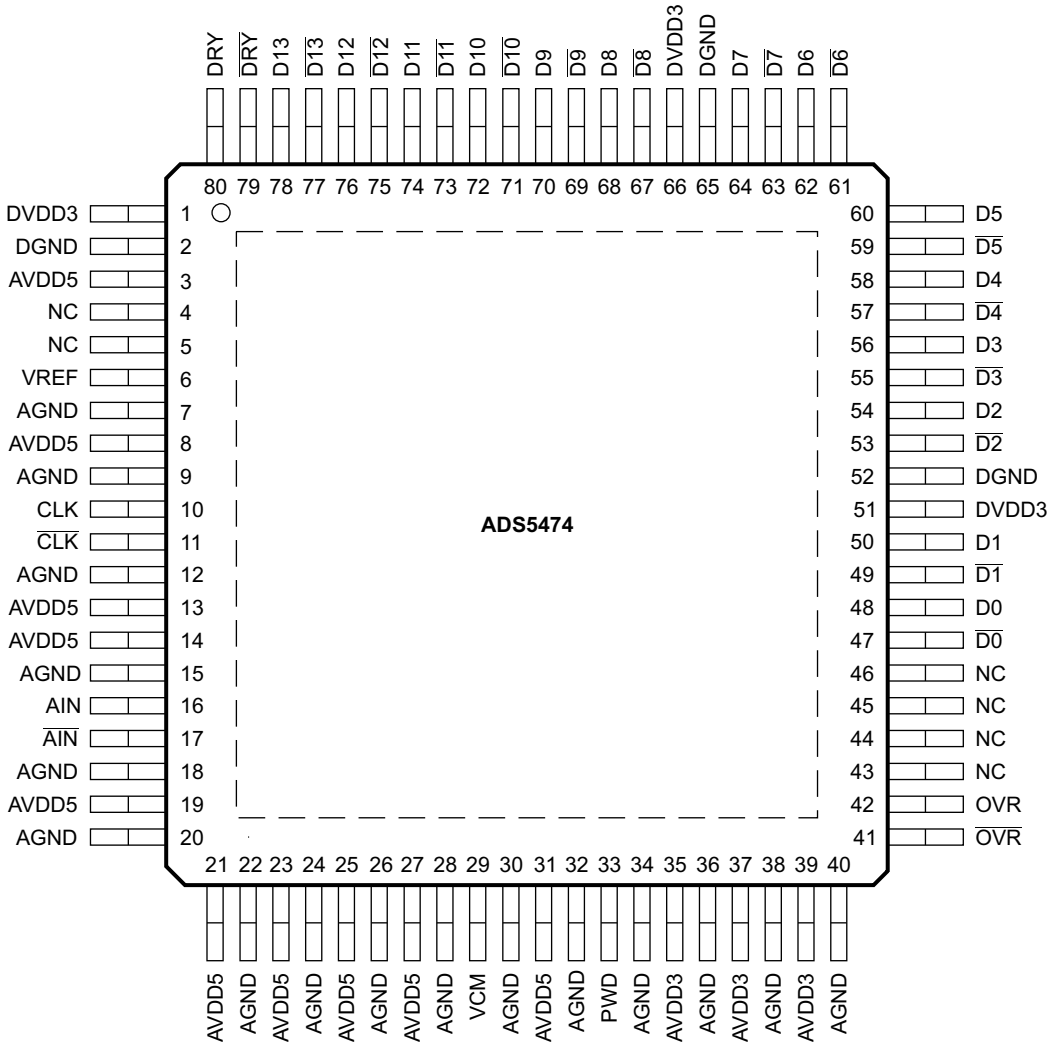
- Added ESD Ratings table, *Feature Description* section, *Device Functional Modes*section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 3

Changes from Revision A (August 2008) to Revision B **Page**

- Changed 1.6pF to 2.3pF TYP Input capacitance in ELECTRICAL CHARACTERISTICS ... 7
- Changed (where DRY equals the CLK frequency) to (where DRY equals ½ the CLK frequency) in Digital Outputs section ... 21

5 Pin Configuration and Functions

PFP Package
80-Pin HTQFP With PowerPAD
Top View



P0027-03

(1) NC - No internal connection.

Pin Functions

PIN			DESCRIPTION
NAME	NO.	TYPE	
AIN	16	I	Differential input signal (positive)
$\overline{\text{AIN}}$	17	I	Differential input signal (negative)
AVDD5	3		Analog power supply (5 V)
	8		
	13		
	14		
	19		
	21		
	23		
	25		
	27		
	31		
AVDD3	35		Analog power supply (3.3 V) (suggestion for ≤ 250 MSPS: leave option to connect to 5 V for ADS5440, ADS5444 13-bit compatibility)
	37		
	39		
DVDD3	1		Digital and output driver power supply (3.3 V)
	51		
	66		
AGND	7		Analog Ground
	9		
	12		
	15		
	18		
	20		
	22		
	24		
	26		
	28		
	30		
	32		
	34		
	36		
	38		
	40		
DGND	2		Digital Ground
	52		
	65		
CLK	10	I	Differential input clock (positive). Conversion is initiated on rising edge, digital outputs on falling edge.
$\overline{\text{CLK}}$	11	I	Differential input clock (negative)
D0	48	O	LVDS digital output pair, least significant bit (LSB)
$\overline{\text{D0}}$	47		

Pin Functions (continued)

PIN			DESCRIPTION
NAME	NO.	TYPE	
D1	50	O	LVDS digital output pairs
$\overline{D1}$	49		
D2	54		
$\overline{D2}$	53		
D3	56		
$\overline{D3}$	55		
D4	58		
$\overline{D4}$	57		
D5	60		
$\overline{D5}$	59		
D6	62		
$\overline{D6}$	61		
D7	64		
$\overline{D7}$	63		
D8	68		
$\overline{D8}$	67		
D9	70		
$\overline{D9}$	69		
D10	72		
$\overline{D10}$	71		
D11	74		
$\overline{D11}$	73		
D12	76		
$\overline{D12}$	75		
D13	78	O	LVDS digital output pair, most significant bit (MSB)
$\overline{D13}$	77		
DRY	80	O	Data ready LVDS output pair
$\overline{DRY}$	79		
NC	4	-	No connection (pins 4 and 5 should be left floating)
	5		
	43	-	No connection (pins 43 to 46 are possible future bit additions for this pinout and therefore can be connected to a digital bus or left floating)
	44		
	45		
	46		
OVR	42	O	Overrange indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
$\overline{OVR}$	41		
VCM	29	O	Common-mode voltage output (3.1 V nominal). Commonly used in DC-coupled applications to set the input signal to the correct common-mode voltage. A 0.1-μF capacitor from VCM to AGND is recommended, but not required. (This pin is not used on the ADS5440, ADS5444, and ADS5463)
PWD	33		Power-down (active high). Device is in sleep mode when PWD pin is logic HIGH. ADC converter is awake when PWD is logic LOW (grounded). (This pin is not used on the ADS5440, ADS5444, and ADS5463)
VREF	6		Reference voltage input/output (2.4 V nominal). A 0.1-μF capacitor from VREF to AGND is recommended, but not required.
(Power Pad)	(not numbered)		Power Pad for thermal relief, also Analog Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Supply voltage	AVDD5 to GND		6	V
	AVDD3 to GND		5	
	DVDD3 to GND		5	
Analog input to GND	Valid when supplies are on and within normal ranges. See additional information in the Power Supplies portion of the applications information in the back of the datasheet regarding Clock and Analog Inputs when the supplies are off.	–0.3	(AVDD5 + 0.3)	V
Clock input to GND		–0.3	(AVDD5 + 0.3)	V
CLK to $\overline{\text{CLK}}$		–2.5	2.5	V
Digital data output to GND		–0.3	(DVDD3 + 0.3)	V
Operating temperature range		–40	85	°C
Maximum junction temperature			+150	°C
Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
SUPPLIES					
AVDD5	Analog supply voltage	4.75	5	5.25	V
AVDD3	Analog supply voltage	3.1	3.3	3.6	V
DVDD3	Output driver supply voltage	3	3.3	3.6	V
ANALOG INPUT					
	Differential input range		2.2		V_{PP}
VCM	Input common mode		3.1		V
DIGITAL OUTPUT (DRY, DATA, OVR)					
	Maximum differential output load		10		pF
CLOCK INPUT (CLK)					
	CLK input sample rate (sine wave)	20		404	MSPS
	Clock amplitude, differential sine wave (see Figure 37)	0.5		5	V_{PP}
	Clock duty cycle (see Figure 31)	40%	50%	60%	
T_A	Operating free-air temperature	–40		+85	°C

6.4 Thermal Information

THERMAL METRIC(1)		ADS5474 PFP (HTQFP) 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values at T_A = 25°C: minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = 400 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				14		Bits
ANALOG INPUTS						
	Differential input range			2.2		V_{PP}
	Analog input common-mode voltage	Self-biased; see VCM specification below		3.1		V
	Input resistance (dc)	Each input to VCM		500		Ω
	Input capacitance	Each input to GND		2.3		pF
	Analog input bandwidth (–3dB)			1.44		GHz
CMRR	Common-mode rejection ratio	Common-mode signal < 50 MHz (see Figure 27)		100		dB
INTERNAL REFERENCE VOLTAGE						
VREF	Reference voltage			2.4		V
VCM	Analog input common-mode voltage reference output	With internal VREF. Provided as an output via the VCM pin for dc-coupled applications. If an external VREF is used, the VCM pin tracks as illustrated in Figure 42	2.9	3.1	3.3	V
	VCM temperature coefficient			–0.8		mV/°C
DYNAMIC ACCURACY						
	No missing codes			Assured		
DNL	Differential linearity error	f_{IN} = 70 MHz	–0.99	±0.7	1.5	LSB
INL	Integral linearity error	f_{IN} = 70 MHz	–3	±1	3	LSB
	Offset error		–11		11	mV
	Offset temperature coefficient			0.02		mV/°C
	Gain error		–5		5	%FS
	Gain temperature coefficient			–0.02		%FS/°C
POWER SUPPLY						
I_{AVDD5}	5-V analog supply current	V_{IN} = full-scale, f_{IN} = 70 MHz, f_S = 400 MSPS		338	372	mA
I_{AVDD3}	3.3-V analog supply current	V_{IN} = full-scale, f_{IN} = 70 MHz, f_S = 400 MSPS		185	201	mA
I_{DVDD3}	3.3-V digital supply current (includes LVDS)	V_{IN} = full-scale, f_{IN} = 70 MHz, f_S = 400 MSPS		75	83	mA
	Total power dissipation			2.5	2.797	W
	Power-up time	From turn-on of AVDD5		50		µs

Electrical Characteristics (continued)

Typical values at T_A = 25°C: minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = 400 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Wake-up time	From PWD pin switched from HIGH (PWD active) to LOW (ADC awake) (see Figure 28)		5		µs
	Power-down power dissipation	PWD pin = logic HIGH		50	350	mW
PSRR	Power-supply rejection ratio, AVDD5 supply	Without 0.1-µF board supply capacitors, with < 1-MHz supply noise (see Figure 46)		75		dB
PSRR	Power-supply rejection ratio, AVDD3 supply	Without 0.1-µF board supply capacitors, with < 1-MHz supply noise (see Figure 46)		90		dB
PSRR	Power-supply rejection ratio, DVDD3 supply	Without 0.1-µF board supply capacitors, with < 1-MHz supply noise (see Figure 46)		110		dB
DYNAMIC AC CHARACTERISTICS						
SNR	Signal-to-noise ratio	f_{IN} = 30 MHz		70.3		dBFS
		f_{IN} = 70 MHz	68.3	70.2		
		f_{IN} = 130 MHz		70.1		
		f_{IN} = 230 MHz	68	69.8		
		f_{IN} = 351 MHz		69.1		
		f_{IN} = 451 MHz		68.4		
		f_{IN} = 651 MHz		67.5		
		f_{IN} = 751 MHz		66.6		
		f_{IN} = 999 MHz		64.7		
SFDR	Spurious-free dynamic range	f_{IN} = 30 MHz		88		dBc
		f_{IN} = 70 MHz	74	86		
		f_{IN} = 130 MHz		80		
		f_{IN} = 230 MHz	71	80		
		f_{IN} = 351 MHz		76		
		f_{IN} = 451 MHz		71		
		f_{IN} = 651 MHz		60		
		f_{IN} = 751 MHz		55		
		f_{IN} = 999 MHz		46		
HD2	Second-harmonic	f_{IN} = 30 MHz		89		dBc
		f_{IN} = 70 MHz		87		
		f_{IN} = 130 MHz		90		
		f_{IN} = 230 MHz		84		
		f_{IN} = 351 MHz		76		
		f_{IN} = 451 MHz		71		
		f_{IN} = 651 MHz		74		
		f_{IN} = 751 MHz		70		
		f_{IN} = 999 MHz		55		

Electrical Characteristics (continued)

Typical values at T_A = 25°C: minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = 400 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	Third-harmonic	f_{IN} = 30 MHz		93		dBc
		f_{IN} = 70 MHz		86		
		f_{IN} = 130 MHz		80		
		f_{IN} = 230 MHz		80		
		f_{IN} = 351 MHz		85		
		f_{IN} = 451 MHz		71		
		f_{IN} = 651 MHz		60		
		f_{IN} = 751 MHz		55		
		f_{IN} = 999 MHz		46		
	Worst harmonic, spur (other than HD2 and HD3)	f_{IN} = 30 MHz		95		dBc
		f_{IN} = 70 MHz		93		
		f_{IN} = 130 MHz		85		
		f_{IN} = 230 MHz		85		
		f_{IN} = 351 MHz		87		
		f_{IN} = 451 MHz		87		
		f_{IN} = 651 MHz		90		
		f_{IN} = 751 MHz		87		
		f_{IN} = 999 MHz		80		
THD	Total harmonic distortion	f_{IN} = 30 MHz		86		dBc
		f_{IN} = 70 MHz		83		
		f_{IN} = 130 MHz		78		
		f_{IN} = 230 MHz		77		
		f_{IN} = 351 MHz		75		
		f_{IN} = 451 MHz		68		
		f_{IN} = 651 MHz		60		
		f_{IN} = 751 MHz		55		
		f_{IN} = 999 MHz		45		
SINAD	Signal-to-noise and distortion	f_{IN} = 30 MHz		69.2		dBc
		f_{IN} = 70 MHz	67	68.9		
		f_{IN} = 130 MHz		68.5		
		f_{IN} = 230 MHz	65.5	68.2		
		f_{IN} = 351 MHz		67.3		
		f_{IN} = 451 MHz		64.8		
		f_{IN} = 651 MHz		58.5		
		f_{IN} = 751 MHz		54		
		f_{IN} = 999 MHz		45.4		
	Two-tone SFDR	f_{IN1} = 69 MHz, f_{IN2} = 70 MHz, each tone at –7 dBFS		93		dBFS
		f_{IN1} = 69 MHz, f_{IN2} = 70 MHz, each tone at –16 dBFS		95		
		f_{IN1} = 297.5 MHz, f_{IN2} = 302.5 MHz, each tone at –7 dBFS		85		
		f_{IN1} = 297.5 MHz, f_{IN2} = 302.5 MHz, each tone at –16 dBFS		83		
ENOB	Effective number of bits	f_{IN} = 70 MHz	10.8	11.2		Bits
		f_{IN} = 230 MHz	10.6	10.9		

Electrical Characteristics (continued)

Typical values at T_A = 25°C: minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = 400 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1 dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted.

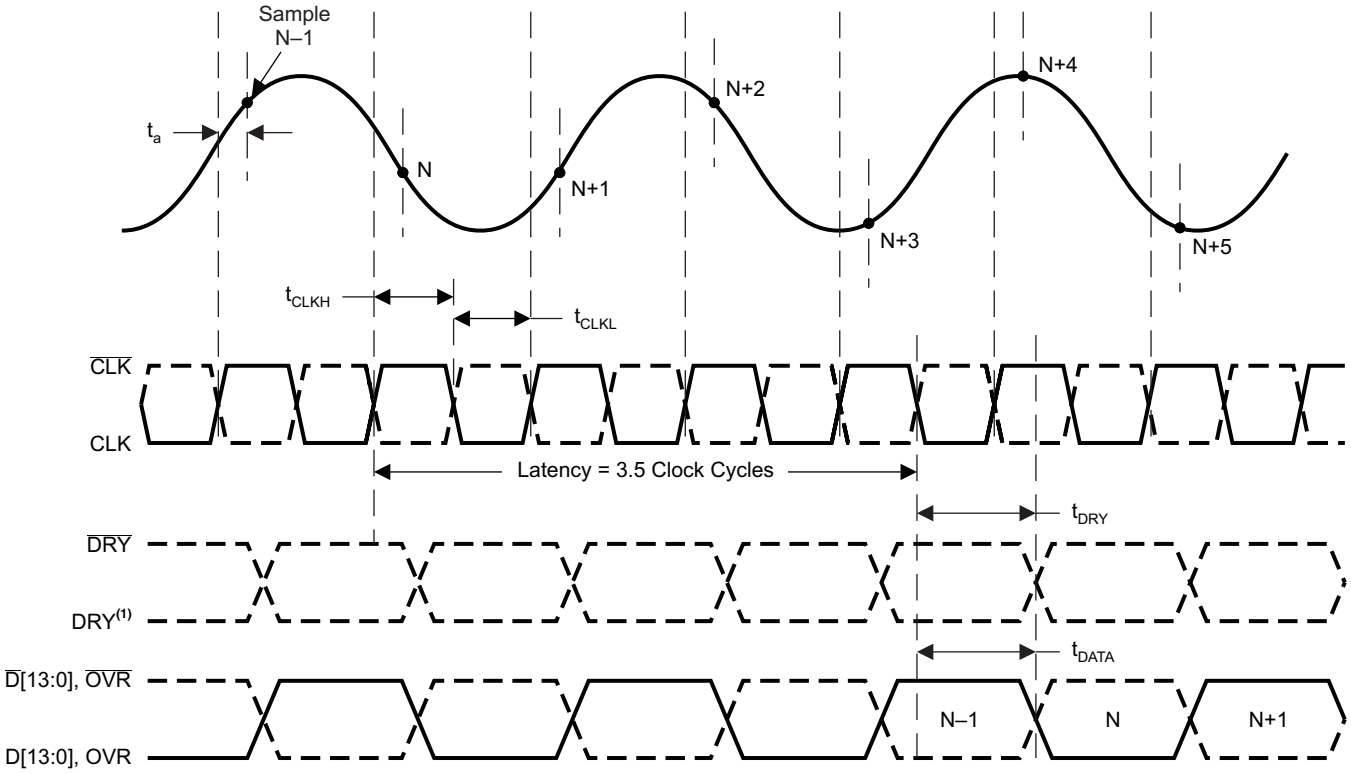
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	RMS idle-channel noise	Inputs tied to common-mode		1.8		LSB
DIGITAL OUTPUTS						
V_{OD}	Differential output voltage (±)		247	350	454	mV
V_{OC}	Common-mode output voltage		1.125		1.375	V
DIGITAL INPUTS						
V_{IH}	High level input voltage	PWD (pin 33)	2			V
V_{IL}	Low level input voltage	PWD (pin 33)			0.8	V
I_{IH}	High level input current	PWD (pin 33)			1	µA
I_{IL}	Low level input current	PWD (pin 33)	–1			µA
	Input capacitance	PWD (pin 33)		2		pF

6.6 Timing Characteristics

Typical values at T_A = 25°C: minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = 400 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, unless otherwise noted.(1)

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_a	Aperture delay			200		ps
	Aperture jitter, rms	Internal jitter of the ADC		103		fs
	Latency			3.5		cycles
t_{CLK}	Clock period		2.5		50	ns
t_{CLKH}	Clock pulse duration, high		1			ns
t_{CLKL}	Clock pulse duration, low		1			ns
t_{DRY}	CLK to DRY delay(2)	Zero crossing, 10-pF parasitic loading to GND on each output pin	1000	1400	1800	ps
t_{DATA}	CLK to DATA/OVR delay(2)	Zero crossing, 10-pF parasitic loading to GND on each output pin	800	1400	2000	ps
t_{SKEW}	DATA to DRY skew	$t_{DATA} – t_{DRY}$, 10-pF parasitic loading to GND on each output pin	–500	0	500	ps
t_{RISE}	DRY/DATA/OVR rise time	10-pF parasitic loading to GND on each output pin		500		ps
t_{FALL}	DRY/DATA/OVR fall time	10-pF parasitic loading to GND on each output pin		500		ps

(1) Timing parameters are ensured by design or characterization, but not production tested.
(2) DRY, DATA, and OVR are updated on the falling edge of CLK. The latency must be added to t_{DATA} to determine the overall propagation delay.



(1) Polarity of DRY is undetermined. For further information, see the *Digital Outputs* section.

Figure 1. Timing Diagram

6.7 Typical Characteristics

At T_A = 25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

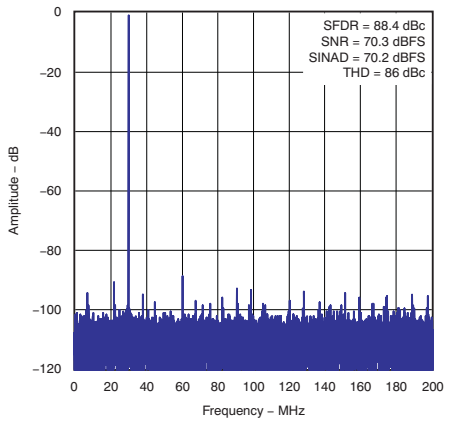


Figure 2. Spectral Performance FFT for 30 MHz Input Signal

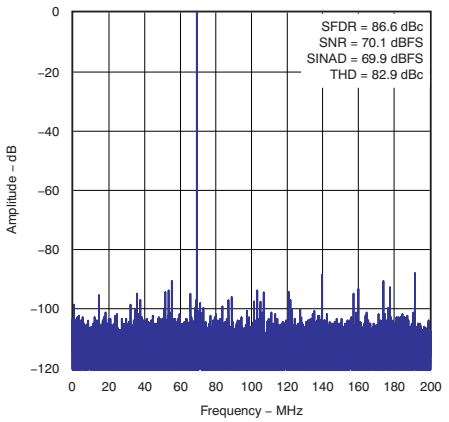


Figure 3. Spectral Performance FFT for 70 MHz Input Signal

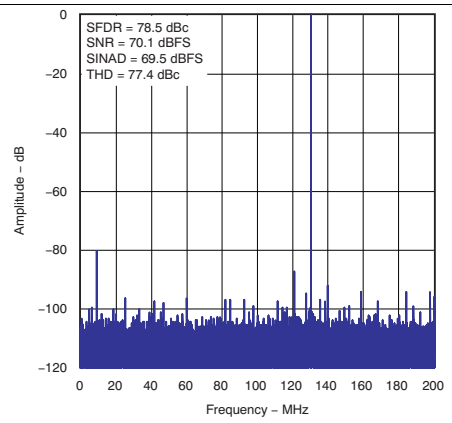


Figure 4. Spectral Performance FFT for 130 MHz Input Signal

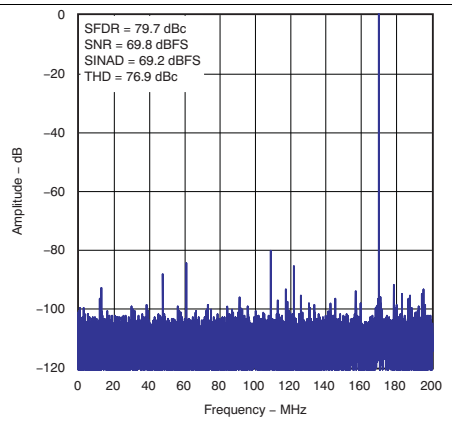


Figure 5. Spectral Performance FFT for 230 MHz Input Signal

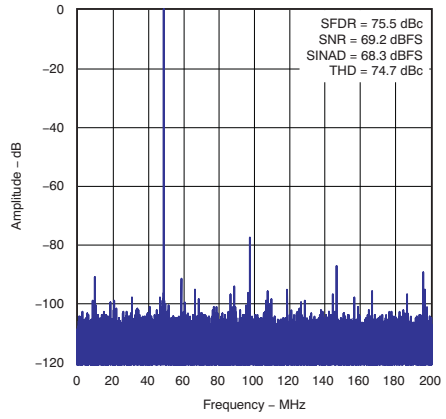


Figure 6. Spectral Performance FFT for 351 MHz Input Signal

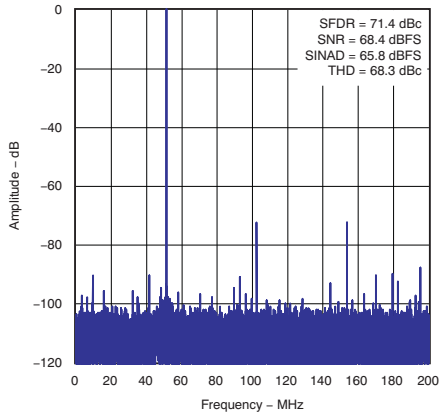


Figure 7. Spectral Performance FFT for 451 MHz Input Signal

Typical Characteristics (continued)

At T_A = 25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

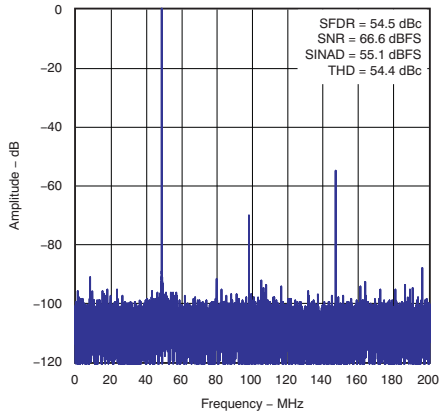


Figure 8. Spectral Performance FFT for 751 MHz Input Signal

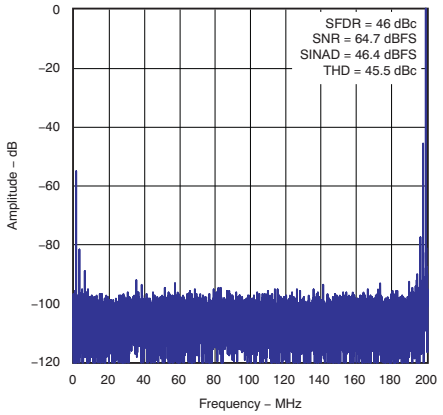


Figure 9. Spectral Performance FFT for 999 MHz Input Signal

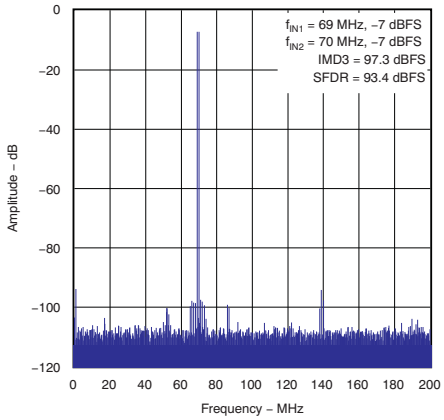


Figure 10. Two-Tone Intermodulation Distortion (FFT for 69 MHz and 70 MHz at –7 dBFS)

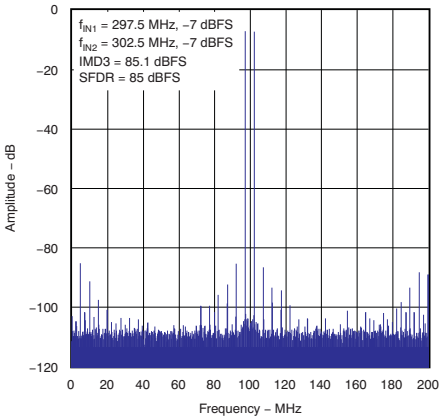


Figure 11. Two-Tone Intermodulation Distortion (FFT for 297.5 MHz and 302.5 MHz at –7 dBFS)

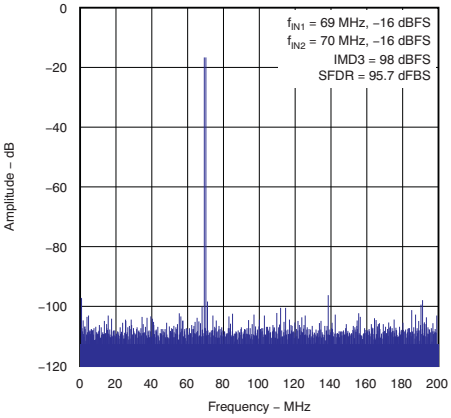


Figure 12. Two-Tone Intermodulation Distortion (FFT for 69 MHz and 70 MHz at –16 dBFS)

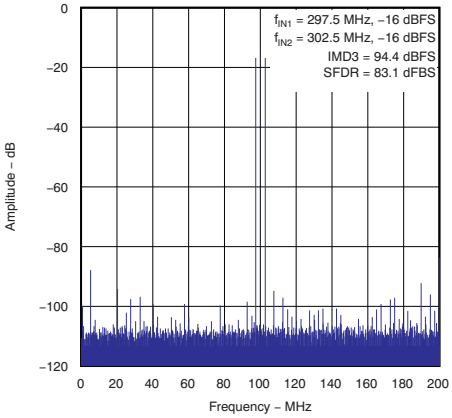


Figure 13. Two-Tone Intermodulation Distortion (FFT for 297.5 MHz and 302.5 MHz at –16 dBFS)

Typical Characteristics (continued)

At T_A = 25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

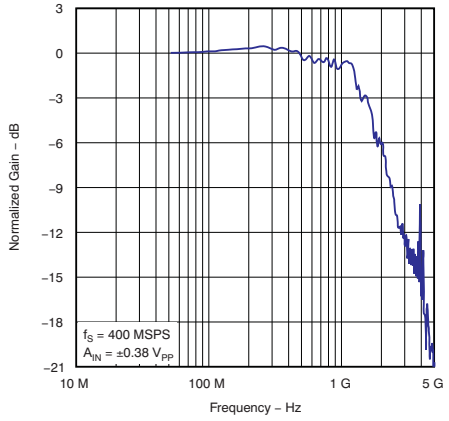


Figure 14. Normalized Gain Response vs Input Frequency

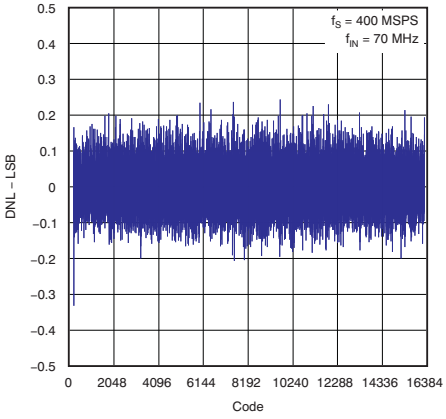


Figure 15. Differential Nonlinearity

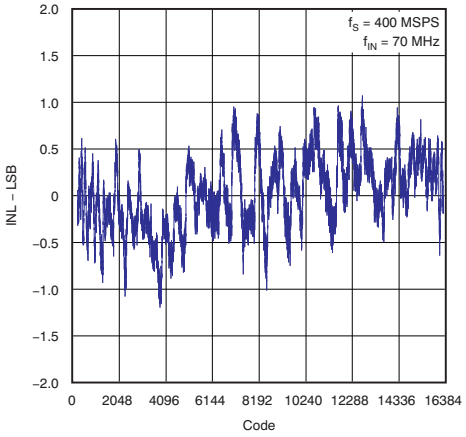


Figure 16. Integral Nonlinearity

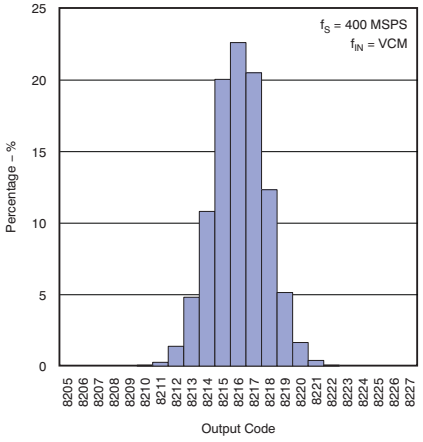


Figure 17. Noise Histogram With Inputs Shorted

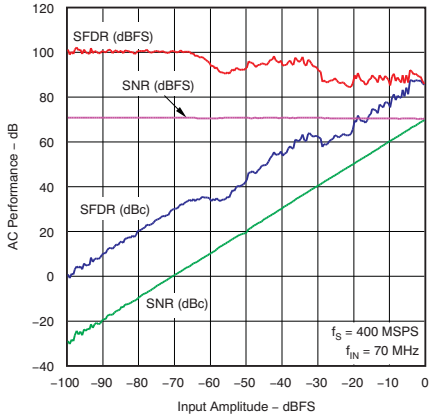


Figure 18. AC Performance vs Input Amplitude (70 MHz Input Signal)

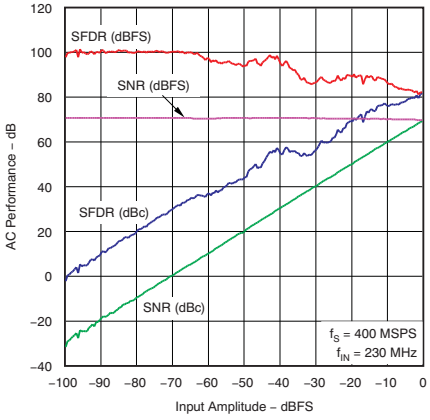


Figure 19. AC Performance vs Input Amplitude (230 MHz Input Signal)

Typical Characteristics (continued)

At T_A = 25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

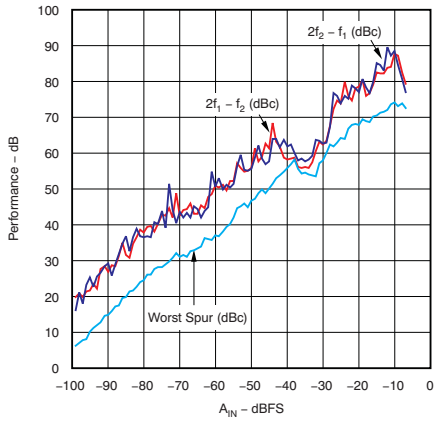


Figure 20. Two-Tone Performance vs Input Amplitude (f1 = 297.5 MHz and f2 = 302.5 MHz)

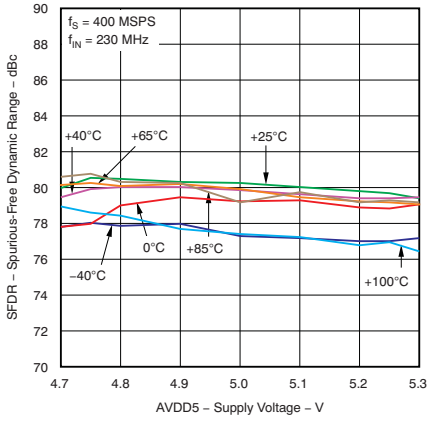


Figure 21. SFDR vs AVDD5 Over Temperature

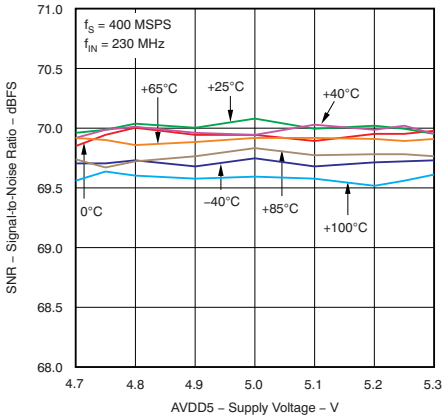


Figure 22. SNR vs AVDD5 Over Temperature

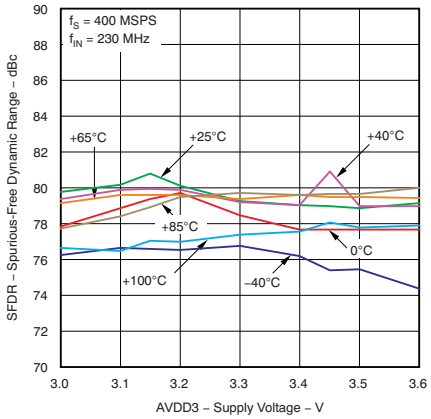


Figure 23. SFDR vs AVDD3 Over Temperature

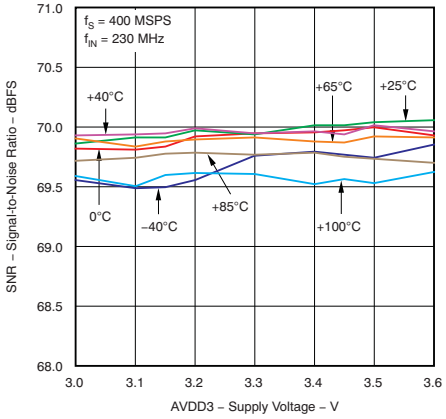


Figure 24. SNR vs AVDD3 Over Temperature

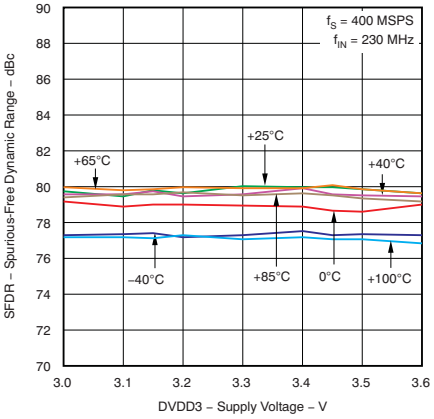


Figure 25. SFDR vs DVDD3 Over Temperature

Typical Characteristics (continued)

At T_A = 25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

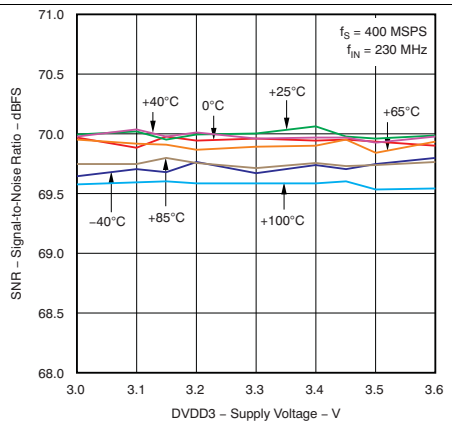


Figure 26. SNR vs DVDD3 Over Temperature

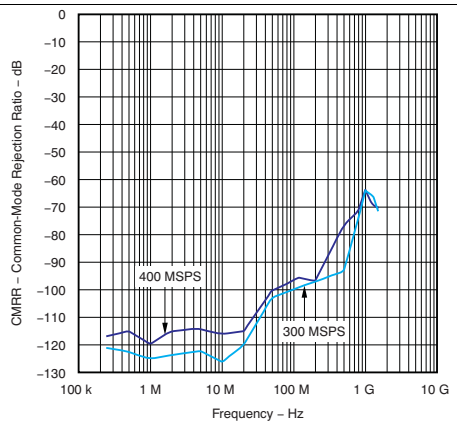


Figure 27. CMRR vs Common-Mode Input Frequency

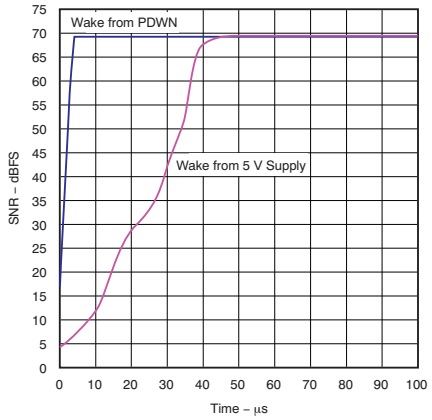


Figure 28. ADC Wakeup Time

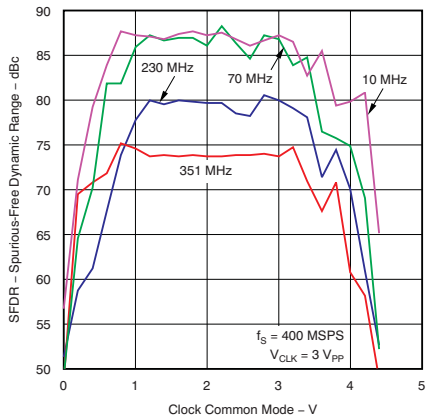


Figure 29. SFDR vs Clock Common Mode

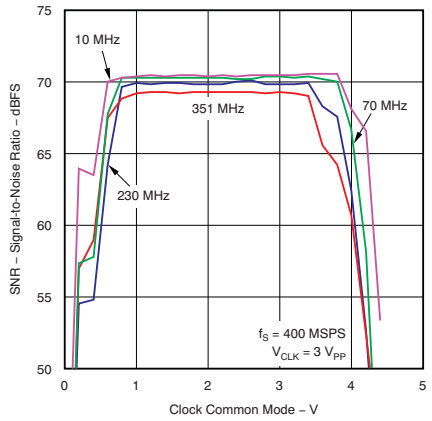


Figure 30. SNR vs Clock Common Mode

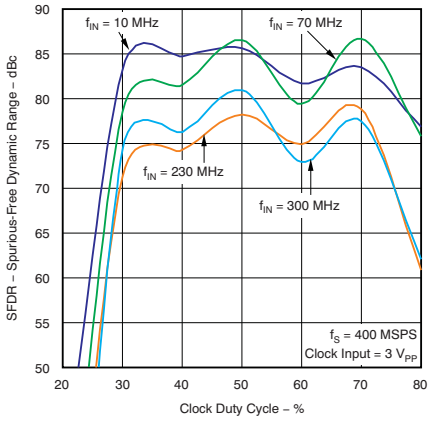


Figure 31. SFDR vs Clock Duty Cycle

Typical Characteristics (continued)

At T_A = 25°C, sampling rate = 400 MSPS, 50% clock duty cycle, 3-V_{PP} differential sinusoidal clock, analog input amplitude = –1 dBFS, AVDD5 = 5 V, AVDD3 = 3.3 V, and DVDD3 = 3.3 V, unless otherwise noted.

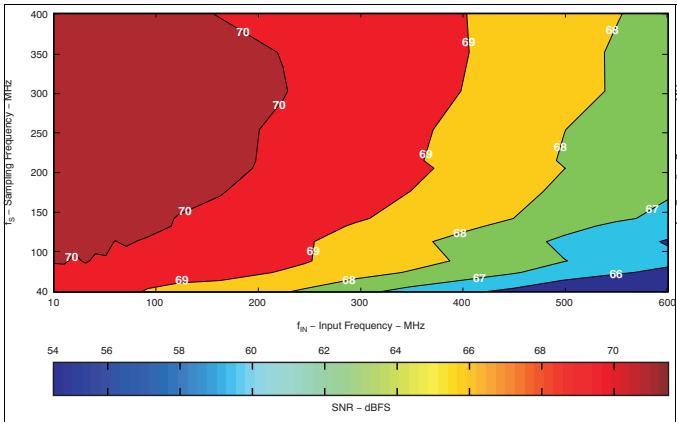


Figure 32. SNR vs Input Frequency And Sampling Frequency

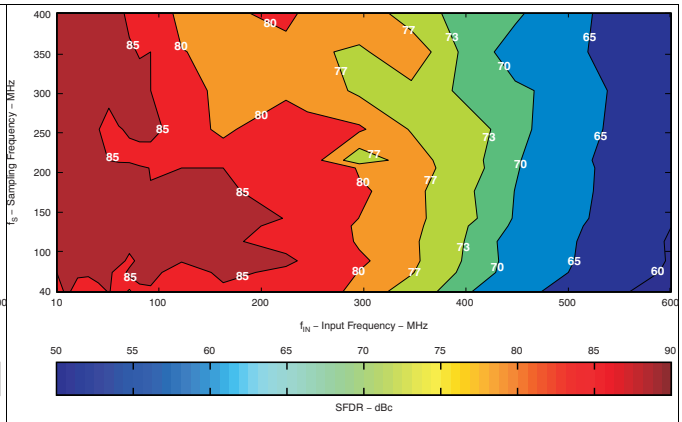


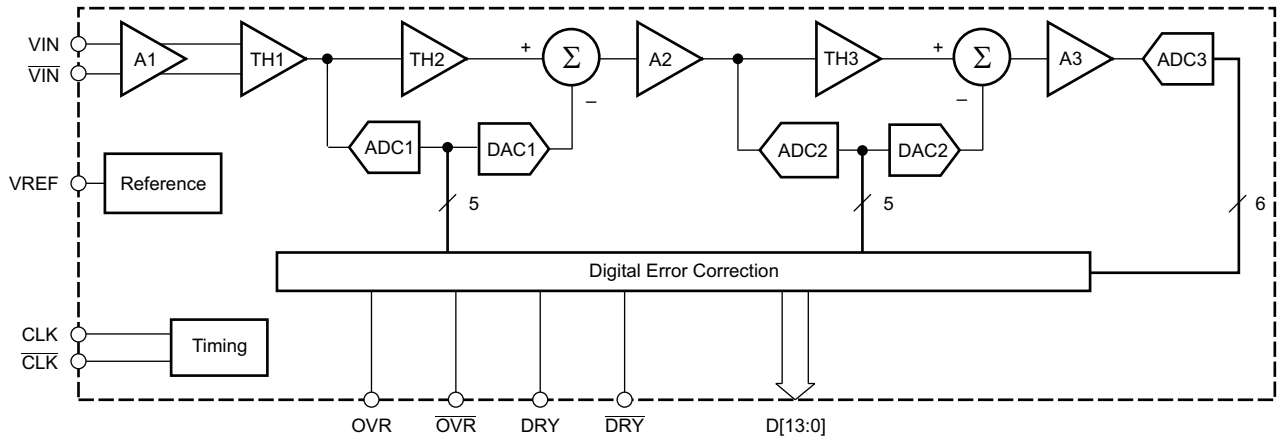
Figure 33. SFDR vs Input Frequency And Sampling Frequency

7 Detailed Description

7.1 Overview

The ADS5474 device is a 14-bit, 400-MSPS, monolithic pipeline ADC. The bipolar analog core operates from 5-V and 3.3-V supplies, while the output uses a 3.3-V supply to provide LVDS-compatible outputs. The conversion process is initiated by the rising edge of the external input clock. At that instant, the differential input signal is captured by the input track-and-hold (T&H), and the input sample is converted sequentially by a series of lower resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 3.5 clock cycles, after which the output data are available as a 14-bit parallel word, coded in offset binary format.

7.2 Functional Block Diagram



7.3 Feature Description

The analog input for the ADS5474 device consists of an analog pseudo-differential buffer followed by a bipolar transistor T&H. The analog buffer isolates the source driving the input of the ADC from any internal switching and presents a high impedance that is easy to drive at high input frequencies, compared to an ADC without a buffered input. The input common-mode is set internally through a 500-Ω resistor connected from 3.1 V to each of the inputs (common-mode is approximately 2.4 V on 12-bit and 13-bit members of this family). This configuration results in a differential input impedance of 1 kΩ.

Feature Description (continued)

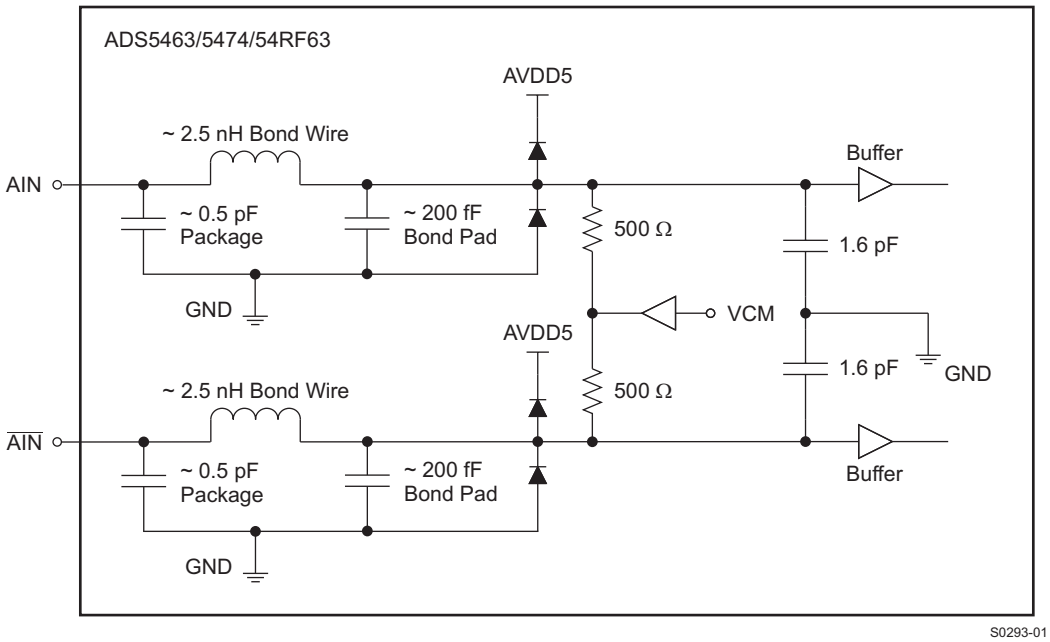


Figure 34. Analog Input Equivalent Circuit

For a full-scale differential input, each of the differential lines of the input signal (pins 16 and 17) swings symmetrically between (3.1 V + 0.55 V) and (3.1 V – 0.55 V). This range means that each input has a maximum signal swing of 1.1 V_{PP} for a total differential input signal swing of 2.2 V_{PP}. Operation below 2.2 V_{PP} is allowable, with the characteristics of performance versus input amplitude demonstrated in Figure 18 and Figure 19. For instance, for performance at 1.1 V_{PP} rather than 2.2 V_{PP}, refer to the SNR and SFDR at –6 dBFS (0 dBFS = 2.2 V_{PP}). The maximum swing is determined by the internal reference voltage generator, eliminating the need for any external circuitry for this purpose.

7.3.1 Clock Inputs

The ADS5474 device clock input can be driven with either a differential clock signal or a single-ended clock input. The characterization of the ADS5474 device is typically performed with a 3-V_{PP} differential clock, but the ADC performs well with a differential clock amplitude down to approximately 0.5 V_{PP}, as shown in Figure 37. The clock amplitude becomes more of a factor in performance as the analog input frequency increases. In low-input-frequency applications, where jitter may not be a big concern, the use of a single-ended clock could save cost and board space without much performance tradeoff. When clocked with this configuration, it is best to connect $\overline{CLK}$ to ground with a 0.01-µF capacitor, while CLK is ac-coupled with a 0.01-µF capacitor to the clock source, as shown in Figure 36.

Feature Description (continued)

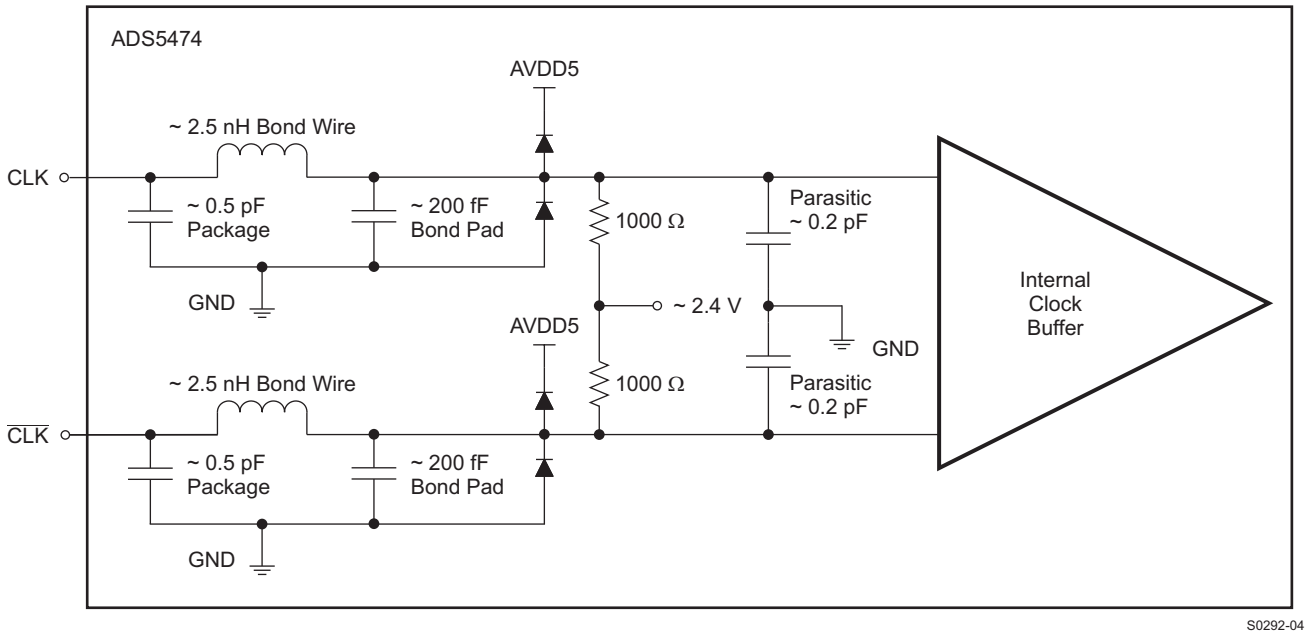


Figure 35. Clock Input Circuit

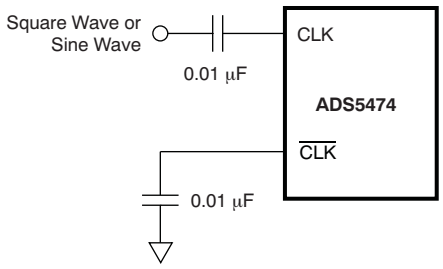


Figure 36. Single-Ended Clock

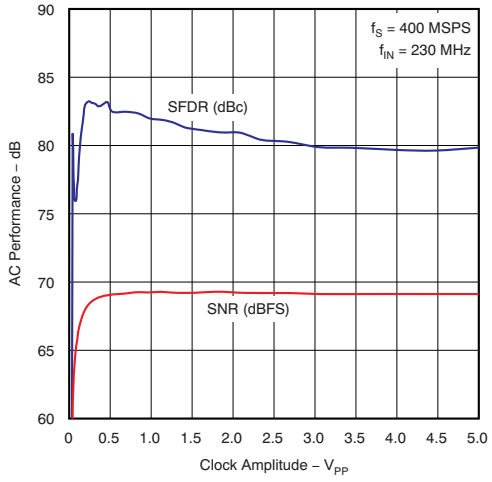


Figure 37. AC Performance vs Clock Level

7.3.2 Digital Outputs

The ADC provides 14 LVDS-compatible, offset binary data outputs (D13 to D0; D13 is the MSB and D0 is the LSB), a data-ready signal (DRY), and an over-range indicator (OVR). TI recommends using the DRY signal to capture the output data of the ADS5474 device. DRY is source-synchronous to the DATA/OVR outputs and operates at the same frequency, creating a half-rate DDR interface that updates data on both the rising and falling edges of DRY. It is recommended that the capacitive loading on the digital outputs be minimized. Higher capacitance shortens the data-valid timing window. The values given for timing (see Figure 1) were obtained with

Feature Description (continued)

a measured 10-pF parasitic board capacitance to ground on each LVDS line (or 5-pF differential parasitic capacitance). When setting the time relationship between DRY and DATA at the receiving device, it is generally recommended that setup time be maximized, but this partially depends on the setup and hold times of the device receiving the digital data (like an FPGA or Field Programmable Field Array). Since DRY and DATA are coincident, it will likely be necessary to delay either DRY or DATA such that setup time is maximized.

Referencing Figure 1, the polarity of DRY with respect to the sample N data output transition is undetermined because of the unknown startup logic level of the clock divider that generates the DRY signal (DRY is a frequency divide-by-two of CLK). Either the rising or the falling edge of DRY will be coincident with sample N and the polarity of DRY could invert when power is cycled off, on or when the power-down pin is cycled. Data capture from the transition and not the polarity of DRY is recommended, but not required. If the synchronization of multiple ADS5474 devices is required, it might be necessary to use a form of the CLKIN signal rather than DRY to capture the data.

The DRY frequency is identical on the ADS5474 and ADS5463 devices (where DRY equals ½ the CLK frequency), but different on the pin-similar ADS5444 and ADS5440 devices (where DRY equals the CLK frequency). The LVDS outputs all require an external 100-Ω load between each output pair in order to meet the expected LVDS voltage levels. For long trace lengths, it may be necessary to place a 100-Ω load on each digital output as close to the ADS5474 device as possible and another 100-Ω differential load at the end of the LVDS transmission line to provide matched impedance and avoid signal reflections. The effective load in this case reduces the LVDS voltage levels by half.

The OVR output equals a logic high when the 14-bit output word attempts to exceed either all 0s or all 1s. This flag is provided as an indicator that the analog input signal exceeded the full-scale input limit of approximately 2.2 V_{PP} (± gain error). The OVR indicator is provided for systems that use gain control to keep the analog input signal within acceptable limits.

7.4 Device Functional Modes

7.4.1 External Voltage Reference

For systems that require the analog signal gain to be adjusted or calibrated, this can be performed by using an external reference. The dependency on the signal amplitude to the value of the external reference voltage is characterized typically by Figure 38 (VREF = 2.4 V is normalized to 0 dB as this is the internal reference voltage). As can be seen in the linear fit, this equates to approximately –0.3 dB of signal adjustment per 100 mV of reference adjustment. The range of allowable variation depends on the analog input amplitude that is applied to the inputs and the desired spectral performance, as can be seen in the performance versus external reference graphs in Figure 39 and Figure 40. As the applied analog signal amplitude is reduced, more variation in the reference voltage is allowed in the positive direction (which equates to a reduction in signal amplitude), whereas an adjustment in reference voltage below the nominal 2.4 V (which equates to an increase in signal amplitude) is not recommended below approximately 2.35 V. The power consumption versus reference voltage and operating temperature should also be considered, especially at high ambient temperatures, because the lifetime of the device is affected by internal junction temperature (see Figure 48).

Device Functional Modes (continued)

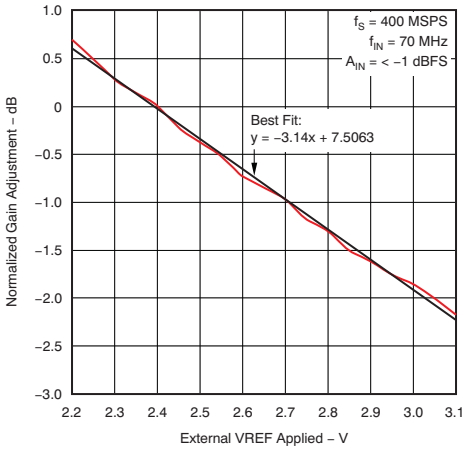


Figure 38. Signal Gain Adjustment vs External Reference (VREF)

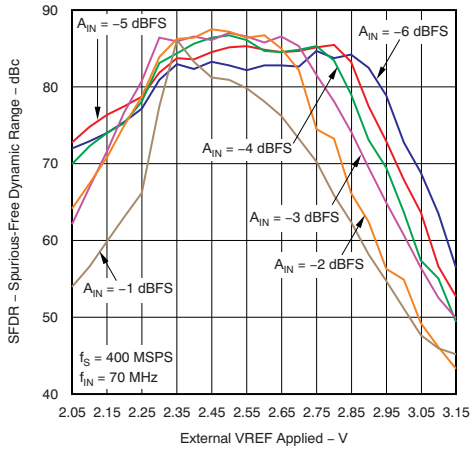


Figure 39. SFDR vs External VREF and A_{IN}

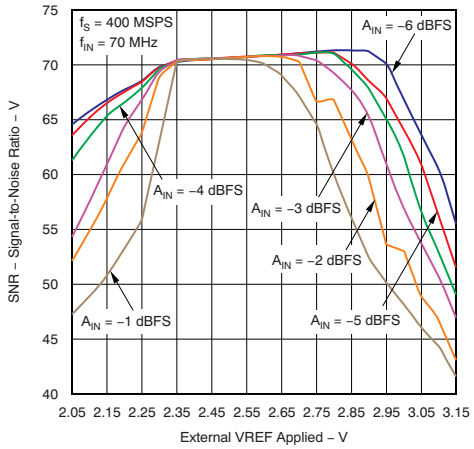


Figure 40. SNR vs External VREF and A_{IN}

For dc-coupled applications that use the VCM pin of the ADS5474 device as the common mode of the signal in the analog signal gain path prior to the ADC inputs, the information in Figure 42 is useful to consider versus the allowable common-mode range of the device that is receiving the VCM voltage, such as an operational amplifier. Because it is pin-compatible, it is important to note that the ADS5463 does not have a VCM pin and primarily uses the VREF pin to provide the common-mode voltage in dc-coupled applications. The ADS5463 (VCM = 2.4 V) and ADS5474 (VCM = 3.1 V) devices do not have the same common-mode voltage. To create a board layout that may accommodate both devices in dc-coupled applications, route VCM and VREF both to a common point that can be selected via a switch, jumper, or a 0-Ω resistor.

Device Functional Modes (continued)

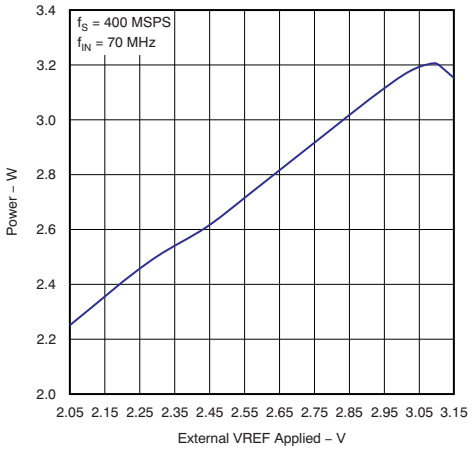


Figure 41. Total Power Consumption vs External VREF

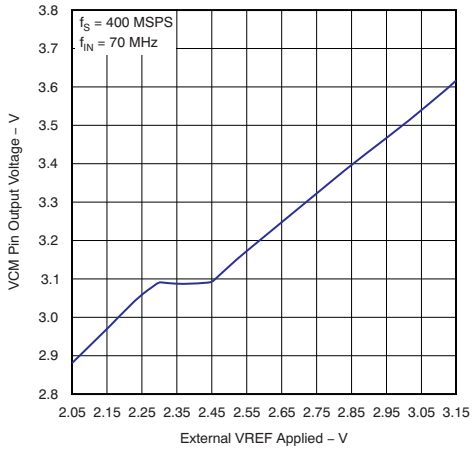


Figure 42. VCM Pin Output vs External VREF

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

In the design of any application involving a high-speed data converter, particular attention should be paid to the design of the analog input, the clocking solution, and careful layout of the clock and analog signals. The ADS5474 evaluation module (EVM) is one practical example of the design of the analog input circuit and clocking solution, as well as a practical example of good circuit board layout practices around the ADC.

8.2 Typical Applications

The analog inputs of the ADS5474 must be fully differential and biased to an appropriate common mode voltage, VCM. It is rare that the end equipment will have a signal that already meets the requisite amplitude and common mode and is fully differential. Therefore, there will be a signal conditioning circuit for the analog input. If the amplitude of the input circuit is such that no gain is needed to make full use of the full-scale range of the ADC, then a transformer coupled circuit as used on the EVM may be used with good results. The transformer coupling is inherently low-noise, and inherently AC-coupled so that the signal may be biased to VCM after the transformer coupling.

If signal gain is required, or the input bandwidth is to include the spectrum all the way down to DC such that AC coupling is not possible, then an amplifier-based signal conditioning circuit would be required. Figure 43 shows LMH3401 interfaced with ADS5474. LMH3401 is configured to have to Single-Ended input with a differential outputs follow by 1st Nyquist based low pass filter with 375-MHz bandwidth. Power supply recommendations for the amplifier are also shown in the figure below.

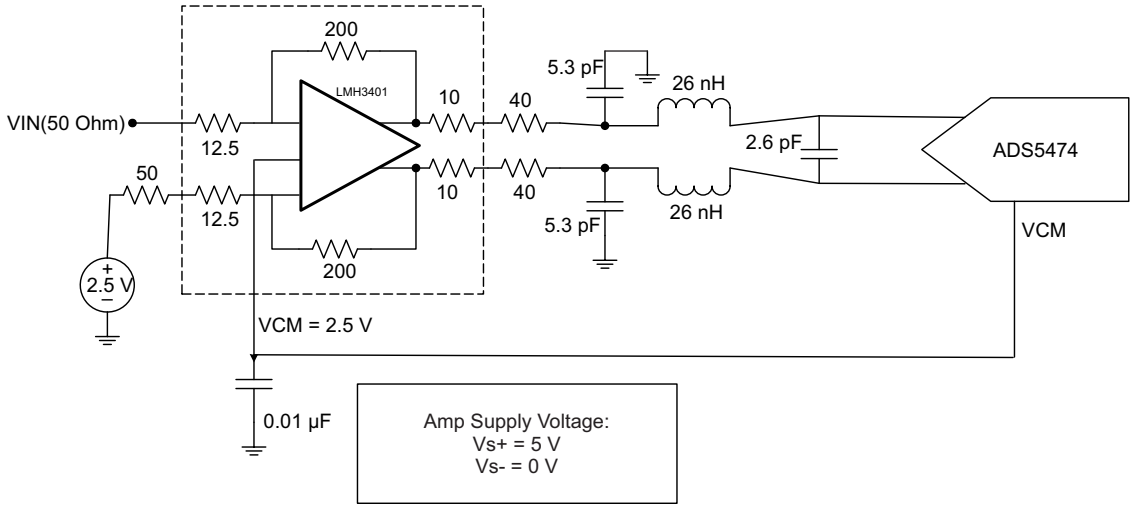


Figure 43. Application Diagram

Clocking a High Speed ADC such as the ADS5474 requires a fully differential clock signal from a clean, low-jitter clock source and driven by an appropriate clock buffer, often with LVPECL or LVDS signaling levels. The sample clock is internally biased to the desired level if the sample clock is AC coupled to the ADS5474. Figure 44 shows the typical AC coupling and termination circuit used for an AC coupled clock source.

Typical Applications (continued)

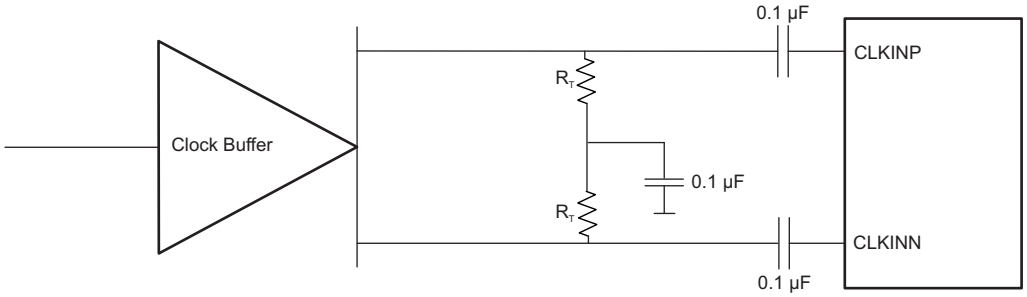


Figure 44. Recommended Differential Clock Driving Circuit

8.2.1 Design Requirements

The ADS5474 requires a fully differential analog input with a full-scale range not to exceed 2.2-V peak to peak differential, biased to a common mode voltage of 3.1 V. In addition the input circuit must provide proper transmission line termination (or proper load resistors in an amplifier-based solution) so the input of the impedance of the ADC analog inputs should be considered as well.

The ADS5474 is capable of a typical SNR of 70.1 dBFS for input frequencies of about 130 MHz, which is well under the Nyquist limit for this ADC operating at 400 Msps. The amplifier and clocking solution will have a direct impact on performance in terms of SNR, so the amplifier and clocking solution should be selected such that the SNR performance of at least 69 dBFS is preserved.

8.2.2 Detailed Design Procedure

The ADS5474 has a max sample rate of 404 MHz and an input bandwidth of approximately 1440 MHz, but an application involving the first Nyquist zone is being considered, therefore limit the frequency bandwidth here to be under 200 MHz.

8.2.2.1 Clocking Source for ADC5474

The signal to noise ratio of the ADC is limited by three different factors: the quantization noise, the thermal noise, and the total jitter of the sample clock. Quantization noise is driven by the resolution of the ADC, which is 14 bits for the ADS5474. Thermal noise is typically not noticeable in high speed pipelined converters such as the ADS5474, but may be estimated by looking at the signal to noise ratio of the ADC with very low input frequencies and using Equation 1 to solve for thermal noise. (For this estimation, we will look to the ADS5474 datasheet and take the specified SNR for the lowest frequency listed. The lowest input frequency listed for the ADS5474 is at 30 MHz, and the SNR at that frequency is 70.3 dB, so we will use 70.3 dB as our SNR limit due to thermal noise. This is just an approximation, and the lower the input frequency that has an SNR specification the better this approximation would be.) The thermal noise limits the SNR at low input frequencies while the clock jitter sets the SNR for higher input frequencies.

Quantization noise is also a limiting factor for SNR, as the theoretical maximum achievable SNR as a function of the number of bits of resolution is set by Equation 1.

$$SNR_{MAX} = 1.76 + (6.02 \times N) \quad (1)$$

where

- N = number of bits resolution

For a 14-bit ADC, the maximum SNR = 1.76 + (6.02 × 14) = 86.04 dB. This is the number that we shall enter into Equation 2 for quantization noise as we solve for total SNR for different amounts of clock jitter using Equation 2.

$$SNR_{ADC}[dBc] = -20 \times \log \sqrt{(10 - \frac{SNR_{Quantization\_Noise}}{20})^2 + (10 - \frac{SNR_{ThermalNoise}}{20})^2 + (10 - \frac{SNR_{Jitter}}{20})^2} \quad (2)$$

The SNR limitation due to sample clock jitter can be calculated using Equation 3:

$$SNR_{Jitter}[dBc] = -20 \times \log(2\pi \times f_{IN} \times t_{Jitter}) \quad (3)$$

Typical Applications (continued)

The clock jitter in Equation 3 is the total amount of clock jitter, whether the jitter source is internal to the ADC itself or external due to the clocking source. The total clock jitter (t_{Jitter}) has two components – the internal aperture jitter (103 fs for ADS5474) which is set by the noise of the clock input buffer, and the external clock jitter from the clocking source and all associated buffering of the clock signal. Total clock jitter can be calculated from the aperture jitter and the external clock jitter as in Equation 4.

$$T_{Jitter} = \sqrt{(T_{Jitter,\,Ext.CLock\_Input})^2 + (T_{Aperture\_ADC})^2} \quad (4)$$

External clock jitter can be minimized by using high quality clock sources and jitter cleaners as well as bandpass filters at the clock input while a faster clock slew rate may at times also improve the ADC aperture jitter slightly.

The ADS5474 has an internal aperture jitter of 103 fs, which is largely fixed. The SNR depending on the amount of external jitter for different input frequencies is shown in Figure 45. Often the design requirements will list a target SNR for a system, and Equation 1 through Equation 3 are then used to calculate the external clock jitter needed from the clocking solution to meet the system objectives.

Figure 45 shows that with an external clock jitter of 100 fs rms, the expected SNR of the ADS5474 would be greater than 69 dBFS at an input tone of 200 MHz, which is the Nyquist limit. Having less external clock jitter such as 35 fs rms or even 50 fs rms would result in an SNR that would exceed our design target, but at possibly the expense of a more costly clocking solution. Having external clock jitter of 150 fs rms or more would fail to meet the design target.

8.2.2.2 Amplifier Selection

The amplifier and any input filtering will have its own SNR performance, and the SNR performance of the amplifier front end will combine with the SNR of the ADC itself to yield a system SNR that is less than that of the ADC itself. System SNR can be calculated from the SNR of the amplifier conditioning circuit and the overall ADC SNR as in Equation 5. In Equation 5, the SNR of the ADC would be the value derived from the datasheet specifications and the clocking derivation presented in the previous section.

$$SNR_{System} = -20 \times \log \sqrt{(10^{\frac{-SNR_{ADC}}{20}})^2 + (10^{\frac{-SNR_{AMP+Filter}}{20}})^2} \quad (5)$$

The signal-to-noise ratio (SNR) of the amplifier and filter can be calculated from the noise specifications in the datasheet for the amplifier, the amplitude of the signal, and the bandwidth of the filter. The noise from the amplifier is band-limited by the filter and the rolloff of the filter will depend on the order of the filter, therefore the user should replace the filter rolloff with an equivalent brick-wall filter bandwidth. For example, a first order filter may be approximated by a brick-wall filter with bandwidth of 1.57 times the bandwidth of the first order filter. We will assume a first order filter for this design. The amplifier and filter noise can be calculated using Equation 6:

Typical Applications (continued)

$$SNR_{AMP+Filter} = 10 \times \log\left(\frac{V_O^{\ 2}}{E^2_{\ FILTEROUT}}\right) = 20 \times \log\left(\frac{V_O}{E_{FILTEROUT}}\right)$$

where

- $E_{FILTEROUT} = E_{NAMPOUT} \times \sqrt{ENB}$
- $E_{NAMPOUT}$ = the output noise density of the LMH3401 (3.4 nV / √Hz)
- ENB = the brick-wall equivalent noise bandwidth of the filter
- VO = the amplifier output signal. (which will be full scale input of the ADC expressed in rms) (6)

In Equation 6, the parameters of the equation can be seen to be in terms of signal amplitude in the numerator and amplifier noise in the denominator, or SNR. For the numerator, use the full scale voltage specification of the ADS5474, or 2.2 V peal to peak differential. Because Equation 6 requires the signal voltage to be in rms, convert 2.2 V p-p to 0.7766 V rms.

The noise specification for the LMH3401 is listed as 3.4 (nV/√Hz), so we will use this value to integrate the noise component from DC out to the filter cutoff, using the equivalent brick wall filter of 200 MHz × 1.57, or 314 MHz. 3.4 (nV/√Hz) × 314 MHz yields 60248 nV, or 60.25 µV.

Using 0.7766 V rms for V_O and 60.25 µV for $E_{filterout}$, the SNR of the amplifier and filter as given by Equation 6 is approximately 82.2 dB.

Taking the SNR of the ADC as 69.2 dB from Figure 45, and SNR of the amplifier and filter as 82.2 dB, Equation 5 predicts the system SNR to be 68.99 dB. In other words, the SNR of the ADC and the SNR of the front end combine as the square root of the sum of squares, and since the SNR of the amplifier front end is seen to be much greater than the SNR of the ADC in this example, the SNR of the ADC dominates Equation 5 and the system SNR is seen to be nearly the SNR of the ADC itself. We assumed our design requirement to be 69 dB, and after a clocking solution was chosen and an amplifier, filter solution was chosen we have a predicted SNR of 68.99 dB. If we deem 68.99 dB to not be close enough, or wish to have some margin in the design, then either improving the clock jitter from 100 fs to 50 fs, or replacing the first order filter with a second order filter would get the predicted system SNR above the 69-dB design requirement.

8.2.3 Application Curves

Figure 45 shows the SNR of the ADC as a function of clock jitter and input frequency for the ADS5474. This plot of curves take into account the aperture jitter of the ADC, the number of bits of resolution, and the thermal noise estimation so that the figure may be used to predict SNR for a given input frequency and external clock jitter. This figure then may be used to set the jitter requirement for the clocking solution for a given input bandwidth and given design goal for SNR.

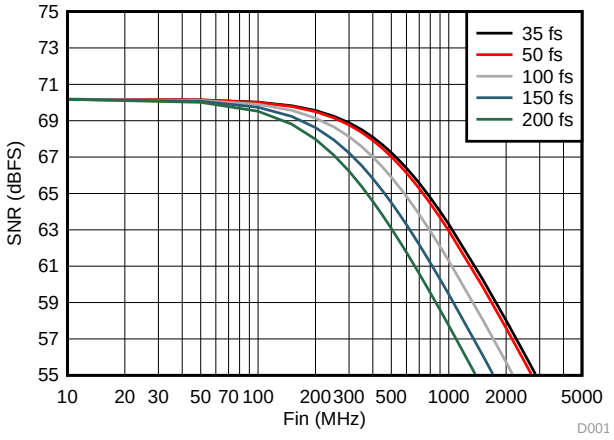


Figure 45. SNR vs Input Frequency and External Clock Jitter

9 Power Supply Recommendations

9.1 Power Supplies

The ADS5474 device uses three power supplies. For the analog portion of the design, a 5-V and 3.3-V supply (AVDD5 and AVDD3) are used, while the digital portion uses a 3.3-V supply (DVDD3). Using low-noise power supplies with adequate decoupling is recommended. Linear supplies are preferred to switched supplies, as switched supplies tend to generate more noise components that can be coupled to the ADS5474 device. However, the PSRR value and the plot shown in Figure 46 were obtained without bulk supply decoupling capacitors. When bulk (0.1-μF) decoupling capacitors are used, the board-level PSRR is much higher than the stated value for the ADC. The user may be able to supply power to the device with a less-than-ideal supply and still achieve good performance. It is not possible to make a single recommendation for every type of supply and level of decoupling for all systems. If the noise characteristics of the available supplies are understood, a study of the PSRR data for the ADS5474 device may provide the user with enough information to select noisy supplies if the performance is still acceptable within the frequency range of interest. The power consumption of the ADS5474 device does not change substantially over clock rate or input frequency as a result of the architecture and process. The DVDD3 PSRR is superior to both the AVDD5 and AVDD3, and therefore was not graphed.

Because there are two diodes connected in reverse between AVDD3 and DVDD3 internally, a power-up sequence is recommended. When there is a delay in power up between these two supplies, the one that lags could have current sinking through an internal diode before it powers up. The sink current can be large or small depending on the impedance of the external supply and could damage the device or affect the supply source. The best power up sequence is one of the following options (regardless of when AVDD5 powers up):

1) Power up both AVDD3 and DVDD3 at the same time (best scenario), OR

2) Keep the voltage difference less than 0.8 V between AVDD3 and DVDD3 during the power up (0.8 V is not a hard specification - a smaller delta between supplies is safer).

If the above sequences are not practical then the sink current from the supply must be controlled or protection added externally. The max transient current (on the order of μsec) for DVDD3 or AVDD3 pin is 500 mA to avoid potential damage to the device or reduce its lifetime.

Values for analog and clock input given in the *Absolute Maximum Ratings* are valid when the supplies are on. When the power supplies are off and the clock or analog inputs are still alive, the input voltage and current must be limited to avoid device damage. If the ADC supplies are off, the max, min continuous DC voltage is ±0.95 V and max DC current is 20 mA for each input pin (clock or analog), relative to ground.

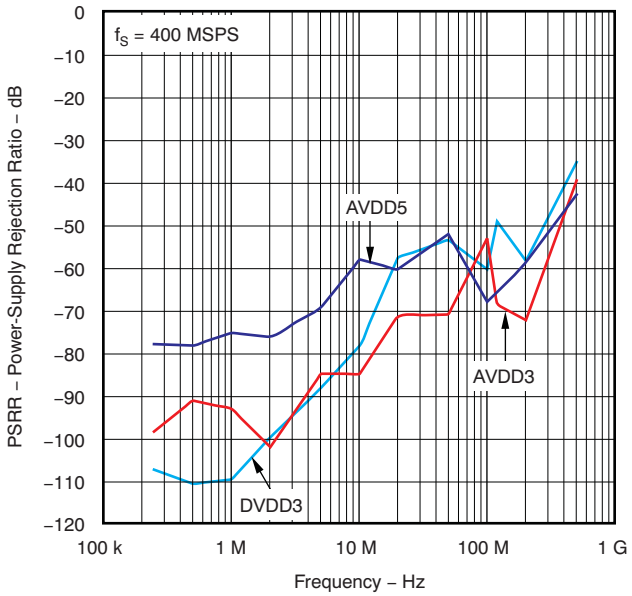


Figure 46. PSRR vs Supply Injected Frequency

10 Layout

10.1 Layout Guidelines

The evaluation board represents a good model of how to lay out the printed circuit board (PCB) to obtain the maximum performance from the ADS5474 device. Follow general design rules such as the use of multilayer boards, a single ground plane for ADC ground connections, and local decoupling ceramic chip capacitors. The analog input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. The clock signal traces should also be isolated from other signals, especially in applications such as high IF sampling where low jitter is required. Besides performance-oriented rules, care must be taken when considering the heat dissipation of the device. The thermal heatsink included on the bottom of the package should be soldered to the board as described in the *PowerPad Package* section. See the *ADS5474 EVM User Guide* (SLAU194) on the TI web site for the evaluation board schematic.

10.1.1 PowerPAD Package

The PowerPAD package is a thermally-enhanced, standard-size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard PCB assembly techniques, and can be removed and replaced using standard repair procedures.

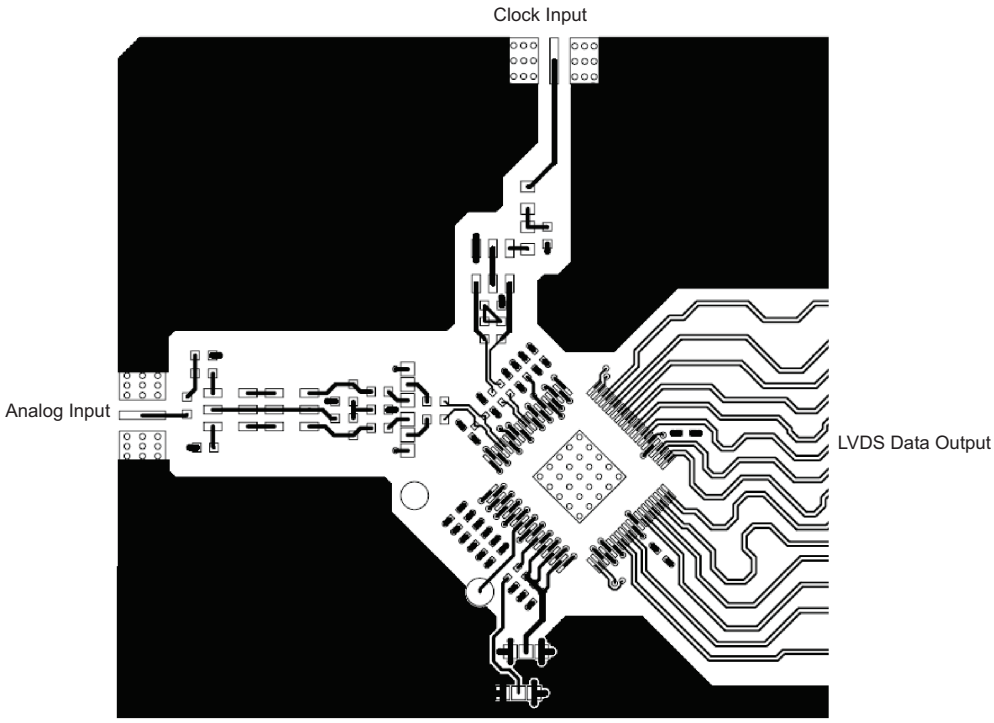
The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. This pad design provides an extremely low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heatsink.

10.1.1.1 Assembly Process

1. Prepare the PCB top-side etch pattern including etch for the leads as well as the thermal pad as illustrated in the Mechanical Data section (at the end of this data sheet).
2. Place a 6 × 6 array of thermal vias in the thermal pad area. These holes should be 13 mils (0.013 in or 0.3302 mm) in diameter. The small size prevents wicking of the solder through the holes.
3. It is recommended to place a small number of 25-mil (0.025-in or 0.635-mm) diameter holes under the package, but outside the thermal pad area, to provide an additional heat path.
4. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
5. Do not use the typical web or spoke via-connection pattern when connecting the thermal vias to the ground plane. The spoke pattern increases the thermal resistance to the ground plane.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area.
7. Cover the entire bottom side of the PowerPAD vias to prevent solder wicking.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

For more detailed information regarding the PowerPAD package and its thermal properties, see either the *PowerPAD Made Easy* application brief (SLMA004) or the *PowerPAD Thermally Enhanced Package* application report (SLMA002), both available for download at www.ti.com.

10.2 Layout Example



*Solid Black is top layer ground fill

Figure 47. ADS5474 Board Layout

10.3 Thermal Considerations

It is important for applications that anticipate running continuously for long periods of time near the maximum-rated ambient temperature of 85°C to consider the data shown in Figure 48. Referring to the *Thermal Information* table, the worst-case operating condition with no airflow has a thermal rise of 23.7°C/W. At approximately 2.5 W of normal power dissipation, at a maximum ambient of 85°C with no airflow, the junction temperature of the ADS5474 device reaches approximately 85°C + (23.7°C/W × 2.5 W) = +144°C. Being even more conservative and accounting for the maximum possible power dissipation that is ensured (2.797 W), the junction temperature becomes nearly 150°C. As Figure 48 shows, this performance limits the expected lifetime of the ADS5474 device. Operation at 85°C continuously can require airflow or an additional heatsink in order to decrease the internal junction temperature and increase the expected lifetime (because of electromigration failures). An airflow of 250 LFM (linear feet per minute) reduces the thermal resistance to 16.4°C/W and, therefore, the maximum junction temperature to 131°C, assuming a worst-case of 2.797 W and 85°C ambient.

The ADS5474 device performance over temperature is quite good and can be seen starting in Figure 21. Though the typical plots show good performance at 100°C, the device is only rated from –40°C to 85°C. For continuous operation at temperatures near or above the maximum, the expected primary negative effect is a shorter device lifetime because of the electromigration failures at high junction temperatures. The maximum recommended continuous junction temperature is 150°C.

Thermal Considerations (continued)

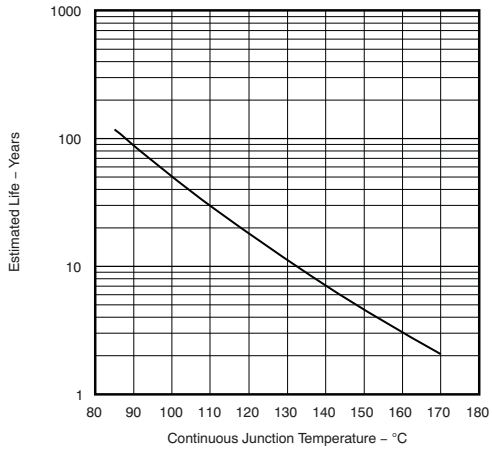


Figure 48. Operating Life Derating Chart, Electromigration Fail Mode

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Analog Bandwidth The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter) The sample-to-sample variation in aperture delay.

Clock Pulse Duration/Duty Cycle The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse duration) to the period of the clock signal, expressed as a percentage.

Differential Nonlinearity (DNL) An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Common-Mode Rejection Ratio (CMRR) CMRR measures the ability to reject signals that are presented to both analog inputs simultaneously. The injected common-mode frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the CMRR in dB.

Effective Number of Bits (ENOB) ENOB is a measure in units of bits of converter performance as compared to the theoretical limit based on quantization noise:

$$ENOB = (SINAD - 1.76)/6.02 \quad (7)$$

Gain Error Gain error is the deviation of the ADC actual input full-scale range from its ideal value, given as a percentage of the ideal input full-scale range.

Integral Nonlinearity (INL) INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best-fit line, measured in units of LSB.

Offset Error Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Power-Supply Rejection Ratio (PSRR) PSRR is a measure of the ability to reject frequencies present on the power supply. The injected frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the PSRR in dB. The measurement calibrates out the benefit of the board supply decoupling capacitors.

Signal-to-Noise Ratio (SNR) SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and in the first five harmonics. SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

$$SNR = 10\log_{10}\frac{P_S}{P_N} \quad (8)$$

Signal-to-Noise and Distortion (SINAD) SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc. SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

$$SINAD = 10\log_{10}\frac{P_S}{P_N + P_D} \quad (9)$$

Temperature Drift Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at T_{MIN} or T_{MAX}. It is computed as the maximum variation the parameters over the whole temperature range divided by $T_{MIN} – T_{MAX}$.

Total Harmonic Distortion (THD) THD is the ratio of the power of the fundamental (P_S) to the power of the first

Device Support (continued)

five harmonics (P_D).THD is typically given in units of dBc (dB to carrier).

$$THD = 10\log_{10}\frac{P_S}{P_D} \quad (10)$$

Two-Tone Intermodulation Distortion (IMD3) IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$). IMD3 is given in units of either dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Clocking High Speed Data Converters*
- *PowerPAD Thermally Enhanced Package*
- *PowerPAD Made Easy*
- *ADS5474 EVM User Guide*
- *ADS5463 12-bit, 500 MSPS Analog-to-Digital Converter with Buffered Input*
- *ADS5440 13-Bit 210 MSPS Analog-to-Digital Converter*
- *ADS5444 13-Bit 250 MSPS Analog-to-Digital Converter*
- *LMK04808 IBIS Model*
- *LMH3401 7-GHz, Ultra-Wideband, Fixed-Gain, Fully-Differential Amplifier*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5474IPFP	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS5474I	Samples
ADS5474IPFPR	ACTIVE	HTQFP	PFP	80	1000	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS5474I	Samples
ADS5474IPFPRG4	ACTIVE	HTQFP	PFP	80	1000	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS5474I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

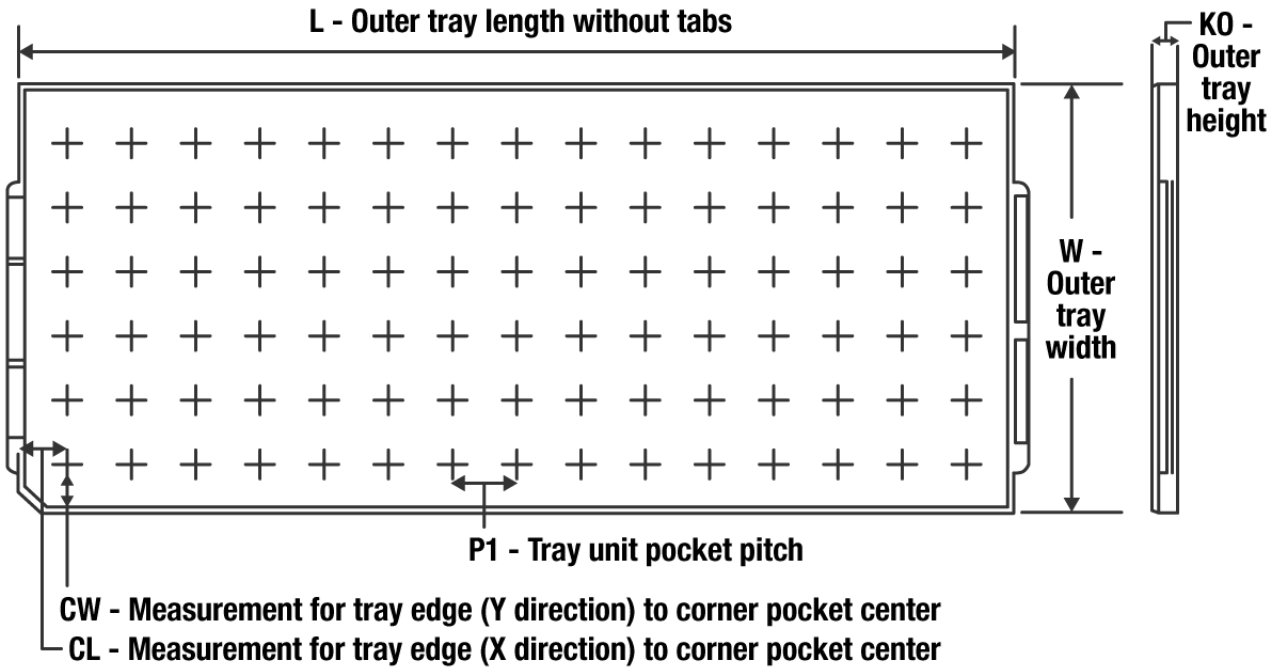
OTHER QUALIFIED VERSIONS OF ADS5474 :

- Space: ADS5474-SP

NOTE: Qualified Version Definitions:

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TRAY

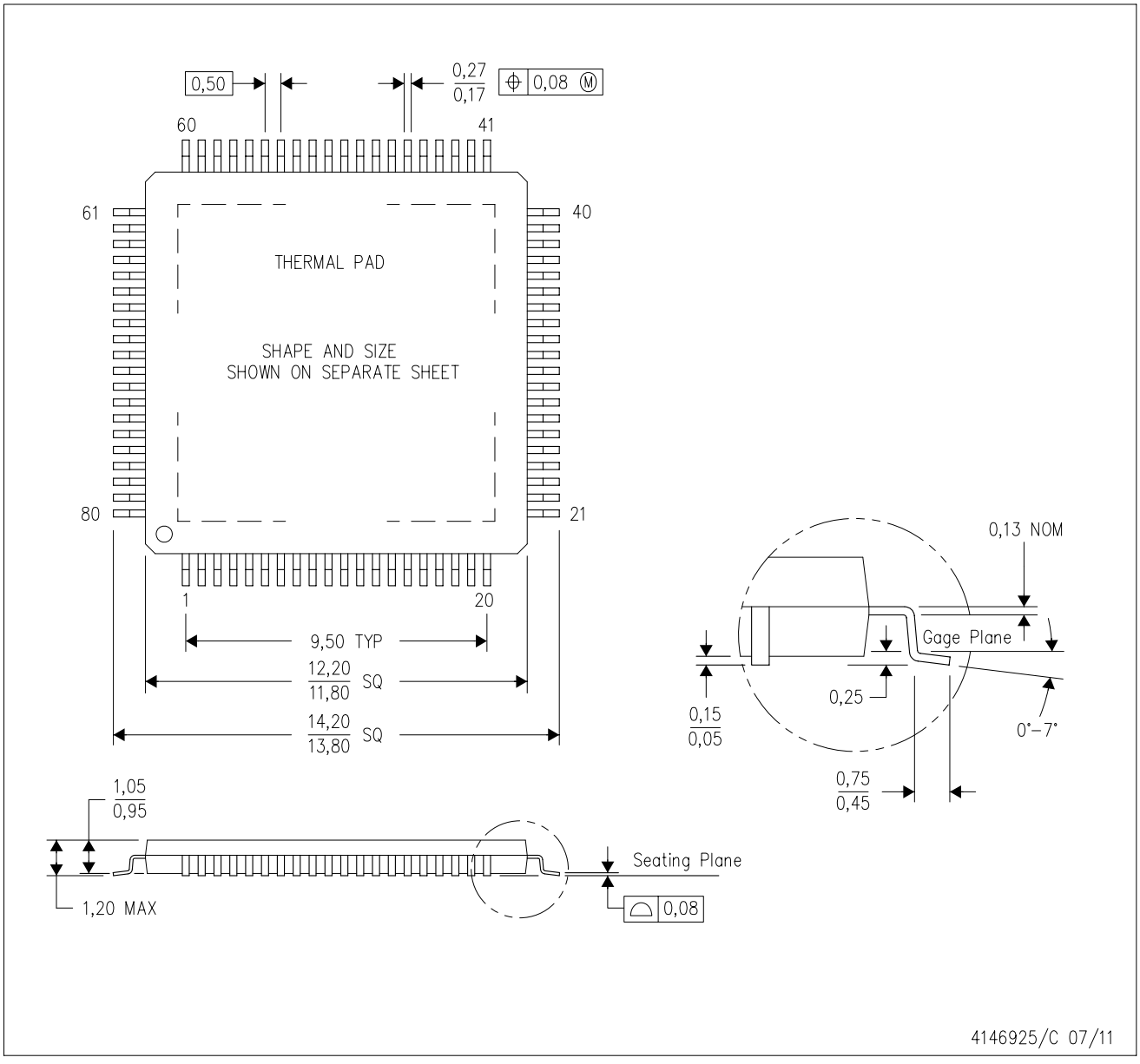


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS5474IPFP	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

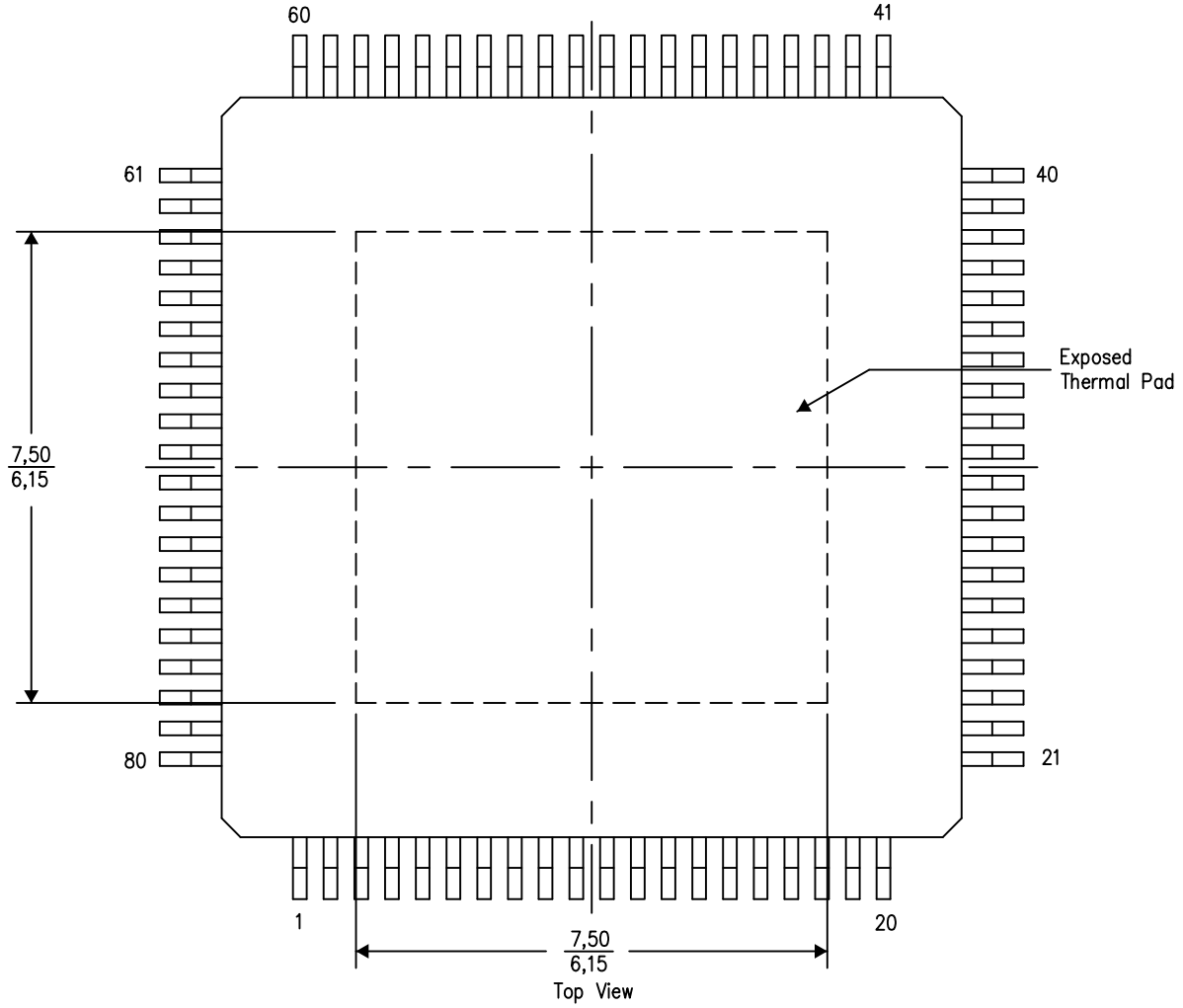
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



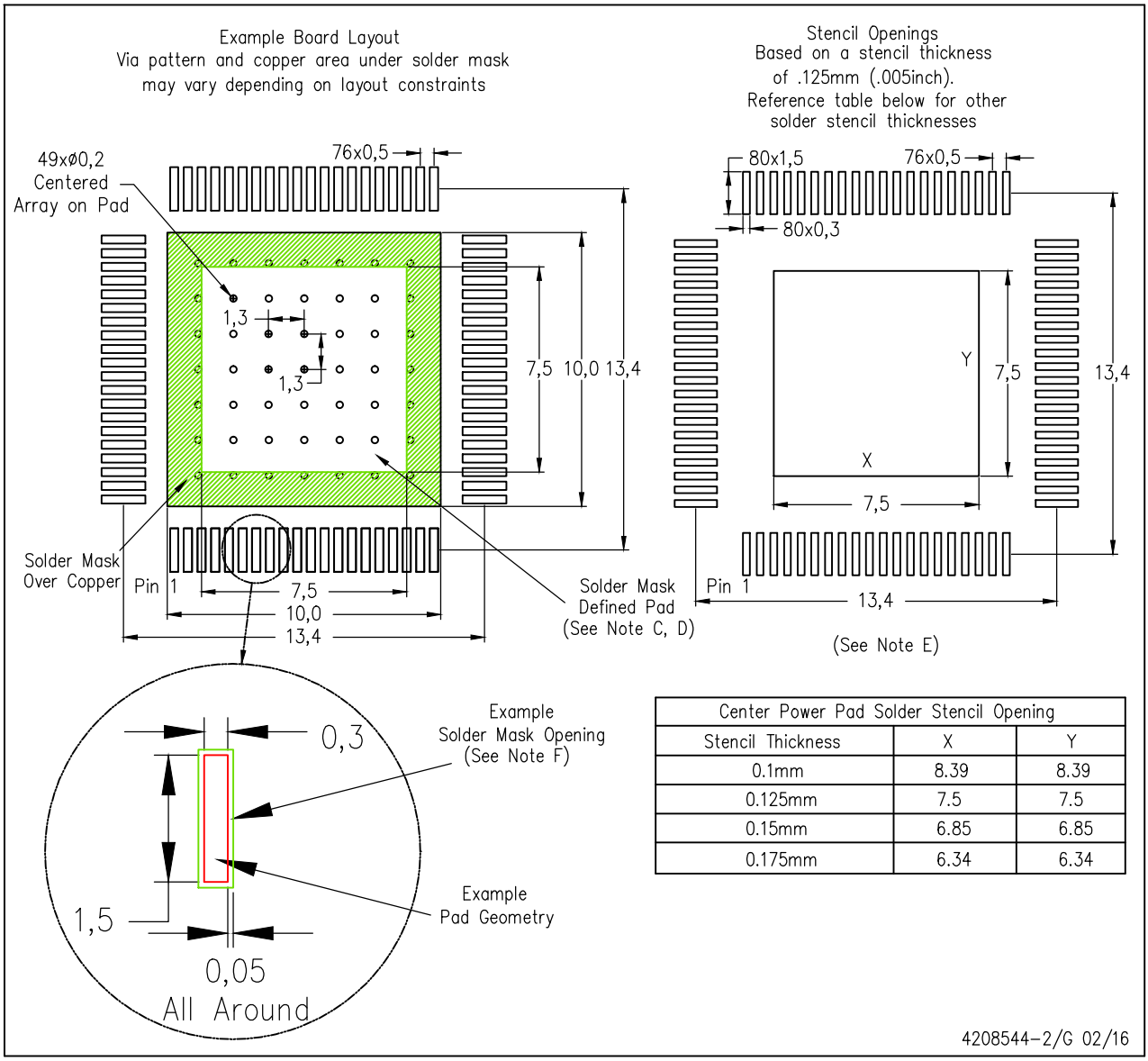
Exposed Thermal Pad Dimensions

4206327–2/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	8.39	8.39
0.125mm	7.5	7.5
0.15mm	6.85	6.85
0.175mm	6.34	6.34

PowerPAD is a trademark of Texas Instruments.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265