

Reference Design:

**HFRD-30.1**

Rev. 2; 11/08

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**REFERENCE DESIGN**  
**SFP+ Host Board**

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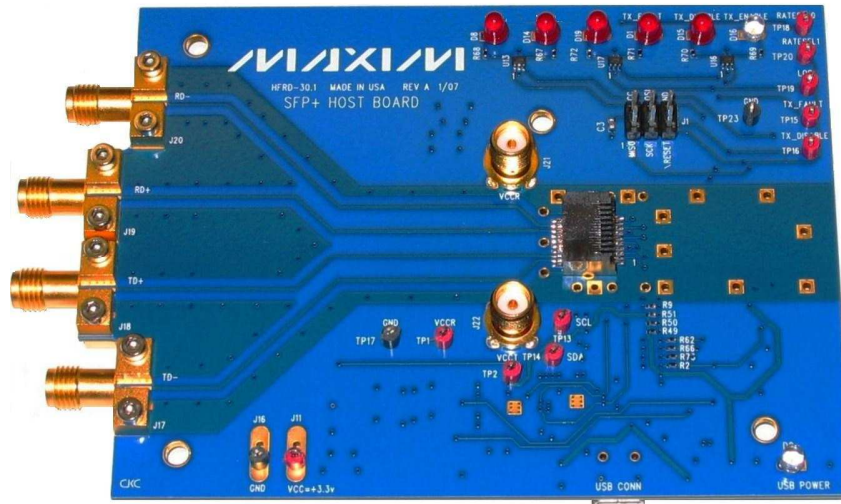
## Reference Design: SFP+ Host Board

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### 1 Overview

High-Frequency Reference Design (HFRD-30.1) is a high-speed, Small Form Factor Pluggable (SFP+) host board designed for evaluating SFP and SFP+ modules that operate at data rates up to 12Gbps. The host board can be used to test a variety of different modules, and includes additional features for testing, monitoring, and programming Maxim SFP+ reference design boards.



#### 1.1 Features

- SFP+ MSA Compatible
- GUI Interface with USB Connection
- High-Quality Low-Loss PCB Material and SMA Connectors
- On-Board Voltage and Current Monitoring
- Schematics and Bill of Materials Provided
- Gerber Files Available

### 2 Obtaining Additional Information

Limited quantities of the SFP+ host board (HFRD-30.1) are available. For more information about this reference design or to obtain a board, please email your request to: <https://support.maxim-ic.com/>.

### 3 Reference Design Details

HFRD-30.1 provides microstrip transmission lines and SMA connectors for transmitted and received data. Supply current monitors, voltage monitors, and digital I/O control/monitoring are provided through the graphical user interface (GUI) (Figure 1). Signal connections from the host board to the module board are made through a 20-pin SFP connector.

HFRD-30.1 comes complete with a Windows® system-based GUI. The GUI communicates to the board through an easy-to-use USB connection. Through the software, the user can monitor and change all of the critical parameters of HFRD-30.1. Diagnostic information can also be read from an SFP/SFP+ module through an I<sup>2</sup>C-compatible interface.

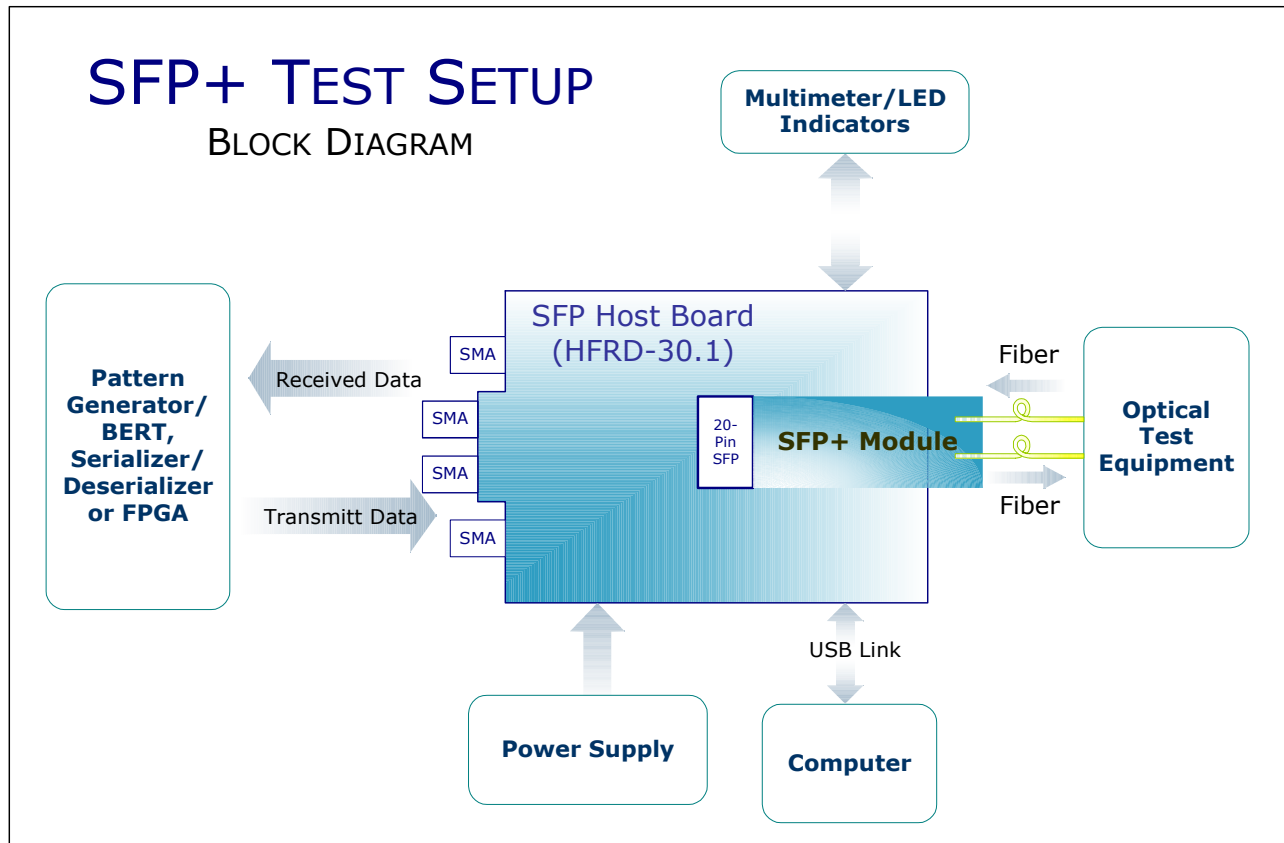


Figure 1. SFP+ test setup (block diagram).

## 4 Application Information

### 4.1 The GUI Evaluation Software

The GUI evaluation software is available at:

[http://www.maxim-integrated.com/products/fiber/reference\\_designs.cfm](http://www.maxim-integrated.com/products/fiber/reference_designs.cfm)

It is also included on CD with each evaluation board. Please check the website regularly for updates.

#### 4.1.1 Software Requirements

The evaluation software is designed to operate on Microsoft® Windows 2000 or Windows XP operating systems. The software can also be used on Windows 98. In the latter case, unstable software operation can occur if the USB cable is unplugged without first stopping the device in Windows.

#### 4.1.2 Software Installation

To install the software, simply download the file ([http://www.maxim-integrated.com/products/fiber/reference\\_designs.cfm](http://www.maxim-integrated.com/products/fiber/reference_designs.cfm)) and run it on your computer or run the Setup.exe file from the CD ROM provided. The evaluation software was built on the Microsoft .NET platform. If the current version of this platform is not already installed on your computer, the evaluation software will need an Internet connection to download the platform components and complete the installation.

*Windows and Microsoft are registered trademarks of Microsoft Corporation in the United States and other countries.*

### 4.1.3 Software Usage

Figures 2 through 3 are screen shots of the GUI that highlight various reference-design features. A brief explanation of the features is listed below each figure.

## 4.2 Layout Considerations

Single-ended transmission lines are designed on the HFRD-30.1 host board. Changing the PCB layer profile (see Section 11) can affect the impedance of these transmission lines and the performance of the reference design. If the layer profile is changed, the transmission line dimensions should be recalculated.

## 5 Evaluation Quick Start

### 5.1 Evaluation Notice

The HFRD-30.1 reference design has DC-coupled I/Os (AC-coupling should be provided inside the module). Care should be taken to ensure that the module is correctly connected to the host board and that all signal levels are within the proper range (differential swing, optical input/output power, etc.). Failure to do so can damage the test equipment or the module.

Precautions must also be taken to ensure safe operation when using a device with a laser diode. Laser light emissions can be harmful and can cause eye damage. Maxim assumes no responsibility for harm, injury, or test-equipment damage as a result of the use of this reference design.

### 5.2 Evaluation Setup

Follow these steps to evaluate an SFP/SFP+ module using the HFRD-30.1 host board:

1. Install the user software as indicated in Section 4.1.2.
2. Connect HFRD-30.1 to the computer using the USB cable provided. When the cable is inserted, D2 (USB\_PWR) should be illuminated. Wait to start the software until step 8 below. Through all of the proceeding steps, assume that laser light could be emitted from the laser diode. Handle the fiber and module with care to avoid eye or equipment damage.
3. Connect the SFP/SFP+ module into the HFRD-30.1 SFP+ Host Board. Ensure that the module is oriented correctly.
4. Clean and inspect the LC fiber patch cords and connect them to the module's Tx and Rx interfaces.

5. Connect the Tx fiber to an optical attenuator and/or optical-to-electrical converter. Use an optical attenuator, if needed, to ensure that the power level is within the safe operating limits of the test equipment.
6. Connect the Rx fiber to an appropriate optical source (power, wavelength, data rate, etc.).
7. Apply a +3.3V supply to J11 (+3.3V) and J16 (GND). Set the current limit to 300mA and turn the supply on.
8. Run the HFRD-30.1 software from the Windows operating system start menu:
  - start
  - All Programs
  - Maxim Integrated Products
  - HFRD-30.1 SFP+...
9. When the software loads, press **Initialize** (Figure 2). If everything is connected correctly, a screen similar to that shown in Figure 3 should appear. Wait to enable the driver until the remaining connections are made.

10. To complete the setup, review the module documentation carefully, noting any connections to the test equipment. Ensure that there is no DC voltage present on center conductor of the SMA connectors (J20, J19, J18, or J17) that would damage the test equipment. Make the appropriate electrical connections to the test equipment by using the module's recommended operational conditions. If assistance is required, please email questions to:

<https://support.maxim-ic.com/>.

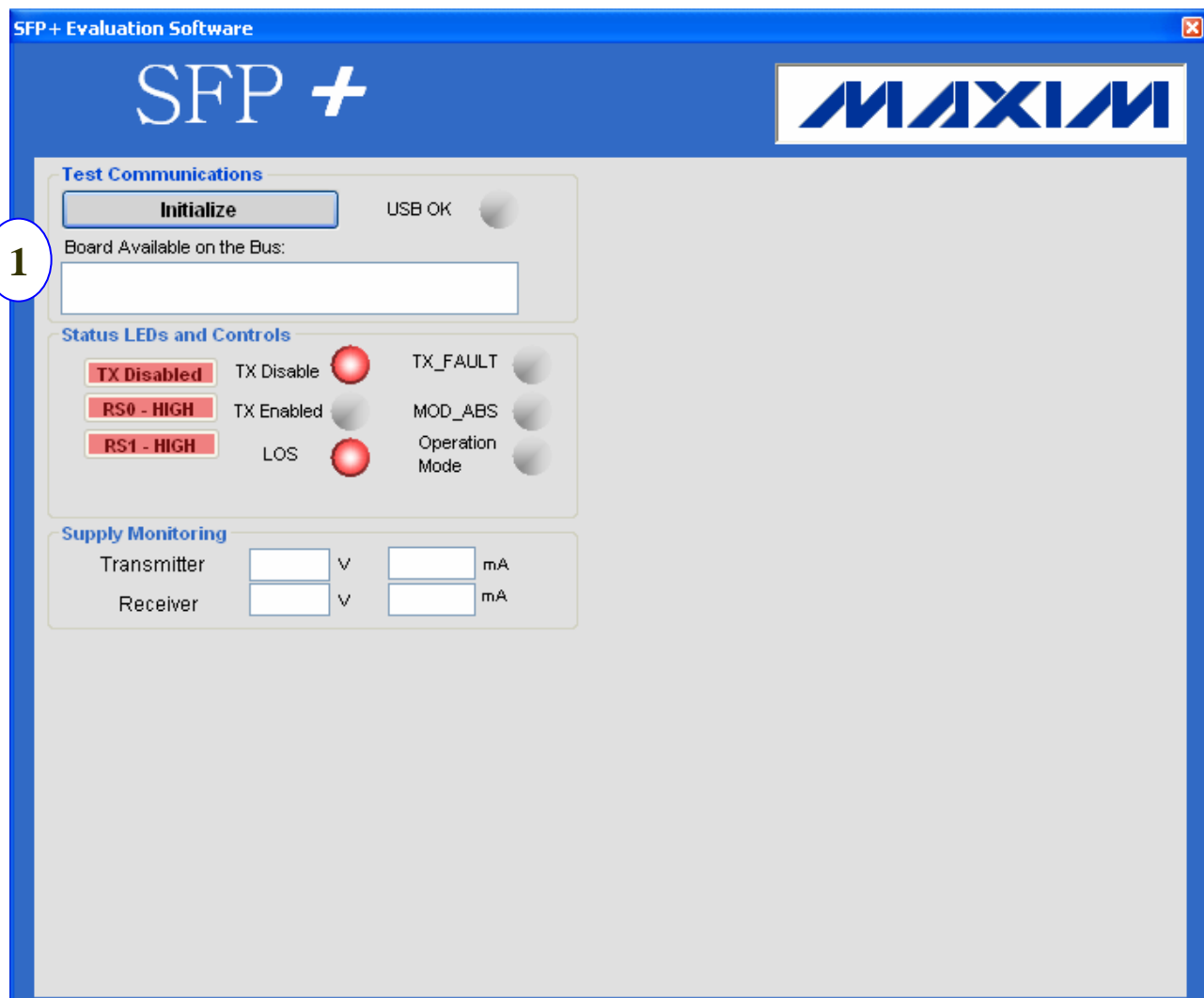


Figure 2. Initial screen.

1. **Initialize** the Test Communication: Pressing this button resets the GUI interface and initializes a test sequence to determine if the HFRD-30.1 is connected to the computer. The software then scans the I<sup>2</sup>C bus to determine if any I<sup>2</sup>C-addressable modules are connected into the HFRD-30.1 board.

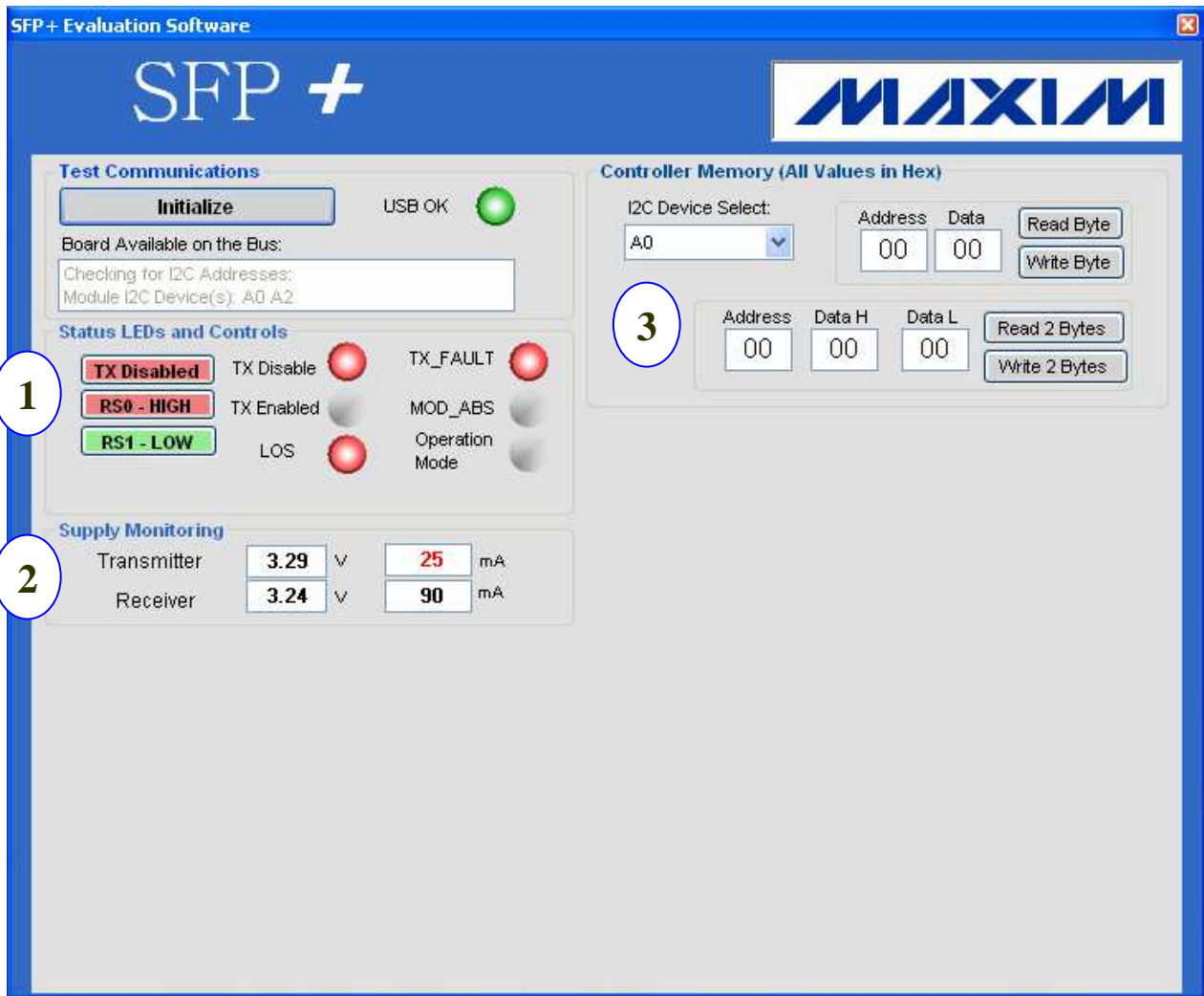


Figure 3. GUI overview.

1. **Status LEDs and Controls:** Pressing “TX Enabled” or “TX Disable” enables or disables the transmitter. Pressing “RS0...” or “RS1...” will toggle the output high or low. **Note:** RS1 can only be toggled when evaluating SFP+ modules and will always be low when evaluating standard SFP modules.
2. **Supply Monitoring:** This section displays the supply voltage and current for the transmitter and receiver section of the SFP/SFP+ module.
3. **Controller Memory:** This section allows the user to read and write from any devices in the module that are connected to the I<sup>2</sup>C bus.

## 6 I/O and Control Description

Component	Name	Function
J1		ISP connector used only for specific Maxim SFP+ reference designs: Pin 1 → MISO Pin 2 → V <sub>CC</sub> (+3.3V) Pin 3 → SCK Pin 4 → MOSI Pin 5 → RESET Pin 6 → GND
J11	+3.3V	Power supply, +3.3V input
J13		SFP Module Connector (See Section 7.)
J16	GND	Power-supply ground input
J17	TD-	Transmitted data inverted input, DC-coupled from SMA to SFP connector
J18	TD+	Transmitted data noninverted input, DC-coupled from SMA to SFP connector
J19	RD+	Received data noninverted output, DC-coupled from SMA to SFP connector
J20	RD-	Received data inverted output, DC-coupled from SMA to SFP connector
J21	VCCR	SMA connector provided for external power-supply noise injection into the receiver power supply. Can also be used for external VCCR supply monitoring.
J22	VCCT	SMA connector provided for external power-supply noise injection into the transmitter power supply. Can also be used for external VCCT supply monitoring.
D1	TX_FAULT	LED illuminates when a transmitter fault condition has occurred.
D2	USB_PWR	LED illuminates when the host board (HFRD-30.1) is connected to a computer through a USB cable.
D8	MOD_ABS	LED illuminates when the SFP/SFP+ module is absent.
D14	PROG_MODE	LED illuminates when the host board is in normal operational mode. The LED is not illuminated when it is in ISP programming mode.
D15	TX_DISABLE	LED illuminates when the transmitter is disabled.
D16	TX_ENABLE	LED illuminates when the transmitter is enabled.
D19	LOS	LED illuminates when the received signal power drops below a defined threshold.
TP1	VCCR	Test point for monitoring receiver supply voltage
TP2	VCCT	Test point for monitoring transmitter supply voltage
TP13	SCL	Test point for monitoring I <sup>2</sup> C serial clock
TP14	SDA	Test point for monitoring I <sup>2</sup> C serial data
TP15	TX_FAULT	Test point for monitoring transmitter fault
TP16	TX_DISABLE	Test point for monitoring transmitter disable
TP17, TP23	GND	Ground test points
TP18	RATESEL0	Test point for monitoring rate select 0
TP19	LOS	Test point for monitoring receiver loss-of-signal (LOS)
TP20	RATESEL1	Test point for monitoring rate select 1



## 7 Signal Definitions (20-Pin Connector, J13)

I/O direction assumes the SFP module as the reference.

Connector Pin (J13)	I/O Type	NAME	Definition
1, 17, 20		VEET	Module transmitter ground. This pin can be connected to VEER inside the SFP module.
2	LVTTL OUTPUT	TX_FAULT	Transmitter fault output (Note 1). The transmitter is disabled when TX_FAULT is asserted.
3	LVTTL INPUT	TX_DISABLE	Transmitter disable input. The transmitter is disabled when TX_DISABLE is asserted.
4	LVTTL INPUT / OUTPUT	MOD-DEF2	2-wire serial interface, bidirectional data line (Note 1)
5	LVTTL INPUT	MOD-DEF1	2-wire serial interface clock line (Note 1)
6	LVTTL OUTPUT	MOD-DEF0	Pin is pulled low by the SFP module to indicate to the host controller that a module is present (Note 1).
7	LVTTL INPUT	RATE SEL0	Optional receiver bandwidth selection input (0)
8	LVTTL OUTPUT	LOS	Receiver loss-of-signal output (Note 1). Output is high when receiver input signal is below the set threshold.
9	LVTTL INPUT	RATE SEL0	Receiver bandwidth selection input (1) for SFP+ modules. This pin is internally grounded in standard SFP modules.
10, 11, 14		VEER	Module receiver ground. This pin can be connected to VEET inside the SFP module.
12	OUTPUT	RD-	Inverted received data output, AC-coupled inside the SFP module
13	OUTPUT	RD+	Noninverted received data output, AC-coupled inside the SFP module
15		VCCR	+3.3V receiver power-supply connection. Can be internally connected to VcCT in the SFP Module.
16		VcCT	+3.3V transmitter power-supply connection. Can be internally connected to VCCR in the SFP Module.
18	INPUT	TD+	Inverted transmit data input, AC-coupled inside the SFP module
19	INPUT	TD-	Noninverted transmit data input, AC-coupled inside the SFP module

**Note 1:** Open collector output. These pins are pulled high on the host board.

## 8 Component List

Designation	Qty	Description
C1, C84	2	10 $\mu$ F $\pm$ 10% ceramic capacitor (0805)
C2, C3, C28, C29, C58, C85	6	0.1 $\mu$ F $\pm$ 10% ceramic capacitor (0603)
C5, C30	2	22 $\mu$ F $\pm$ 10% ceramic capacitor (0805)
C17, C19, C20, C34, C51, C55, C57	7	1 $\mu$ F $\pm$ 10% ceramic capacitor (0603)
C18, C22	2	33pF $\pm$ 10% ceramic capacitor (0402)
C21, C23, C37	3	4.7 $\mu$ F $\pm$ 10% ceramic capacitor (0805)
C24-C27, C49, C50, C52, C59, C63, C64, C90, C91	12	0.1 $\mu$ F $\pm$ 10% ceramic capacitor (0402)
C76-C78	3	0.01 $\mu$ F $\pm$ 10% ceramic capacitor (0402)
D1, D8, D14, D15, D19	5	Red LED
D2, D16	2	Green LED
J1	1	2x3 header, 0.1in spacing
J12	1	USB connector, Tyco 440247-1
J13	1	SFP connector, AMP 1367073-1
J17-J20	4	Side-mount SMA connector, Rosenberger 32k243-40M
J21, J22	2	PCB-mount SMA connector, Johnson 142-701-231
L1, L3	2	22 $\mu$ H inductor, Taiyo-Yuden CBC3225T220M

Designation	Qty	Description
L5, L18	2	4.7 $\mu$ H inductor, Taiyo-Yuden CBC3225T4R7M
L6	1	1.0 $\mu$ H inductor, Taiyo-Yuden CBC3225T1R0M
R1, R3, R4, R48, R89, R94, R97, R98	8	Open (0402)
R2, R52, R55, R62, R66, R73, R86	7	49.9 $\Omega$ $\pm$ 1% resistor (0402)
R9, R25, R37, R41, R49-R51, R92, R107	7	10k $\Omega$ $\pm$ 1% resistor (0402)
R24	1	1.5k $\Omega$ $\pm$ 1% resistor (0402)
R67-R72	6	470 $\Omega$ $\pm$ 5% resistor (0402)
R87, R88	2	24.9k $\Omega$ $\pm$ 1% resistor (0402)
R90, R93	2	0 $\Omega$ $\pm$ 5% resistor (0402)
R91	1	681 $\Omega$ $\pm$ 5% resistor (0402)
R95, R96	2	0.1 $\Omega$ $\pm$ 1% resistor (1206)
TP1, TP2, TP13-TP20, TP23, J11, J16	13	Test points
U10	1	Microcontroller, Microchip PIC16C745-I/SO
U13, U16, U17	3	Dual inverter, Fairchild NC7WZ04P6X
U14, U19	2	ADC, Max1362EUB
U20, U22	2	High-side current-sense amp, MAX4070AUA
U21	1	Bidirectional level translator, MAX3373EXK
Y1	1	Crystal, ECS Inc. XC679CT

# 9 Schematic

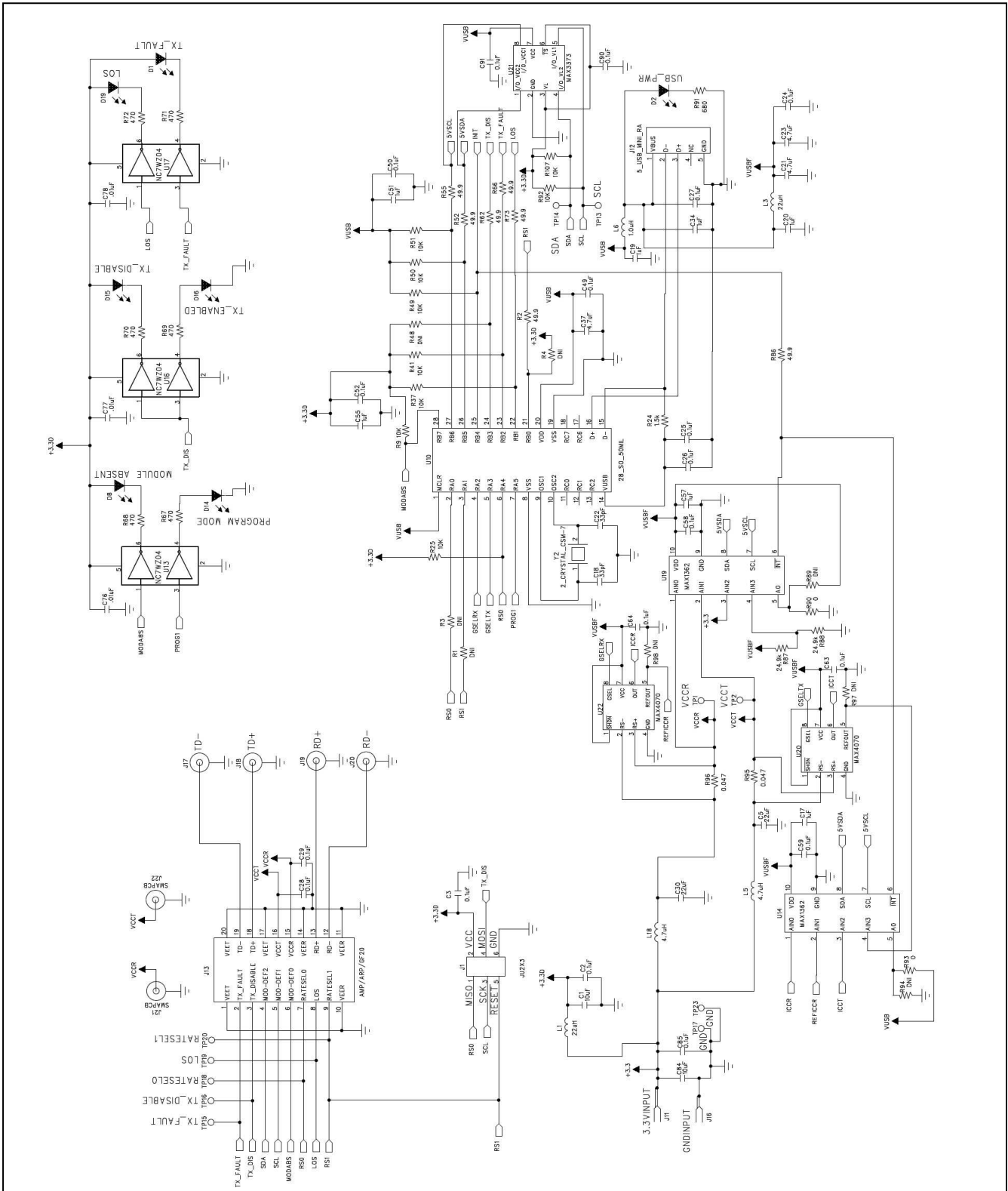


Figure 4. HFRD-30.1 SFP+ host board schematic.

# 10 Board Dimensions/Layout

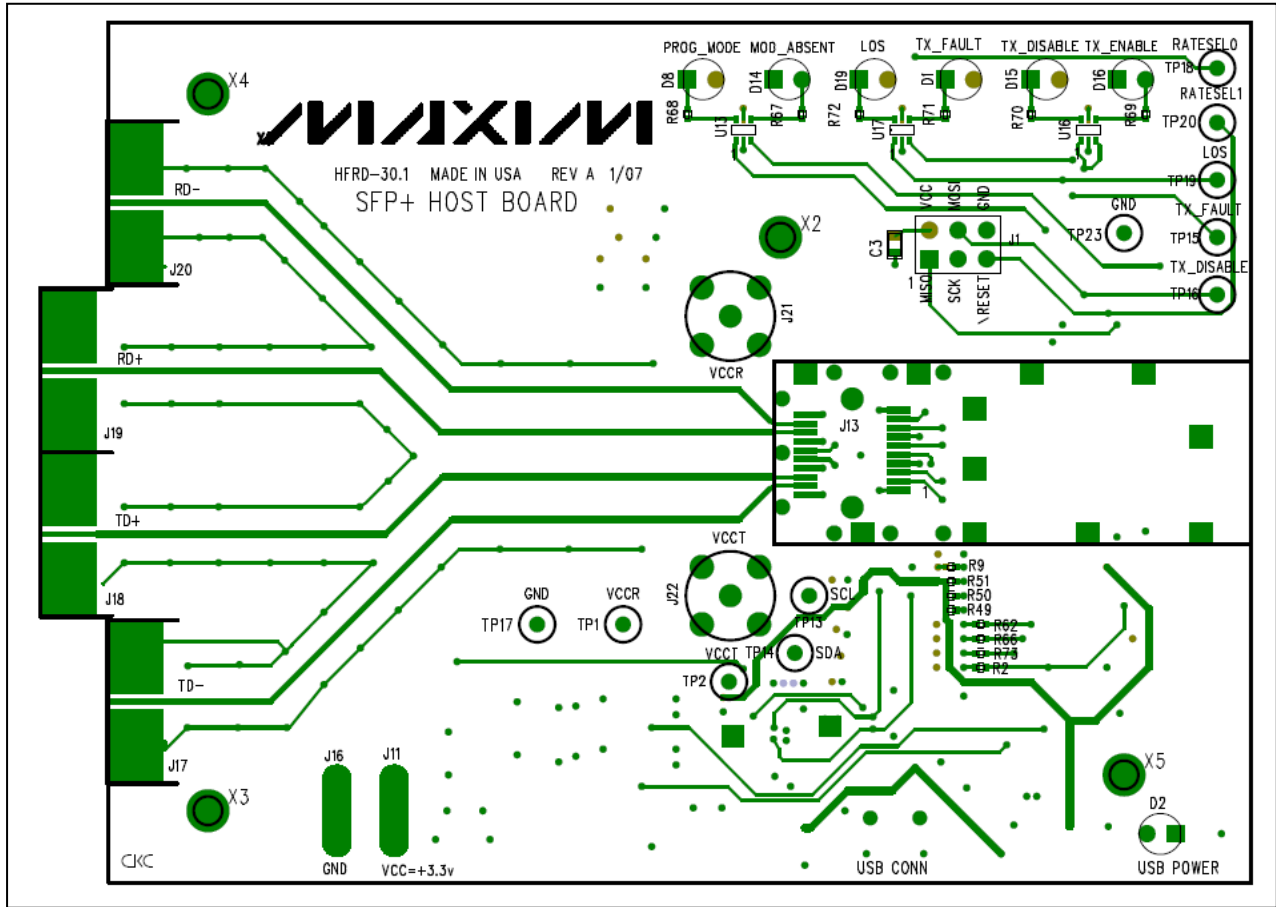


Figure 5. HFRD-30.1 application view, Layer 1.

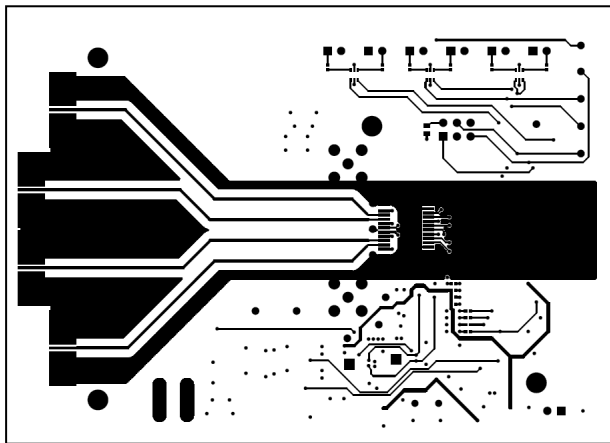


Figure 6. Board layout—component side, Layer 1.

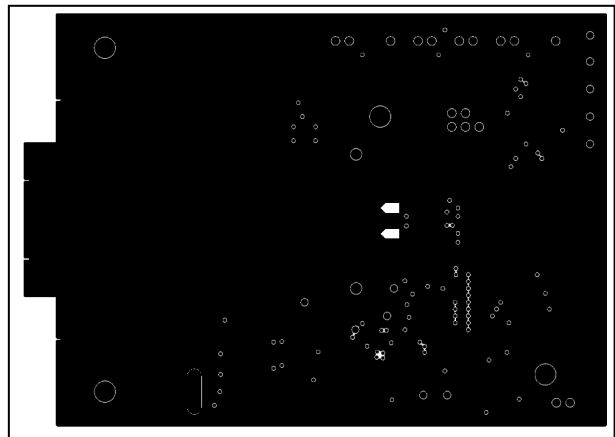


Figure 7. Board layout—ground plane, Layer 2.

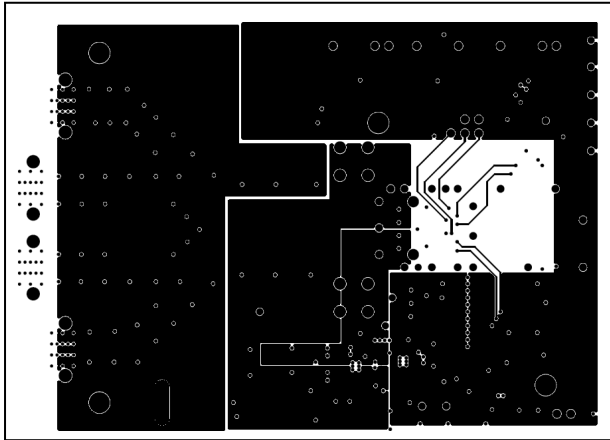


Figure 8. Board layout—power plane, Layer 3.

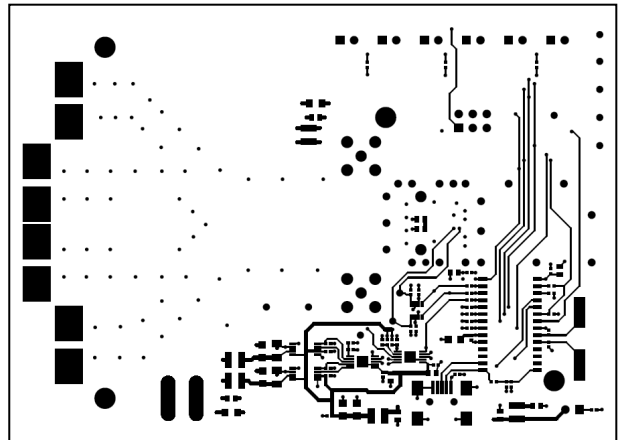


Figure 9. Board layout—solder side, Layer 4.

## 11 Layer Profile

The HFRD-30.1 SFP+ host board includes controlled-impedance transmission lines (**Figure 10**). The layer profile is based on the following assumptions:

1. Dielectric material is Rogers 4350 with a dielectric constant of ~ 3.48
2. 0.5oz copper foil before plating

	Single-Ended	Coupled
<b>A</b>	20mil	N.A.
<b>B</b>	> 60mil	N.A.
<b>C</b>	10mil	N.A.
<b>D</b>	As needed	As needed

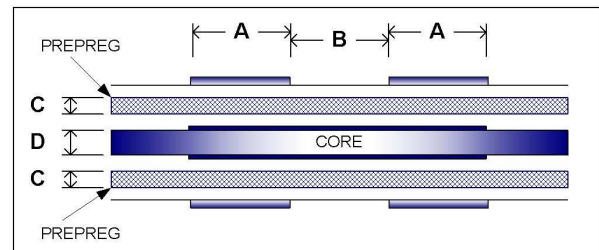


Figure 10. Layer profile.

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