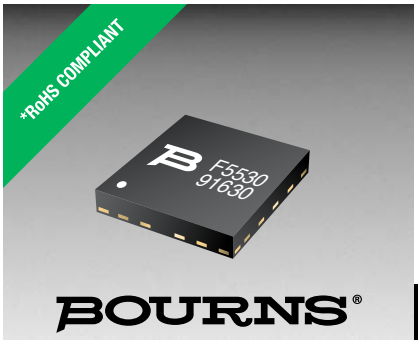


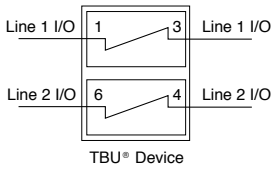
Features

- Superior circuit protection
- Overcurrent protection
- Blocks surges up to rated voltage limit
- High-speed performance
- Small SMT package
- RoHS compliant*

TBU-DF Series - TBU® High-Speed Protectors

General Information

The TBU-DF Series of Bourns® TBU® products are low capacitance dual bidirectional high-speed Electronic Current Limiters (ECLs), constructed using MOSFET semiconductor technology, and designed to protect against faults caused by short circuits, overvoltage transients and faults in battery cells, up to rated limits.



The TBU® high-speed protector placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics will not be exposed to large voltages or currents during transient events.

The TBU® device is provided in a surface mount DFN package and meets industry standard requirements such as RoHS and Pb Free solder reflow profiles.

Additional Information

Click these links for more information:

PRODUCT SELECTOR | TECHNICAL LIBRARY | INVENTORY | SAMPLES | CONTACT

Absolute Maximum Ratings (@ T_A = 25 °C Unless Otherwise Noted)

Symbol	Parameter	Part Number	Value	Unit
V_{imp}	Peak impulse voltage withstand with duration less than 10 ms	TBU-DF055-xxx-WH TBU-DF085-xxx-WH	550 850	V
V_{rms}	Continuous A.C. RMS voltage	TBU-DF055-xxx-WH TBU-DF085-xxx-WH	250 425	V
T_{op}	Operating temperature range		-55 to +125	°C
T_{stg}	Storage temperature range		-65 to +150	°C
T_{amax}	Maximum Ambient Temperature		+125	°C

Electrical Characteristics (@ T_A = 25 °C Unless Otherwise Noted)

Symbol	Parameter		Part Number	Min.	Typ.	Max.	Unit
$I_{trigger}$	Current required for the device to go from operating state to protected state		TBU-DFxxx-050-WH TBU-DFxxx-100-WH TBU-DFxxx-200-WH TBU-DFxxx-300-WH TBU-DFxxx-500-WH	50 100 200 300 500	75 150 300 450 750	100 200 400 600 1000	mA
R_{device}	Series resistance of the TBU® device	V_{imp} = 550 V $I_{trigger}$ (min.) = 50 mA V_{imp} = 550 V $I_{trigger}$ (min.) = 100 mA V_{imp} = 550 V $I_{trigger}$ (min.) = 200 mA V_{imp} = 550 V $I_{trigger}$ (min.) = 300 mA V_{imp} = 550 V $I_{trigger}$ (min.) = 500 mA V_{imp} = 850 V $I_{trigger}$ (min.) = 50 mA V_{imp} = 850 V $I_{trigger}$ (min.) = 100 mA V_{imp} = 850 V $I_{trigger}$ (min.) = 200 mA V_{imp} = 850 V $I_{trigger}$ (min.) = 300 mA V_{imp} = 850 V $I_{trigger}$ (min.) = 500 mA	TBU-DF055-050-WH TBU-DF055-100-WH TBU-DF055-200-WH TBU-DF055-300-WH TBU-DF055-500-WH TBU-DF085-050-WH TBU-DF085-100-WH TBU-DF085-200-WH TBU-DF085-300-WH TBU-DF085-500-WH	12 9.5 7.5 6 5 23 14.5 12.5 15 12		26 18.5 15.5 14 13 38 26.5 22.5 26 25	Ω
R_{match}	Package resistance matching of the TBU® device #1 - TBU® device #2					+0.5	Ω
t_{block}	Time for the device to go from normal operating state to protected state				1		µs
I_Q	Current through the triggered TBU® device with 50 Vdc circuit voltage				0.5		mA
V_{reset}	Voltage below which the triggered TBU® device will transition to normal operating state			12	16	20	V
$R_{th(j-a)}$	Junction to ambient - FR4 using JESD51-3 board				125		°C/W
$R_{th(j-a)}$	Junction to ambient - FR4 using JESD51-7 board				50		°C/W

WARNING Cancer and Reproductive Harm
www.P65Warnings.ca.gov

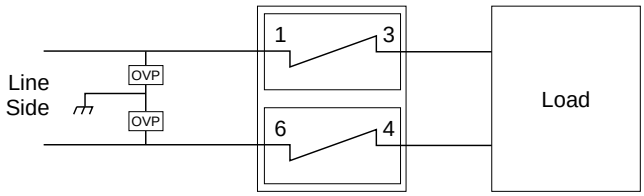
*RoHS Directive 2015/863, Mar 31, 2015 and Annex.
Specifications are subject to change without notice.
Users should verify actual device performance in their specific applications.
The products described herein and this document are subject to specific legal disclaimers as set forth on the last page of this document, and at www.bourns.com/docs/legal/disclaimer.pdf.

Environmental Characteristics

Parameter	Value
Moisture Sensitivity Level	1
ESD Classification (HBM)	1B

Reference Application

The TBU® devices are general use protectors used in a wide variety of applications, including telecommunications, and industrial communications. The maximum voltage rating of the TBU® device should never be exceeded. Where necessary, an OVP device should be employed to limit the maximum voltage. A cost-effective protection solution combines Bourns® TBU® protection devices with a pair of Bourns® TISP® Overvoltage Protectors or MOVs. For bandwidth sensitive applications, a Bourns® GDT may be substituted for the MOV.



TBU® Device

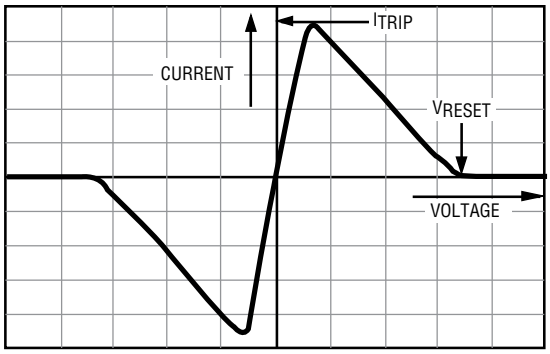
Basic TBU Operation

The TBU® device, constructed using MOSFET semiconductor technology, placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics are not exposed to large voltages or currents during transient events. When operated, the TBU® device will limit the current to less than the $I_{trigger}$ value within the t_{block} duration. If voltage above V_{reset} is continuously sustained, the TBU® device will subsequently reduce the current to a quiescent current level within a period of time that is dependent upon the applied voltage.

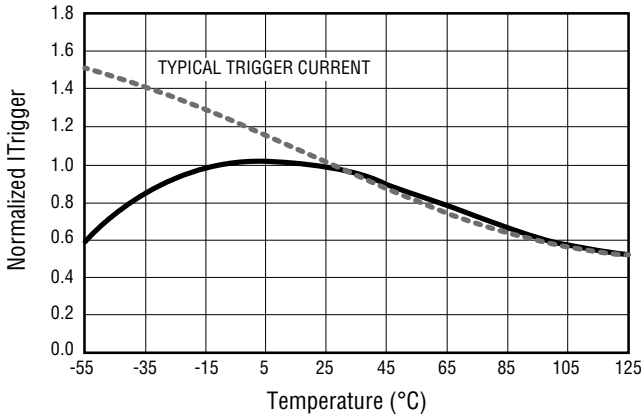
After the surge, the TBU® device resets when the voltage across the TBU® device falls to the V_{reset} level. The TBU® device will automatically reset on lines which have no DC bias or have DC bias below V_{reset} (such as unpowered signal lines).

Performance Graphs

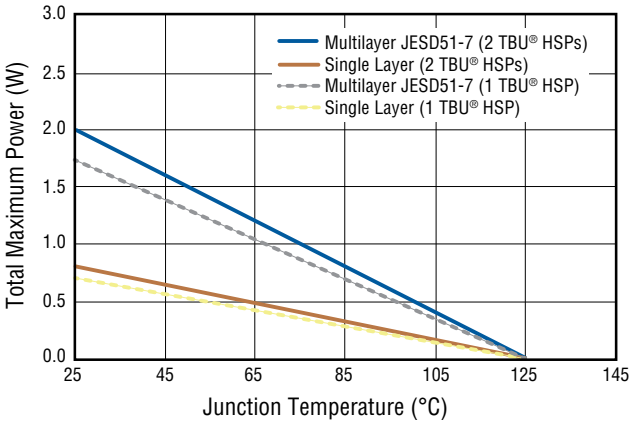
Typical V-I Characteristics



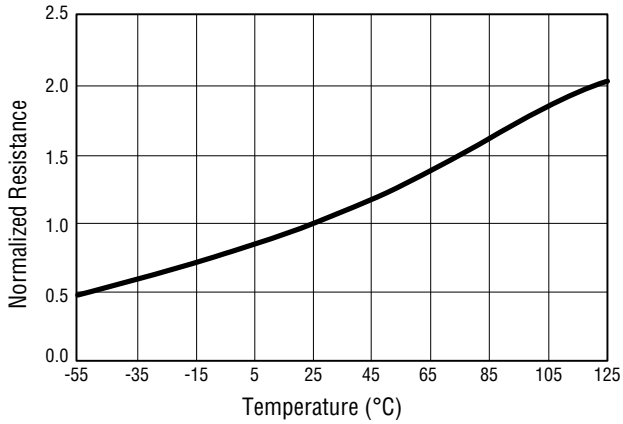
Normalized Itrigger vs. Temperature



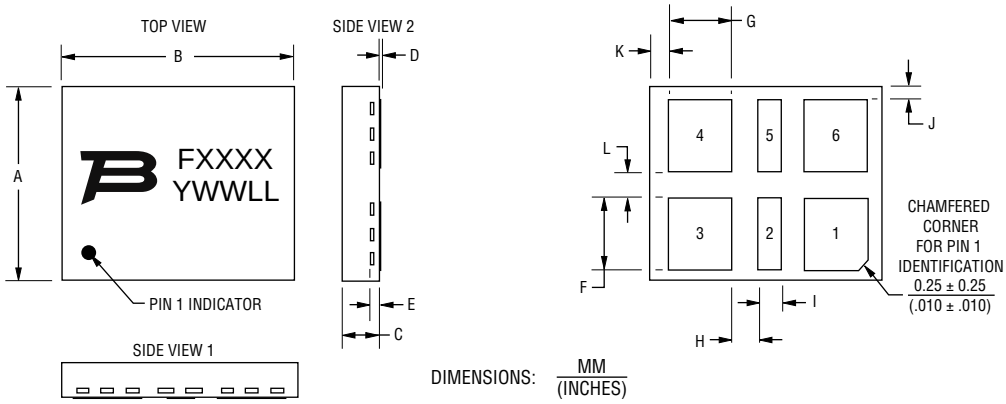
Power Derating Curve



Normalized Resistance vs. Temperature



Product Dimensions



Dim.	Min.	Nom.	Max.
A	5.40 (.213)	5.50 (.217)	5.60 (.220)
B	6.40 (.252)	6.50 (.256)	6.60 (.260)
C	0.80 (.031)	0.90 (.035)	1.00 (.039)
D	0.00 (.000)	—	0.05 (.002)
E		0.20 (.008) REF.	
F	1.90 (.075)	2.00 (.079)	2.10 (.083)
G	1.75 (.069)	1.85 (.073)	1.95 (.077)
H	0.65 (.026)	0.70 (.028)	0.75 (.030)
I	0.70 (.028)	0.80 (.031)	0.90 (.035)
J	0.30 (.012)	0.35 (.014)	0.40 (.016)
K	0.25 (.010)	0.30 (.012)	0.35 (.014)
L	0.75 (.030)	0.80 (.031)	0.85 (.033)

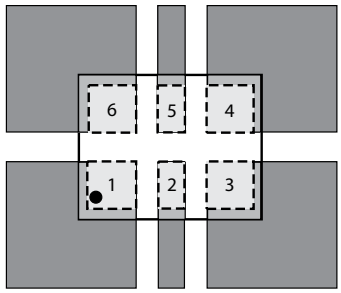
Pad #	Pin Out
1	Line 1 In/Out
2	NU (Not Used)
3	Line 1 In/Out
4	Line 2 In/Out
5	NU (Not Used)
6	Line 2 In/Out

NOTES:

1. Pin 1 Indicator is laser marked; radius and location within the Pin 1 terminal.
   Pin 1 dot size: 0.500 ± 0.125 mm / (.020 ± .005 in.).
2. Pin 2 and 5 are NU (Not Used) and must be left unconnected; do not connect to In/Out lines, do not connect to system Ground.
3. Coplanarity on exposed pads shall not exceed 0.08 mm / (.003 in.).
4. Warpage shall not exceed 0.10 mm / (.004 in.) on all surfaces.
5. Exposed tie bars at package side are not plated.

Recommended Pad Layout

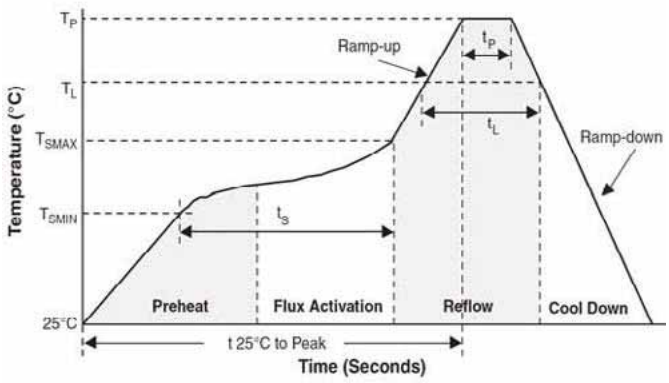
TBU® High-Speed Protectors have a 100 % matte-tin termination finish. For improved thermal dissipation, the recommended layout uses PCB copper areas which extend beyond the exposed solder pad. The exposed solder pads should be defined by a solder mask which matches the pad layout of the TBU® device in size and spacing. It is recommended that they should be the same dimension as the TBU® pads but if smaller solder pads are used, they should be centered on the TBU® package terminal pads and not more than 0.10-0.12 mm (0.004-0.005 in.) smaller in overall width or length. Solder pad areas should not be larger than the TBU® pad sizes to ensure adequate clearance is maintained. The recommended stencil thickness is 0.10-0.12 mm (0.004-0.005 in.) with a stencil opening size 0.025 mm (0.0010 in.) less than the solder pad size. Extended copper areas beyond the solder pad significantly improve the junction to ambient thermal resistance, resulting in operation at lower junction temperatures with a corresponding benefit of reliability. All pads should soldered to the PCB, including pads marked as NC or NU but no electrical connection should be made to these pads. Care should be taken to assure no resistive path exists between the NC or NU pins to any other point to avoid unexpected performance issues. For minimum parasitic capacitance, it is recommended that signal, ground or power signals are not routed beneath any pad. For minimum parasitic capacitance, it is recommended that signal, ground or power signals are not routed beneath any pad.



Dark grey areas show added PCB copper area for better thermal resistance.

Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Tsmax to Tp)	3 °C/sec. max.
Preheat - Temperature Min. (Tsmin) - Temperature Max. (Tsmax) - Time (tsmin to tsmax)	 150 °C 200 °C 60-180 sec.
Time maintained above: - Temperature (TL) - Time (tL)	 217 °C 60-150 sec.
Peak/Classification Temperature (Tp)	260 °C
Time within 5 °C of Actual Peak Temp. (tp)	20-40 sec.
Ramp-Down Rate	6 °C/sec. max.
Time 25 °C to Peak Temperature	8 min. max.



How to Order

TBU - DF xxx - yyy - WH

TBU® Product

Series
DF = Dual Bidirectional Series

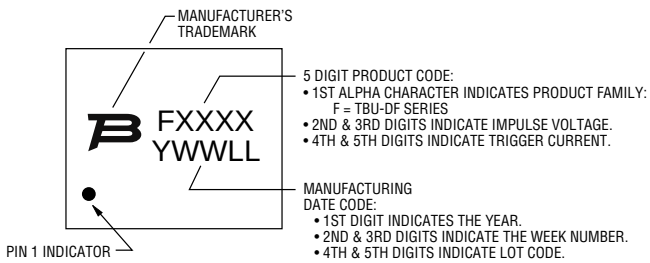
Impulse Voltage Rating
055 = 550 V
085 = 850 V

Trigger Current
050 = 50 mA
100 = 100 mA
200 = 200 mA
300 = 300 mA
500 = 500 mA

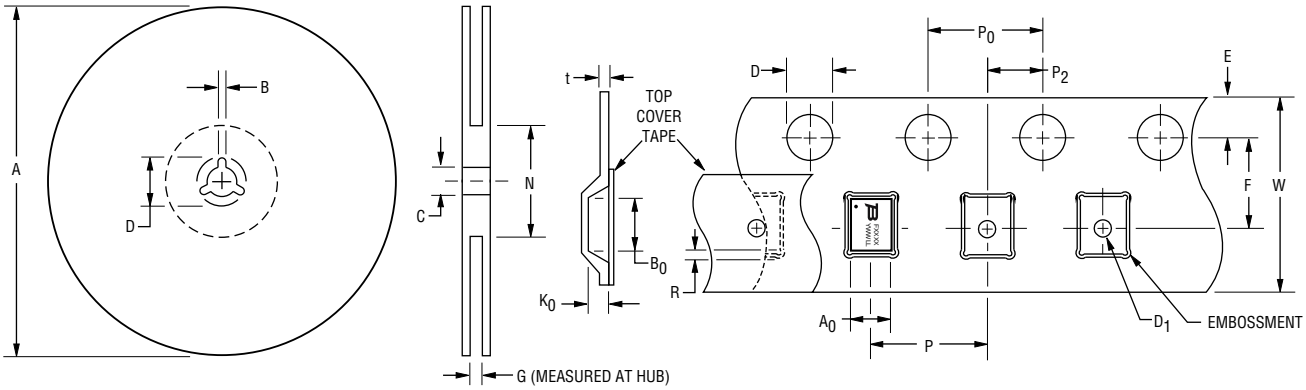
Hold to Trip Ratio Suffix
W = Hold to Trip Ratio

Package Suffix
H = DFN Package

Typical Part Marking



Packaging Specifications



QUANTITY: 3000 PIECES PER REEL

A		B		C		D		G	N
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Ref.	Ref.
328.5 (12.93)	331 (13.05)	2.0 (.079)	2.4 (.094)	12.8 (.504)	13.5 (.531)	17.0 (.669)	17.4 (.690)	16.5 (.650)	100 ± 1.5 (3.94 ± .059)

A_0		B_0		D_0		D_1		E		F	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
5.75 (.224)	5.95 (.234)	6.75 (.266)	6.95 (.274)	1.5 (.059)	1.6 (.063)	1.5 (.059)	—	1.65 (.065)	1.85 (.073)	7.4 (.291)	7.6 (.299)

K_0		P		P_0		P_2		R		t	
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
1.05 (.041)	1.25 (.049)	7.9 (.311)	8.1 (.319)	3.9 (.159)	4.1 (.161)	1.9 (.075)	2.1 (.083)	0 (0)	0.5 (.020)	0.25 (.010)	0.35 (.014)

W	
Min.	Max.
15.7 (.618)	16.3 (.642)

DIMENSIONS: MM (INCHES)

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