



2-Lane DisplayPort™ Rev 1.2 Compliant Switch

Features

- → Two-Lane, 1:2 Mux/Demux Supports RBR, HBR1, or HBR2
- → One-Channel 1:2 Mux/Demux for DP_HPD Signal
- → One-Differential Channel 1:2 Mux/Demux for DP_Aux Signal with Support up to 720Mbps
- → Insertion Loss for High-Speed Channels @ 2.7 GHz: -1.7dB
- → -3dB Bandwidth for High-Speed Channels: 4.7GHz
- → Return Loss for High-Speed Channels @ 2.7GHz: -16dB
- → Low Bit-to-Bit Skew, 7ps max (between '+' and '-' bits)
- → Low Crosstalk for High-Speed Channels: -25dB @ 5.4Gbps
- → Low Off Isolation for High-Speed Channels: -25dB @ 5.4Gbps
- → V_{DD} Operating Range: 3.3V ±10%
- → ESD Tolerance: 2kV HBM
- → Low Channel-to-Channel Skew, 35ps max
- → Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- → Halogen and Antimony Free. "Green" Device (Note 3)
- → Packaging (Pb-free & Green):
 - 32 TQFN (ZL)

Truth Table

ŌĒ	SEL	AUX_SEL	Function
Low	Low	Low	Port A Active for all Channels
Low	Low	High	Port A for HS, Port B for HPD/AUX
Low	High	Low	Port B for HS, Port A for HPD/AUX
Low	High	High	Port B Active for all Channels
High	X	X	All I/Os are hi-z and IC is Power Down

Description

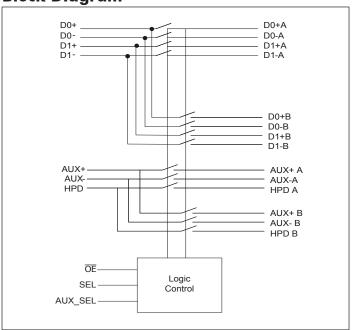
Diodes' PI3VDP3212 mux/demux is targeted for next generation digital video signals. This device can be used to connect a DisplayPort™ Source to two independent DisplayPort sinks or to connect two DisplayPort sources to a single DP display.

The newly released DisplayPort spec requires a data rate of 5.4Gbps. Diodes' solution is specifically designed around this standard and supports such signals.

Application

Routing of DisplayPort signals with low-signal attenuation between source and sink.

Block Diagram



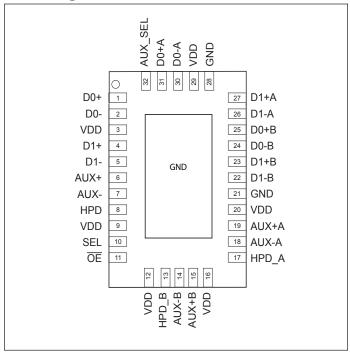
Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.





Pin Assignment



Pin Description

Pin#	Pin Name	Type	Description
1	D0+	I/O	Positive differential signal 0 for COM port
2	D0-	I/O	Negative differential signal 0 for COM port
4	D1+	I/O	Positive differential signal 1 for COM port
5	D1-	I/O	Negative differential signal 1 for COM port
6	AUX+	I/O	Positive differential signal for AUX COM port
7	AUX-	I/O	Negative differential signal for AUX COM port
8	HPD	I/O	HPD for COM port
10	SEL	I	Switch logic control. If HIGH, path B is selected for high-speed channels only. If LOW, path A is selected for high-speed channels only.
11	ŌĒ	I	Output enable. If \overline{OE} is low, IC is enabled. If \overline{OE} is high, IC is powered down and all I/Os are hi-z.
13	HPD_B	I/O	HPD for port B
14	AUX-B	I/O	Negative differential signal for AUX, port B
15	AUX+B	I/O	Positive differential signal for AUX, port B
17	HPD_A	I/O	HPD for port A
18	AUX-A	I/O	Negative differential signal for AUX, port A
19	AUX+A	I/O	Positive differential signal for AUX, port A





Pin Description Cont.

Pin#	Pin Name	Type	Description
22	D1-B	I/O	Negative differential signal 1 for port B
23	D1+B	I/O	Positive differential signal 1 for port B
24	D0-B	I/O	Negative differential signal 0 for port B
25	D0+B	I/O	Positive differential signal 0 for port B
26	D1-A	I/O	Negative differential signal 1 for port A
27	D1+A	I/O	Positive differential signal 1 for port A
21, 28	GND	Ground	Ground
3, 9, 12, 16, 20, 29	VDD	Power	3.3V ±10% power supply
30	D0-A	I/O	Negative differential signal 0 for port A
31	D0+A	I/O	Positive differential signal 0 for port A
			Switches only the AUX and HPD channels from port A vs. port B.
32	AUX_SEL	I	If High, path B is selected.
			If LOW, path A is selected.





Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	65°C to +150°C
Supply Voltage to Ground Potential	0.5V to +4.2V
DC Input Voltage	0.5V to V _{DD}
DC Output Current	120mA
Power Dissipation	0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics for Switching over Operating Range

 $(TA = -40^{\circ}C \text{ to } +85^{\circ}C, VDD = 3.3V \pm 10\%)$

Parameter	Description	Test Conditions(1)	Min	Typ ⁽¹⁾	Max	Units
v_{IH}	Input HIGH Voltage	Guaranteed HIGH level	1.5	_	_	
v_{IL}	Input LOW Voltage	Guaranteed LOW level	_	_	0.75	V
v_{IK}	Clamp Diode Voltage, Dx	$V_{\mathrm{DD}} = \mathrm{Max.}, \mathrm{I_{\mathrm{IN}}} = -18\mathrm{mA}$	_	-1.6	-1.8	
IIH	Input HIGH Current	$V_{DD} = Max., V_{IN} = V_{DD}$	_	_	±5	
IIL	Input LOW Current	$V_{DD} = Max., V_{IN} = GND$	_	_	±5	
I _{OFF_SB}	I/O Leakage when Part is off for Sideband Signals Only (DDC, AUX, HPD)	$V_{DD} = 0V$, $V_{INPUT} = 0V$ to 3.6V	_	_	20	μA
R _{ON_HS}	On Resistance between Input to Output for High-Speed Signals	$V_{\rm DD}$ = 3.3V, Vinput = 0V to 2V, $I_{\rm INPUT}$ = 20mA	_	10	_	Ω
R _{ON_AUX}	On Resistance between Input to Output for Sideband Signals (AUX)	$V_{\rm DD}$ = 3.3V, Vinput = 0 to 3.3V, $I_{\rm INPUT}$ = 20mA	_	7	_	Ω
Aux_ss	Signal Swing Tolerance in Aux Path	$V_{\mathrm{DD}} = 3.0 \mathrm{V}$	-0.5	_	3.6	V
HPD_I	Input Voltage Tolerance on HPD Path	_	_	_	5.5	V
HPD_O	Output Voltage on HPD Path	HPD input from 0V to 5.25V	_	_	3.6	V

Power Supply Characteristics (TA = -40° C to $+85^{\circ}$ C)

Parameter	Description	Test Conditions(1)	Min	Typ(1)	Max	Units
I_{CC}	Quiescent Power Supply Current	$V_{DD} = 3.3V$, $V_{IN} = GND$ or V_{DD}	_	320	500	μΑ





Dynamic Electrical Characteristics over Operating Range

(TA = -40°C to +85°C, $VDD = 3.3V \pm 10$ %)

Parameter	Description	Test Conditions		Тур.	Max	Units
37		See Figure 1 for	f = 2.7GHz	-25dB		
X_{TALK}	Crosstalk on High-Speed Channels	Measurement Setup	f = 1.35GHz	-32dB		
			f = 2.7GHz	-22dB	_	dB
O _{IRR}	OFF Isolation on High-Speed Channels	See Figure 2 for Measurement Setup	f = 1.35GHz	-30dB		
I_{LOSS}	Differential Insertion Loss on High-Speed Channels	@ 5.4Gbps (see Figure 3)		-1.7	_	dB
R _{loss}	Differential Return Loss on High-Speed Channels	@ 2.7GHz		-16	_	dB
BW_Dx±	Bandwidth -3dB for Main High-Speed Path (Dx±)	See Figure 3		4.7	_	GHz
BW_AUX/ HPD	-3dB BW for AUX and HPD Signals	ee Figure 3		1.5	_	GHz
Tsw a-b	Switching Time from Port A to Port B	_		_	1	μs
Tsw b-a	Switching Time from Port B to Port A	_		_	1	μs
Tstartup	Vdd Valid to Channel Enable	_		_	10	μs
Twakeup	Enabling Output by Changing $\overline{\text{OE}}$ from Low to High	_		_	10	μs

Note:

Switching Characteristics ($T_A = -40$ °C to +85°C, $V_{DD} = 3.3V \pm 10\%$)

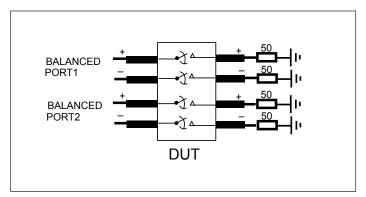
Parameter	Description		Тур.	Max.	Units
T_{pd}	Propagation Delay (Input pin to Output pin)	_	80	_	ps
t _{b-b}	Bit-to-Bit Skew Within the Same Differential Pair	_	5	_	ps
t _{ch-ch}	Channel-to-Channel Skew	_	_	50	ps

^{1.} For maxium or minimum conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.

^{2.} Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.







BALANCED PORT1

BALANCED
PORT2

BALANCED
PORT2

Fig 1. Crosstalk Setup

Fig 2. Off-Isolation Setup

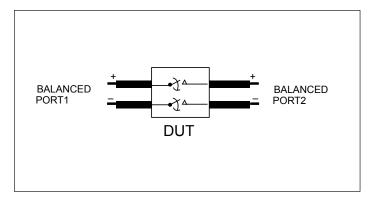


Fig 3. Differential Insertion Loss Setup

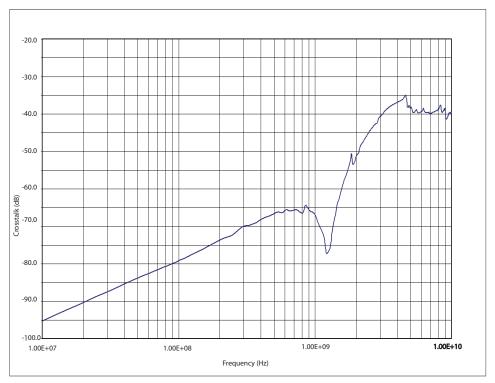


Fig 4. Xtalk for High-Speed Channels (D0 and D1)





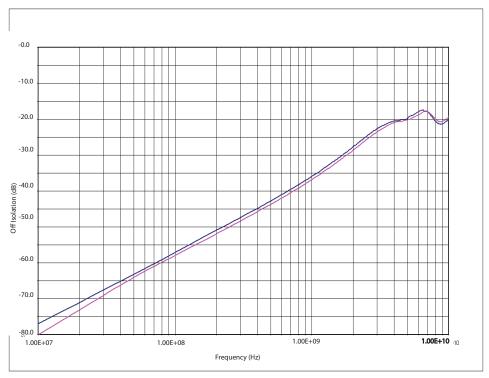


Fig 5. Off Isolation for High-Speed Channels (D0 and D1); Red is for Path B and Blue is for Path A

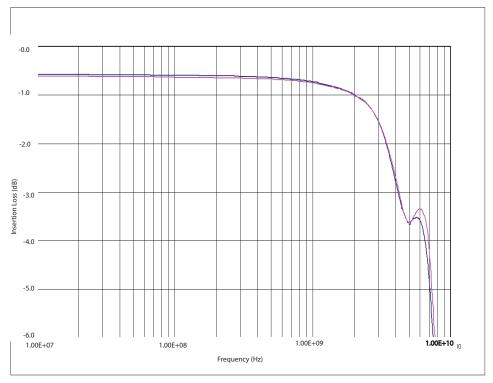
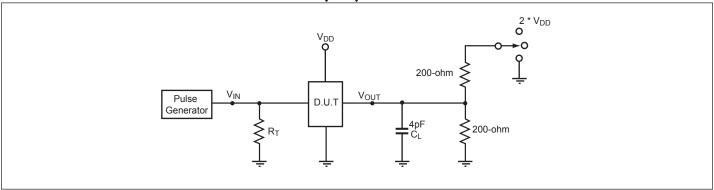


Fig 6. Insertion Loss for High-Speed Channels (D0 and D1); Red is for Path B and Blue is for Path A





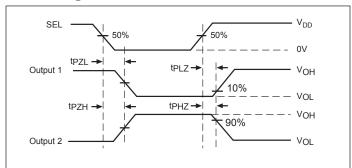
Test Circuit for Electrical Characteristics (1-5)



Notes:

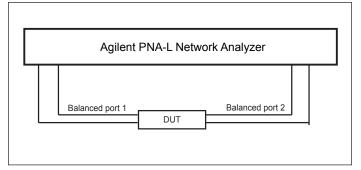
- 1. C_L = Load capacitance; includes jig and probe capacitance.
- 2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
- 3. Output 1 is for an output with internal conditions, so the output is low except when disabled by the output control.
- 4. Output 2 is for an output with internal conditions, so the output is high except when disabled by the output control.
- 5. All input impulses are supplied by generators having the following characteristics: $PRR \le MHz$, $Z_O = 50\Omega$, $t_R \le 2.5$ ns, $t_F \le 2.5$ ns.
- 6. The outputs are measured one at a time with one transition per measurement.

Switching Waveforms



Voltage Waveforms Enable and Disable Times

Test Circuit for Dynamic Electrical Characteristics



Switch Positions

Test	Switch
t _{PLZ} , t _{PZL} (Output on B-side)	$2 \times Vdd$
t _{PHZ} , t _{PZH} (Output on B-side)	GND
Prop Delay	Open

Part Marking

ZL Package



YY: Year

WW: Workweek

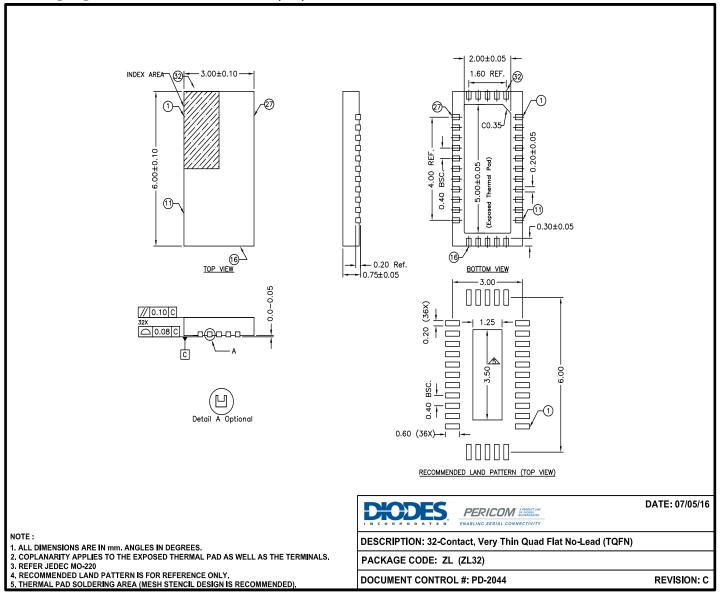
1st X: Assembly Code

2nd X: Fab Code





Packaging Mechanical: 32-TQFN (ZL)



0 0 1 4 2

For latest package information:

 $See \ http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/. \\$

Ordering Information

Ordering Code	Package Code	Package Description
PI3VDP3212ZLEX	ZL	32-Contact, Very-Thin Quad-Flat No-Lead (TQFN)

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. E = Pb-free and Green
- 5. X suffix = Tape/Reel





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