

## 6.5Gbps 4-Lane SAS2/SATA/XAUI ReDriver™ with Equalization & De-emphasis

### Features

- Up to 6.5Gbps SAS2/SATA/XAUI ReDriver™
- Supporting 8 differential channels or 4 lanes
- Independent channel configuration
- Pin strapped and I<sup>2</sup>C configuration controls (3.3V Tolerant)
- Adjustable receiver equalization
- Adjustable transmitter amplitude and de-emphasis
- Adjustable input threshold level
- 50-Ohm input/output termination
- Mux/Demux and loop-back features
- OOB fully supported
- Single supply voltage, 1.2V ± 5%
- Active Current per channel - 95mA (typical)
- Automatic slumber mode power savings
  - Slumber current per channel -10mA (typical)
- Power down Standby Mode
  - Standby current -1mA (typical)
- Industrial temperature range: -40°C to 85°C
- Packaging (Pb-free & Green):
  - 100-contact LPGA (11mm x11mm)

### Description

Pericom Semiconductor's PI2EQX6814 is a 6.5Gbps low power, 4 lane (8 channel) SAS2, SATA, XAUI signal ReDriver™. The device provides programmable equalization, amplification, and de-emphasis by either pin strapping or I<sup>2</sup>C control, select bits, to optimize performance over a variety of physical mediums by reducing Inter-symbol interference.

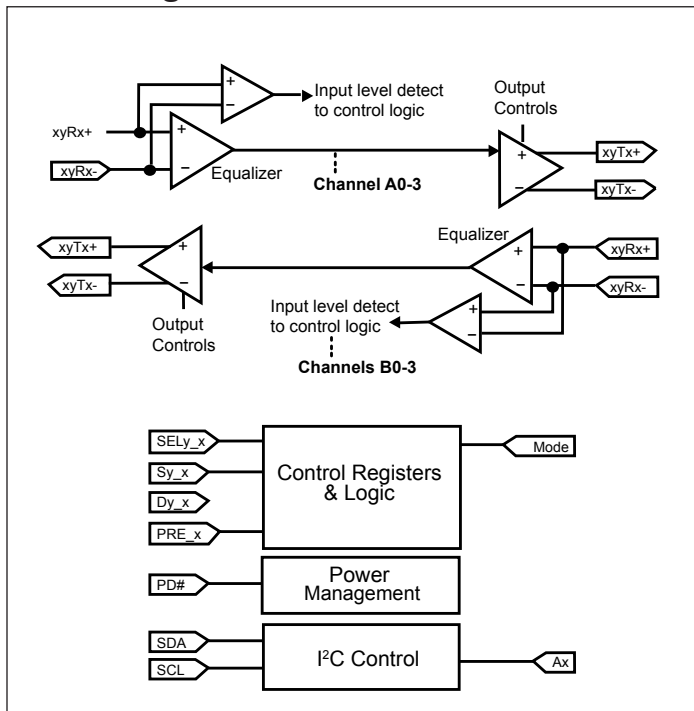
PI2EQX6814 supports eight 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a back-plane, or extends the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver, whereas the integrated de-emphasis circuitry provides flexibility with signal integrity of the signal after the ReDriver.

In addition to providing signal re-conditioning, Pericom's PI2EQX6814 also provides power management Stand-by mode operated by a Power Down pin, or through I<sup>2</sup>C register.

In addition, the device performs automatic Slumber Mode (Disable Transmit) during idle conditions on the receiver.

### Block Diagram



### Pin Configuration (Top-Side View)

|   | 1      | 2      | 3      | 4     | 5    | 6    | 7      | 8     | 9      | 10     |
|---|--------|--------|--------|-------|------|------|--------|-------|--------|--------|
| A | VDD    | B0TX-  | B0TX+  | VDD   | SCL  | SDA  | VDD    | B0RX+ | B0RX-  | VDD    |
| B | A1RX+  | GND    | GND    | A0RX- | DE_A | VDD  | A0TX-  | GND   | GND    | A1TX+  |
| C | A1RX-  | GND    | GND    | A0RX+ | NC   | PD#  | A0TX+  | GND   | GND    | A1TX-  |
| D | VDD    | B1TX+  | B1TX-  | VDD   | D2_A | GND  | VDD    | B1RX- | B1RX+  | VDD    |
| E | SEL0_A | SEL1_A | SEL2_A | GND   | D1_A | S0_A | NC     | S1_A  | SIG_A  | NC     |
| F | NC     | SIG_B  | S1_B   | NC    | S0_B | A1   | SEL2_B | LB#   | SEL1_B | SEL0_B |
| G | VDD    | A2RX-  | A2RX+  | VDD   | MODE | GND  | VDD    | A2TX+ | A2TX-  | VDD    |
| H | B2TX+  | GND    | GND    | B3TX- | DE_B | A0   | B3RX-  | GND   | GND    | B2RX+  |
| J | B2TX-  | GND    | GND    | B3TX+ | NC   | D1_B | B3RX+  | GND   | GND    | B2RX-  |
| K | VDD    | A3RX+  | A3RX-  | VDD   | D2_B | A4   | VDD    | A3TX- | A3TX+  | VDD    |

## Pin Description

| Pin #                  | Pin Name        | Type   | Description  |
|------------------------|-----------------|--------|--|
| <b>Data Signals</b>    |                 |        |  |
| C4<br>B4               | A0RX+,<br>A0RX- | I<br>I | CML inputs for Channel A0, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0). |
| C7<br>B7               | A0TX+,<br>A0TX- | O<br>O | CML outputs for Channel A0, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).  |
| B1<br>C1               | A1RX+,<br>A1RX- | I<br>I | CML inputs for Channel A1, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0). |
| B10<br>C10             | A1TX+,<br>A1TX- | O<br>O | CML outputs for Channel A1, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).  |
| G3<br>G2               | A2RX+,<br>A2RX- | I<br>I | CML inputs for Channel A2, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0). |
| G8<br>G9               | A2TX+,<br>A2TX- | O<br>O | CML outputs for Channel A2, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).  |
| K2<br>K3               | A3RX+,<br>A3RX- | I<br>I | CML inputs for Channel A3 with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0).  |
| K9<br>K8               | A3TX+,<br>A3TX- | O<br>O | CML outputs for Channel A3, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).  |
| A8<br>A9               | B0RX+,<br>B0RX- | I<br>I | CML inputs for Channel B0, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0). |
| A3<br>A2               | B0TX+,<br>B0TX- | O<br>O | CML outputs for Channel B0, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).  |
| D9<br>D8               | B1RX+,<br>B1RX- | I<br>I | CML inputs for Channel B1, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0). |
| D2<br>D3               | B1TX+,<br>B1TX- | O<br>O | CML outputs for Channel B1, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).  |
| H10<br>J10             | B2RX+,<br>B2RX- | I<br>I | CML inputs for Channel B2, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0). |
| H1<br>J1               | B2TX+,<br>B2TX- | O<br>O | CML outputs for Channel B2, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).  |
| J7<br>H7               | B3RX+,<br>B3RX- | I<br>I | CML inputs for Channel B3, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0). |
| J4<br>H4               | B3TX+,<br>B3TX- | O<br>O | CML outputs for Channel B3, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).  |
| <b>Control Signals</b> |                 |        |  |
| H6, F6, K6             | A0, A1, A4      | I      | I <sup>2</sup> C programmable address bit A0, A1 and A4 with 100K-Ohm internal pull up                       |
| E5<br>D5               | D1_A<br>D2_A    | I      | Selection pins for Channel Ax de-emphasis (See de-emphasis Configuration Table) w/ 100K-Ohm internal pull up |

| Pin #  | Pin Name        | Type | Description   |
|--|-----------------|------|---|
| J6<br>K5   | D1_B<br>D2_B    | I    | Selection pins for Channel Bx de-emphasis (See de-emphasis Configuration Table) w/ 100K-Ohm internal pull up  |
| B5   | DE_A            | I    | De-emphasis enable input for Channel A0, A1, A2 and A3 with internal 100K-Ohm pull-up resistor. Set high selects output pre-de-emphasis and set low selects output de-emphasis.   |
| H5   | DE_B            | I    | De-emphasis enable input for Channel B0, B1, B2 and B3 with internal 100K-Ohm pull-up resistor. Set high selects output pre-de-emphasis and set low selects output de-emphasis.   |
| F8   | LB#             | I    | Input with internal 100K-Ohm pull-up resistor. LB# = High or open for normal operation. LB# = Low for loopback connection of A_RX to A_TX and B_TX.   |
| G5   | MODE            | I    | Input switch between pin control and I <sup>2</sup> C control with internal 100k-ohm pull-up resistor. A LVCMOS high level selects input pin control, and disables I <sup>2</sup> C operation. Note, during startup, input status of the control pin (LB#, PD#, SEL0-2_A/B, D1-2_A/B, S0-1_A/B, DE_A/B) will be latched to the initial state of some I <sup>2</sup> C control bits only once. |
| C5, E7, E10, F1, F4, J5  | NC              |      | Do Not Connect (Reserved for future use.)   |
| C6   | PD#             | I    | Input with internal 100K-Ohm pull-up resistor, PD# =High or open is normal operation, PD# =Low disable the IC, and set IC to power down mode, both input and output go Hi-Z.  |
| E6<br>E8   | S0_A<br>S1_A    | I    | Selection pins for Channel Ax output level (see Output Swing Configuration Table) w/ 100K-Ohm internal pull up  |
| F5<br>F3   | S0_B<br>S1_B    | I    | Selection pins for Channel Bx output level (see Output Swing Configuration Table) w/ 100K-Ohm internal pull up  |
| A5   | SCL             | I    | I <sup>2</sup> C SCL clock input. Up to 3.3V input tolerance.   |
| A6   | SDA             | I/O  | I <sup>2</sup> C SDA data input/output. Up to 3.3V input tolerance  |
| E1, E2, E3   | SEL[0:2]_A      | I    | Selection pins for Channel Ax Equalization (see Equalizer Configuration Table) w/ 100K-Ohm internal pull up   |
| F10, F9, F7  | SEL[0:2]_B      | I    | Selection pins for Channel Bx Equalization (see Equalizer Configuration Table) w/ 100K-Ohm internal pull up   |
| E9   | SIG_A           | O    | Signal detect output pin for Channel A0. SIG_A=High represents a input signal > threshold at the differential inputs.   |
| F2   | SIG_B           | O    | Signal detect output pin for Channel B0. SIG_B=High represents a input signal > threshold at the differential inputs.   |
| <b>Power Pins</b>  |                 |      |   |
| B2, B3, B8, B9, C2, C3,<br>C8, C9, D6, E4, G6, H2,<br>H3, H8, H9, J2, J3, J8, J9 | GND             | PWR  | Supply Ground   |
| A1, A4, A7, A10, B6, D1,<br>D4, D7, D10, G1, G4, G7,<br>G10, K1, K4, K7, K10     | V <sub>DD</sub> | PWR  | 1.2V Supply Voltage   |

## DESCRIPTION of OPERATION

### Configuration Modes

Device configuration can be performed in two ways depending on the state of the MODE input. MODE determines whether IC configuration is from the input pins or via I<sup>2</sup>C control. Note that the MODE pin is not latched, and is always active to enable or disable I<sup>2</sup>C access. When MODE is set high, the configuration input pins determine the configuration operating state and changes to the input configuration pins will change the operating mode.

When the MODE pin is low, programming of all control registers via I<sup>2</sup>C is allowed. During initial power-on, the value at the configuration input pins: LB#, PD#, DE\_A, DE\_B, SEL0\_A, SEL1\_A, SEL2\_A, D1\_A, D2\_A, S0\_A, S1\_A, SEL0\_B, SEL1\_B, SEL2\_B, D1\_B, D2\_B, S0\_B, S1\_B, will be latched to the configuration registers as initial startup states.

### Equalizer Configuration

The PI2EQX6814 input equalizer compensates for signal attenuation and Inter-Symbol Interference (ISI) resulting from long signal traces or cables, vias, signal crosstalk and other factors, by boosting the gain of high-frequency signal components. Because either too little, or too much, signal compensation may be non-optimal eight levels are provided to adjust for any application.

Equalizer configuration is performed in two ways determined by the state of the MODE pin. When the device first powers up, the SELx\_[A:B] input pins are read into the appropriate control registers to set the equalization characteristic. If the MODE pin is low, reprogramming of these control registers via I<sup>2</sup>C is allowed.

Each group of four channels, A and B, has separate equalization control, and all four channels within the group are assigned the same configuration state. The Equalizer Selection table below describes pin strapping options and associated operation of the equalizer. Refer to the section on I<sup>2</sup>C programming for information on software configuration of the equalizer.

### Equalizer Selection

| SEL2_[A:B] | SEL1_[A:B] | SEL0_[A:B] | @1.5GHz | @3.0GHz |
|------------|------------|------------|---------|---------|
| 0          | 0          | 0          | 0.8dB   | 1.5dB   |
| 0          | 0          | 1          | 1.0dB   | 1.9dB   |
| 0          | 1          | 0          | 1.5dB   | 3.2dB   |
| 0          | 1          | 1          | 2.5dB   | 5.2dB   |
| 1          | 0          | 0          | 3.5dB   | 6.9dB   |
| 1          | 0          | 1          | 4.4dB   | 8.3dB   |
| 1          | 1          | 0          | 5.9dB   | 10.4dB  |
| 1          | 1          | 1          | 8.7dB   | 13.8dB  |

## Output Configuration

The PI2EQX6814 provides flexible output swing and de-emphasis controls to provide the optimum signal to pre-compensate for losses across long trace or noisy environments so that the receiver gets a clean eye opening. In MODE = I (Input pin Control), Control of output configuration is grouped for the A and B channels, so that each channel within the group has the same setting. In MODE = 0 (I<sup>2</sup>C control), each channel is independently controlled for output swing and output de-emphasis.

## Output Swing Control

When the device first powers up, the S[ 1:0]\_X = 00 is set. If the MODE pin is low, reprogramming of these control registers Bit 2 and 1 of Byte 5,6, 7, 8, 9, 10, 11,12 control register via I<sup>2</sup>C is allowed on a per channel basis.

| S1_[A:B] | S0_[A:B] | Swing (Differential)                |
|----------|----------|-------------------------------------|
| 0        | 0        | 1.1V (Available for Pin Strap only) |
| 0        | 1        | 0.5V                                |
| 1        | 0        | 0.8V                                |
| 1        | 1        | 1.0V                                |

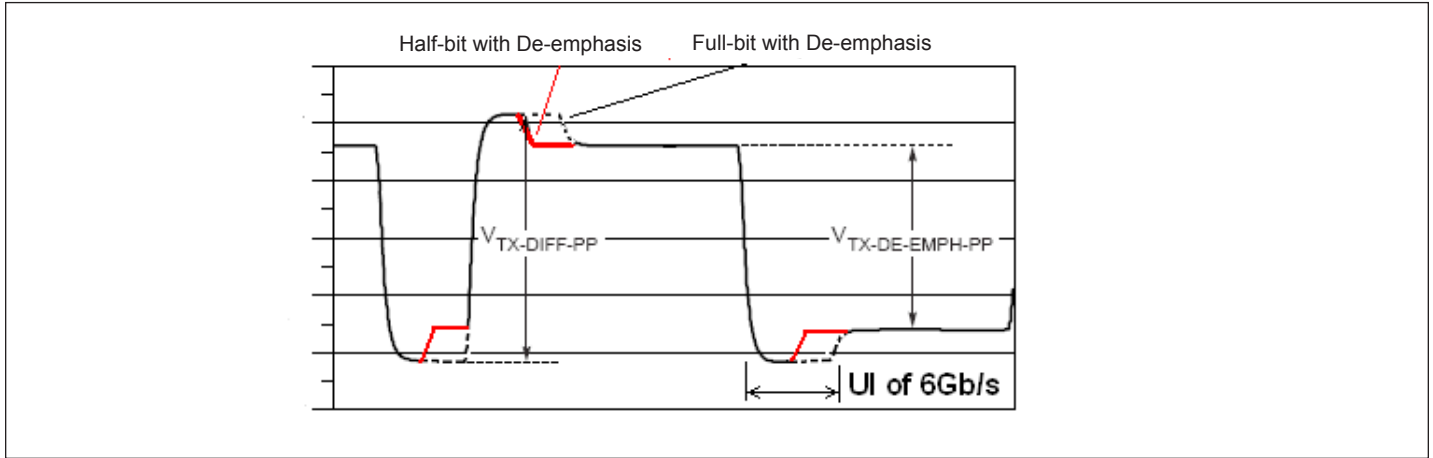
The Output Swing Control table shows available configuration settings for output level control, as specified using registers. Output swing settings are independant of the data rate.

## Output De-emphasis Width Adjustment

De-emphasis settings are determined by the state of the configuration registers (Bits 4, 3 of control Registers 5, 6, 7, 8, 9, 10, 11, 12) or pins D1\_A, D2\_A, D1\_B, D2\_B, as shown in the Output De-emphasis Adjustment table below. De-emphasis-half-bit is selected as the default power-on mode, but can be changed to De-emphasis-full-bit via reprogramming the Loopback and De-emphasis Control register (Bit 2 and 3 of Byte 2) using the I2C interface. Output De-emphasis settings are independant of the data rate.

### Output De-emphasis Adjustment

| D2_[A:B] | D1_[A:B] | De-emphasis |
|----------|----------|-------------|
| 0        | 0        | 2.5dB       |
| 0        | 1        | 4.5dB       |
| 1        | 0        | 6.5dB       |
| 1        | 1        | 8.5dB       |



Choice of half-bit or full-bit de-emphasis depends on the need for more de-emphasis (longer trace) or less de-emphasis (shorter trace) respectively.

### Input Level Detect

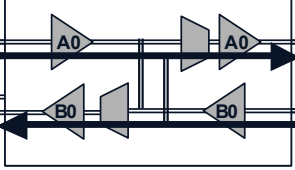
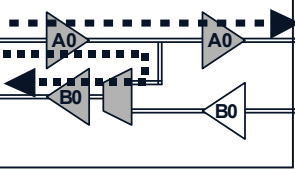
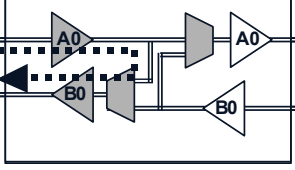
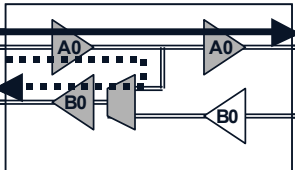
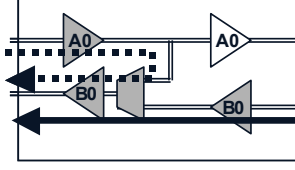
An input level detect and output squelch function is provided on each channel to eliminate re-transmission of input noise. A continuous signal level below the  $V_{th}$  threshold causes the output driver to drive both the plus and minus signal pair to the common mode voltage.

The input sensitivity can be adjusted via the input level threshold register for special requirements.

### Input Threshold Configuration

| Bit | Threshold (mVppd) |
|-----|-------------------|
| 7   | 180               |
| 6   | 160               |
| 5   | 140               |
| 4   | 120 (Default)     |
| 3   | 100               |
| 2   | 80                |
| 1   | 60                |
| 0   | 40                |

## Loopback Operation

| Loopback Modes   | CONDITIONS   |
|--|--|
|  <p>NORMAL MODE<br/>A0Rx to A0Tx, B0Rx to B0Tx</p>  | LB_A0B0# = 1<br>INDIS_A0 = 0<br>OUTDIS_A0 = 0<br>INDIS_B0 = 0<br>OUTDIS_B0 = 0 |
|  <p>BROADCAST MODE<br/>A0Rx to A0Tx and B0Tx</p>  | LB_A0B0# = 0<br>INDIS_A0 = 0<br>OUTDIS_A0 = 0<br>INDIS_B0 = 1<br>OUTDIS_B0 = 0 |
|  <p>LOOPBACK MODE<br/>A0Rx to B0Tx</p>  | LB_A0B0# = 0<br>INDIS_A0 = 0<br>OUTDIS_A0 = 1<br>INDIS_B0 = 1<br>OUTDIS_B0 = 0 |
|  <p>DEMUX MODE<br/>Solid Line<br/>A0Rx to A0Tx</p> <p>DEMUX MODE<br/>Dashed Line<br/>A0Rx to B0Tx</p> | LB_A0B0# = 1<br>INDIS_A0 = 0<br>OUTDIS_A0 = 0<br>INDIS_B0 = 1<br>OUTDIS_B0 = 1 |
|  | LB_A0B0# = 0<br>INDIS_A0 = 0<br>OUTDIS_A0 = 1<br>INDIS_B0 = 1<br>OUTDIS_B0 = 0 |
|  <p>MUX MODE<br/>Solid Line<br/>B0Rx to B0Tx</p> <p>MUX MODE<br/>Dashed Line<br/>A0Rx to B0Tx</p>     | LB_A0B0# = 1<br>INDIS_A0 = 1<br>OUTDIS_A0 = 1<br>INDIS_B0 = 0<br>OUTDIS_B0 = 0 |
|  | LB_A0B0# = 0<br>INDIS_A0 = 0<br>OUTDIS_A0 = 1<br>INDIS_B0 = 1<br>OUTDIS_B0 = 0 |

Each lane provides a loopback mode for test purposes which is controlled by a strapping pin and I<sup>2</sup>C register bit. The LB# pin controls all lanes together. When this pin is high normal data mode is enabled. When LB# is low the loopback feature is enabled. The adjacent figure diagrams this operation. Loopback is not intended to be dynamically switched, and the normal system application is to initialize to one configuration or the other.

The Loopback mode can also support mux/demux operation. Using I<sup>2</sup>C configuration, unused inputs and outputs can be disabled to minimize power and noise.

## I<sup>2</sup>C Operation

The integrated I<sup>2</sup>C interface operates as a slave device, supporting standard rate operation of 100Kbps, with 7-bit addressing mode. The data byte format is 8 bit bytes, and supports the format of indexing to be compatible with other bus devices. The index, or dummy byte will have no effect on the PI2EQX6814 operation. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred. Address bits A4, A1 and A0 are programmable to support multiple chips environment. The Data is loaded until a Stop sequence is issued.

Note that the I<sup>2</sup>C inputs, SCL and SDA operate at 1.2V logic levels, and are 3.3V tolerant.

## Configuration Register Summary

| Byte | Mnemonic | Function  |
|------|----------|---|
| 0    | SIG      | Signal Detect, indicates valid input signal level   |
| 1    | RSVD     | Reserved for future use   |
| 2    | LBEC     | Loopback and De-emphasis Control, provides for control of the loopback function and de-emphasis mode (pre-de-emphasis or de-emphasis) |
| 3    | INDIS    | Channel Input Disable, controls whether s channels input buffer is enabled or disabled  |
| 4    | OUTDIS   | Channel Output Disable, controls whether a channel output buffer is enabled or disabled.  |
| 5    | A0       | Channel A0 configuration  |
| 6    | B0       | Channel B0 configuration  |
| 7    | A1       | Channel A1 configuration  |
| 8    | B1       | Channel B1 configuration  |
| 9    | A2       | Channel A2 configuration  |
| 10   | B2       | Channel B2 configuration  |
| 11   | A3       | Channel A3 configuration  |
| 12   | B3       | Channel B3 configuration  |
| 13   | VTH      | Input level threshold configuration   |
| 14   | RSVD     | Reserved for future use   |



## Register Description

### BYTE 0 - Signal Detect (SIG)

SIG<sub>xy</sub>=0=low input signal, SIG<sub>xy</sub>=1=valid input signal

| Bit            | 7             | 6             | 5             | 4             | 3             | 2             | 1             | 0             |
|----------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| <b>Name</b>    | <b>SIG_A0</b> | <b>SIG_B0</b> | <b>SIG_A1</b> | <b>SIG_B1</b> | <b>SIG_A2</b> | <b>SIG_B2</b> | <b>SIG_A3</b> | <b>SIG_B3</b> |
| Type           | R             | R             | R             | R             | R             | R             | R             | R             |
| Power-on State | X             | X             | X             | X             | X             | X             | X             | X             |

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Signal Detect register provides information on the instantaneous status of the channel input from the Input Level Threshold Detect circuit. If the input level falls below the V<sub>th</sub>- level the relevant SIG<sub>xy</sub> bit will be 0, indicating a low-level noise or electrical idle input, resulting in the outputs going to the high-impedance off state or squelch mode. If the input level is above V<sub>th</sub>-, then SIG<sub>xy</sub> is 1, indicating a valid input signal, and active signal recovery operation.

### BYTE 1 - Reserved

Reserved Byte 1 is visible via the I<sup>2</sup>C interface. This is a read-only byte with an undefined initial state after power-up. This byte is reserved for future use.

### BYTE 2 - Loopback and De-emphasis Control Register (LBEC)

LB<sub>xyxy</sub>#=0=loopback mode, LB<sub>xyxy</sub>#=1=normal mode,

Slumber = 1 = auto-power down slumber enabled,

Slumber = 0 = auto power down disabled

DE<sub>x</sub> = 0 Full-bit de-emphasis, DE<sub>x</sub> = 1 Half-bit de-emphasis,

| Bit            | 7               | 6               | 5               | 4               | 3           | 2           | 1              | 0             |
|----------------|-----------------|-----------------|-----------------|-----------------|-------------|-------------|----------------|---------------|
| <b>Name</b>    | <b>LB_A0B0#</b> | <b>LB_A1B1#</b> | <b>LB_A2B2#</b> | <b>LB_A3B3#</b> | <b>DE_A</b> | <b>DE_B</b> | <b>Slumber</b> | <b>Bypass</b> |
| Type           | R/W             | R/W             | R/W             | R/W             | R/W         | R/W         | R/W            | R/W           |
| Power-on State | LB#             | LB#             | LB#             | LB#             | DE_A        | DE_B        | 1              | 0             |

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

Individual control for each lane is provided for the loopback function via this register. Slumber mode, auto power down for all channels is enabled by slumber. For details on Full-bit de-emphasis and Half-bit de-emphasis, refer to Output De-emphasis Width Adjustment section description. Bypass is for IC manufacturing test only, and should always be set to "0" for normal operation.

### BYTE 3 - Channel Input Disable (INDIS)

INDIS\_xy=0=enable input, INDIS\_xy=1=disable input

| Bit            | 7               | 6               | 5               | 4               | 3               | 2               | 1               | 0               |
|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| <b>Name</b>    | <b>INDIS_A0</b> | <b>INDIS_B0</b> | <b>INDIS_A1</b> | <b>INDIS_B1</b> | <b>INDIS_A2</b> | <b>INDIS_B2</b> | <b>INDIS_A3</b> | <b>INDIS_B3</b> |
| Type           | R/W             | R/W             | R/W             | R/W             | R/W             | R/W             | R/W             | R/W             |
| Power-on State | 0               | 0               | 0               | 0               | 0               | 0               | 0               | 0               |

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Channel Input Disable register, provides control over the input buffer of each channel independently. When and INDIS\_xy bit is logic 1, then the input buffer is switched off and the input termination is high impedance. This feature can be used for PCB testing, and when only one input is used during Loopback as a demux function. When INDIS\_xy is at a logic 0 state then the input buffer is enabled (normal operating mode).

### BYTE 4 - Channel Output Disable (OUTDIS)

ODIS\_xy=0=enable output, ODIS\_xy=1=disable output

| Bit            | 7              | 6              | 5              | 4              | 3              | 2              | 1              | 0              |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| <b>Name</b>    | <b>ODIS_A0</b> | <b>ODIS_B0</b> | <b>ODIS_A1</b> | <b>ODIS_B1</b> | <b>ODIS_A2</b> | <b>ODIS_B2</b> | <b>ODIS_A3</b> | <b>ODIS_B3</b> |
| Type           | R/W            | R/W            | R/W            | R/W            | R/W            | R/W            | R/W            | R/W            |
| Power-on State | 0              | 0              | 0              | 0              | 0              | 0              | 0              | 0              |

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Channel Output Disable register, allows control over the output buffer of each channel independently. When and OUTDIS\_xy bit is logic 1, then the output buffer is switched off and the termination is high impedance. This feature can be used for PCB testing, and when only one output is used during Loopback as a mux function. When INDIS\_xy is at a logic 0 state then the input buffer is enabled (normal operating mode).

**BYTE 5 - A0 Channel Configuration**

**BYTE 6 - B0 Channel Configuration**

**BYTE 7 - A1 Channel Configuration**

**BYTE 8 - B1 Channel Configuration**

**BYTE 9 - A2 Channel Configuration**

**BYTE 10 - B2 Channel Configuration**

**BYTE 11 - A3 Channel Configuration**

**BYTE 12 - B3 Channel Configuration**

SEL<sub>x</sub>\_B: Equalizer configuration (see Equalizer Configuration Table)

Dx\_B: De-emphasis control (see De-emphasis Configuration Table)

Sx\_B: Output level control (see Output Swing Configuration Table)

| Bit            | 7              | 6              | 5              | 4            | 3            | 2            | 1            | 0          |
|----------------|----------------|----------------|----------------|--------------|--------------|--------------|--------------|------------|
| <b>Name</b>    | <b>SEL0_XX</b> | <b>SEL1_XX</b> | <b>SEL2_XX</b> | <b>D1_XX</b> | <b>D2_XX</b> | <b>S0_XX</b> | <b>S1_XX</b> | <b>PD#</b> |
| Type           | R/W            | R/W            | R/W            | R/W          | R/W          | R/W          | R/W          | R/W        |
| Power-on State | SEL0_XX        | SEL1_XX        | SEL2_XX        | D1_XX        | D2_XX        | S0_XX        | S1_XX        | PD#        |

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Ax/Bx-Channel configuration registers are used to control the input equalizer and output de-emphasis, swing levels and power-down. These register bits are loaded from the input configuration pins of the same name at power-on. These bits may be changed if the PGM# input is set low to allow I<sup>2</sup>C configuration. Please refer to the tables (1) Equalizer Configuration, (2) Output Swing Configuration and (3) Output De-emphasis Configuration earlier in this document for setting information.

**BYTE 13 - Input Level Threshold Configuration**

| Bit            | 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
|----------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| <b>Name</b>    | <b>VTH7</b> | <b>VTH6</b> | <b>VTH5</b> | <b>VTH4</b> | <b>VTH3</b> | <b>VTH2</b> | <b>VTH1</b> | <b>VTH0</b> |
| Type           | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         |
| Power-on State | 1           | 1           | 1           | 0           | 1           | 1           | 1           | 1           |

Note:

R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

Only 1 bit can be enabled at a time

0 = enable level, 1 = disable level,

Refer to Input Threshold Table for configuration information.

**BYTE 14 - Reserved**

Reserved Byte 14 is visible via the I<sup>2</sup>C interface. This byte is R/W, is in an undefined state at power up, and should not be changed for normal operation.

## Transferring Data

Every byte put on the SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I<sup>2</sup>C Data Transfer diagram). The PI2EQX6814 will never hold the clock line SCL LOW to force the master into a wait state.

Note: Byte-write and byte-read transfers have a fixed offset of 0x00, because of the very small number of configuration bytes. An offset byte presented by a host to the PI2EQX6814 is not used.

## Addressing

Up to eight PI2EQX6814 devices can be connected to a single I<sup>2</sup>C bus. The PI2EQX6814 supports 7-bit addressing, with the LSB indicating either a read or write operation. The address for a specific device is determined by the A0, A1 and A4 input pins.

| Address Assignment |    |         |    |    |              |    |          |
|--------------------|----|---------|----|----|--------------|----|----------|
| A6                 | A5 | A4      | A3 | A2 | A1           | A0 | R/W      |
| 1                  | 1  | Program | 0  | 0  | Programmable |    | 1=R, 0=W |

## Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, the PI2EQX6814 will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I<sup>2</sup>C Data Transfer diagram. The PI2EQX6814 will generate an acknowledge after each byte has been received.

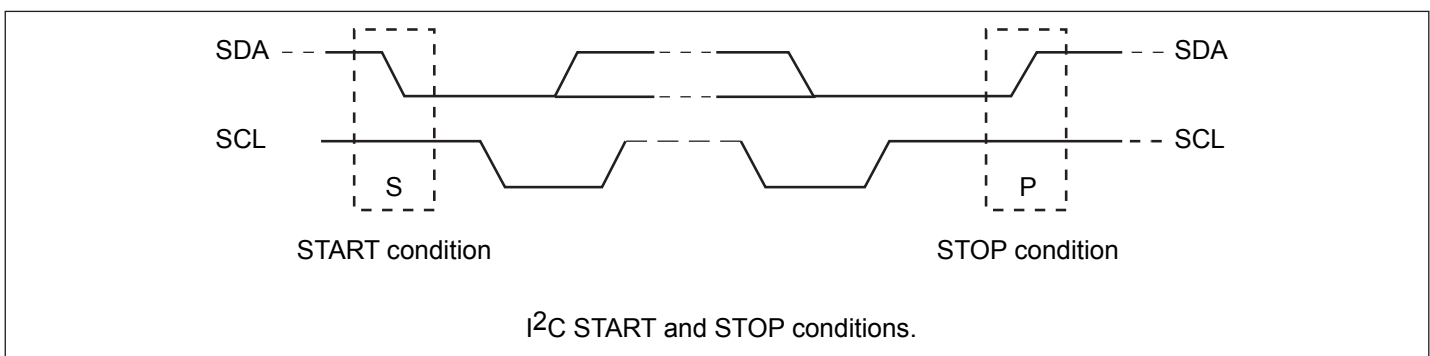
## Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, the PI2EQX6814 will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. For a write cycle, the first data byte following the address byte is a dummy or fill byte that is not used by the PI2EQX6814. This byte is provided to provided compatibility with systems implementing 10-bit addressing. Data is transferred with the most significant bit (MSB) first.

## I<sup>2</sup>C Data Transfer

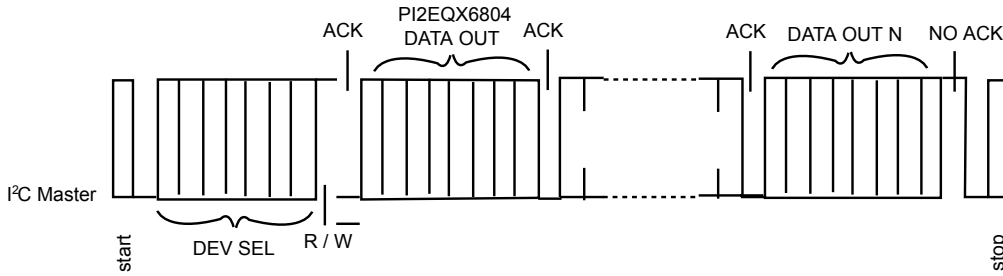
### Start & Stop Conditions

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below.

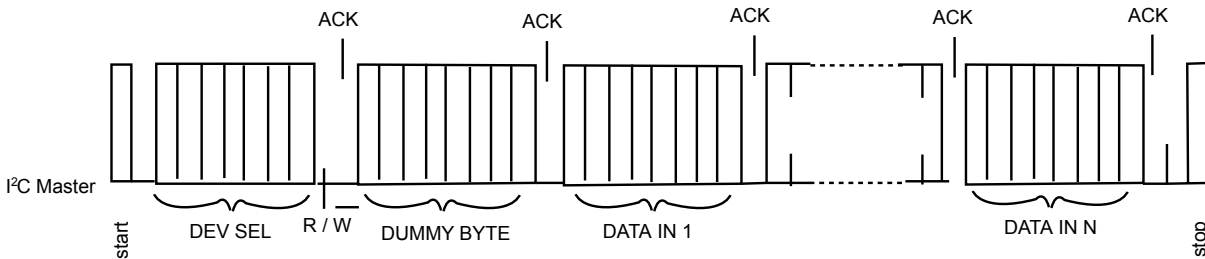


**I<sup>2</sup>C Data Transfer**

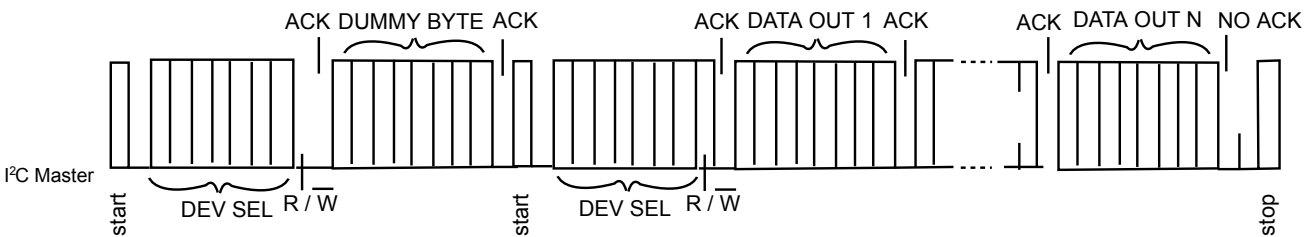
1. Read sequence



2. Write sequence



3. Combined sequence



Notes:

1. only block read and block write from the lowest byte are supported for this application.
2. for some I2C application, an offset address byte will be presented at the second byte in write command, which is called dummy byte here and will be simply ignored in this application for correct interoperation.

### Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

|  |                    |
|--|--------------------|
| Storage Temperature . . . . .                | -65°C to +150°C    |
| Supply Voltage to Ground Potential . . . . . | -0.5V to +2.5V     |
| DC SIG Voltage . . . . .                     | -0.5V to VDD +0.5V |
| Current Output . . . . .                     | -25mA to +25mA     |
| Power Dissipation Continuous . . . . .       | 1W                 |
| Operating Temperature . . . . .              | -40 to +85°C       |
| ESD, HBM, . . . . .                          | -2kV to +2kV       |

Note:  
 Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Power Supply Characteristics (V<sub>DD</sub> = 1.2V ± 5%, T<sub>A</sub> = -40 TO 85°C)

| Symbol                  | Parameter                                   | Conditions                        | Min. | Typ. | Max. | Units |
|-------------------------|---|-----------------------------------|------|------|------|-------|
| I <sub>DDactive</sub>   | Power supply current - active               | All channels switching @ 6.5 Gbps |      |      | 900  | mA    |
| I <sub>DDstandby</sub>  | Power supply current - standby              | PD# = 0                           |      | 1    | 5    |       |
| I <sub>DDslumber</sub>  | Power supply current - per channel, Slumber |                                   |      | 10   |      |       |
| I <sub>DD-channel</sub> | Power supply current - per channel, Active  |                                   |      | 95   |      |       |

### AC Performance Characteristics (V<sub>DD</sub> = 1.2V ± 5%, T<sub>A</sub> = -40 TO 85°C)

| Symbol          | Parameter                            | Conditions | Min. | Typ. | Max. | Units |
|-----------------|--------------------------------------|------------|------|------|------|-------|
| T <sub>pd</sub> | Channel latency from input to output |            |      | 750  |      | ps    |

**CML Receiver Input** ( $V_{DD} = 1.2V \pm 5\%$ ,  $T_A = -40$  TO  $85^\circ\text{C}$ )

| Symbol                    | Parameter                               | Conditions            | Min. | Typ. | Max.               | Units |
|---------------------------|---|-----------------------|------|------|--------------------|-------|
| <b>CML Receiver Input</b> |   |                       |      |      |                    |       |
| $Z_{RX-DC}$               | DC Input Impedance                      |                       | 40   |      |                    | Ohm   |
| $Z_{RX-DIFF-DC}$          | DC Differential Input Impedance         |                       | 85   | 100  | 115                |       |
| $V_{RX-DIFFP-P}$          | Differential Input Peak-to-peak Voltage |                       | 240  |      | 1000               | mV    |
| $V_{RX-CM-ACP}$           | AC Peak Common Mode Input Voltage       |                       |      |      | 100                |       |
| $V_{TH-SD}$               | OOB Signal detect input Threshold       |                       | 75   |      | 200 <sup>(1)</sup> | mVppd |
| <b>Equalization</b>       |   |                       |      |      |                    |       |
| $T_J$                     | Total Jitter                            | Measured at 6Gbps/500 |      |      | 0.37               | Ulp-p |
| $D_J$                     | Deterministic Jitter                    | Measured at 6Gbps/500 |      |      | 0.19               | psrms |

**Note:**

- Using Compliance test at 1.5Gbps and 3Gbps. Also using OOB (OOB is formed by ALIGNp primitive or D24.3) test patterns at 1.5Gbps. The ALIGN primitive (K28.5+D10.2+D27.3 = 0011111010+0101010101+0010011100). The D24.3 = 00110011001100110011

**CML Transmitter Output ( $V_{DD} = 1.2V \pm 5\%$ ,  $T_A = -40$  TO  $85^\circ C$ )**

| Symbol            | Parameter  | Conditions                   | Min. | Typ.           | Max. | Units |
|-------------------|--|------------------------------|------|----------------|------|-------|
| $Z_{TX-DIFF-DC}$  | DC Differential TX Impedance   |                              | 80   | 100            | 120  | Ohms  |
| $V_{TX-DIFFP-P0}$ | Differential Peak-to-peak Output Voltage<br>$V_{TX-DIFFP-P} = 2 *  V_{TX-D+} - V_{TX-D-} $ | S[1:0] = 00, 0dB de-emphasis | 0.9  | 1.1            | 1.3  | V     |
|                   |  | S[1:0] = 01, 0dB de-emphasis | 0.3  | 0.5            | 0.7  |       |
|                   |  | S[1:0] = 10, 0dB de-emphasis | 0.6  | 0.8            | 1    |       |
|                   |  | S[1:0] = 11, 0dB de-emphasis | 0.8  | 1              | 1.2  |       |
| $V_{TX-C}$        | Common-Mode Voltage<br>$ V_{TX-D+} + V_{TX-D-}  / 2$                                       |                              |      | $V_{DD} - 0.6$ |      | V     |
| $t_F, t_R$        | Transition Time  | 20% to 80%                   |      |                | 150  | ps    |
| $t_F - t_R$       | Mismatch Transition Time   | @3Gbps                       |      |                | 35   | %     |
| $V_{amp\_bal}$    | TX amplitude imbalance   | @3Gbps                       |      |                | 10   |       |
| $T_{skew}$        | TX differential skew   |                              |      |                | 20   | ps    |
| $V_{cm\_ac}$      | TX AC common mode voltage  | @3Gbps                       |      |                | 50   | mVpp  |
| $V_{cmOOB}$       | OOB common mode delta voltage  |                              |      |                | 50   | mV    |
| $V_{diffOOB}$     | OOB differential delta voltage   |                              |      |                | 25   |       |



**Digital I/O DC Specifications ( $V_{DD} = 1.2V \pm 5\%$ ,  $T_A = -40$  TO  $85^\circ\text{C}$ )**

| Symbol          | Parameter                           | Conditions             | Min.             | Typ. | Max.             | Units         |
|-----------------|-------------------------------------|------------------------|------------------|------|------------------|---------------|
| $V_{IH}$        | DC input logic high                 |                        | $V_{DD}/2 + 0.2$ |      | $V_{DD} + 0.3$   | V             |
| $V_{IL}$        | DC input logic low                  |                        | -0.3             |      | $V_{DD}/2 - 0.2$ |               |
| $V_{OH}$        | DC output logic high                | $I_{OH} = -4\text{mA}$ | $V_{DD} - 0.4$   |      |                  |               |
| $V_{OL}$        | DC output logic low                 | $I_{OL} = 4\text{mA}$  |                  |      | 0.4              |               |
| $V_{hys}$       | Hysteresis of Schmitt trigger input |                        | 0.1              |      |                  |               |
| $I_{IH}^{(1)}$  | Input high current                  |                        |                  |      | 250              | $\mu\text{A}$ |
| $I_{IL1}^{(2)}$ | Input low current                   |                        | -250             |      |                  |               |
| $I_{IL2}^{(3)}$ | Input low current                   |                        | -250             |      |                  |               |

**Notes:**

1. Includes input signals A1, A2, A4, Dx\_[A:B], DE\_[A:B], LB#, MODE#, PD#, Sx\_[A:B], SCL, SDA, SEL\_x[A:B]
2. For control inputs without pullups: SCL, SDA
3. Control inputs with pull-ups include: Dx\_[A:B], DE\_[A:B], LB#, MODE#, PD#, Sx\_[A:B], SEL\_x[A:B], A1, A2, A4

**SDA and SCL I/O for I<sup>2</sup>C-bus ( $V_{DD} = 1.2V \pm 5\%$ ,  $T_A = -40$  TO  $85^\circ\text{C}$ )**

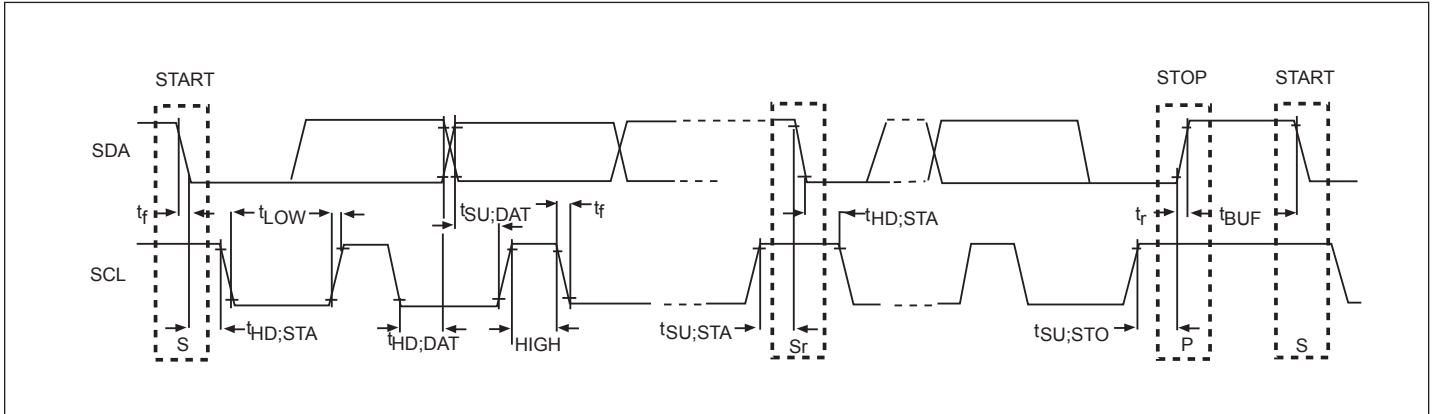
| Symbol    | Parameter                           | Conditions            | Min.                 | Typ. | Max. | Units |
|-----------|-------------------------------------|-----------------------|----------------------|------|------|-------|
| $V_{IH}$  | DC input logic high                 |                       | $0.85 \times V_{DD}$ |      | 3.6  | V     |
| $V_{IL}$  | DC input logic low                  |                       | -0.3                 |      | 0.4  |       |
| $V_{OL}$  | DC output logic low                 | $I_{OL} = 3\text{mA}$ |                      |      | 0.4  |       |
| $V_{hys}$ | Hysteresis of Schmitt trigger input |                       | 0.2                  |      |      |       |

**Characteristics of the SDA and SCL bus lines for Standard Mode I<sup>2</sup>C-bus devices<sup>(1)</sup>**

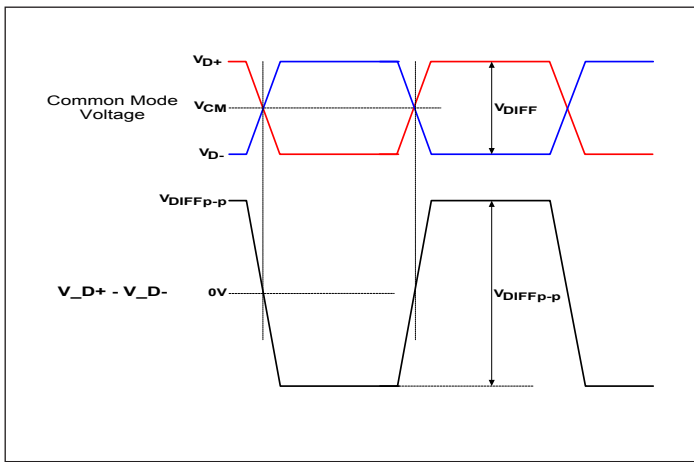
| Symbol              | Parameter  | Conditions | Min. | Typ. | Max. | Units |
|---------------------|--|------------|------|------|------|-------|
| f <sub>SCL</sub>    | SCL clock frequency  |            | 0    |      | 100  | kHz   |
| t <sub>HD;STA</sub> | Hold time (repeated) START condition. After this period, the first clock pulse is generated. |            | 4.0  |      | –    | μs    |
| t <sub>LOW</sub>    | LOW period of the SCL clock  |            | 4.7  |      | –    |       |
| t <sub>HIGH</sub>   | HIGH period of the SCL clock   |            | 4.0  |      | –    |       |
| t <sub>SU;STA</sub> | Set-up time for a repeated START condition   |            | 4.7  |      | –    |       |
| t <sub>HD;DAT</sub> | Data hold time   |            | 10   |      | –    | ns    |
| t <sub>SU;DAT</sub> | Data set-up time   |            | 250  |      | –    | ns    |
| t <sub>r</sub>      | Rise time of both SDA and SCL signals  |            | -    |      | 1000 |       |
| t <sub>f</sub>      | Fall time of both SDA and SCL signals  |            |      |      | 300  |       |
| t <sub>SU;STO</sub> | Set-up time for STOP condition   |            | 4.0  |      | –    | μs    |
| t <sub>BUF</sub>    | Bus free time between a STOP and STOP condition  |            | 4.7  |      | –    |       |
| C <sub>b</sub>      | Capacitive load for each bus line  |            | -    |      | 400  | pF    |

**Notes:**

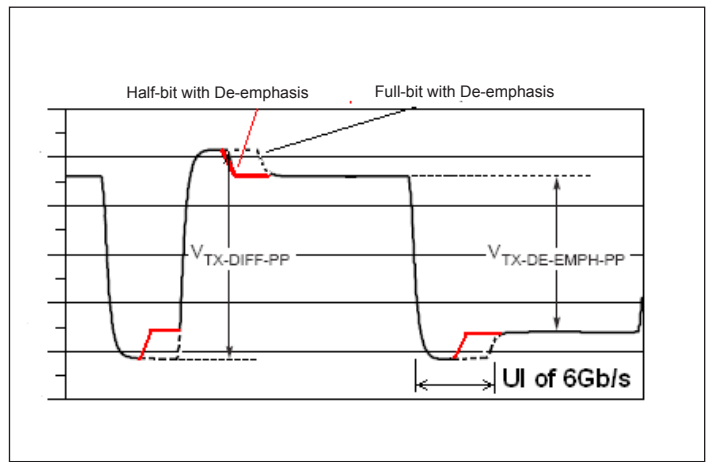
1. All values referred to VIH min and VIL max levels



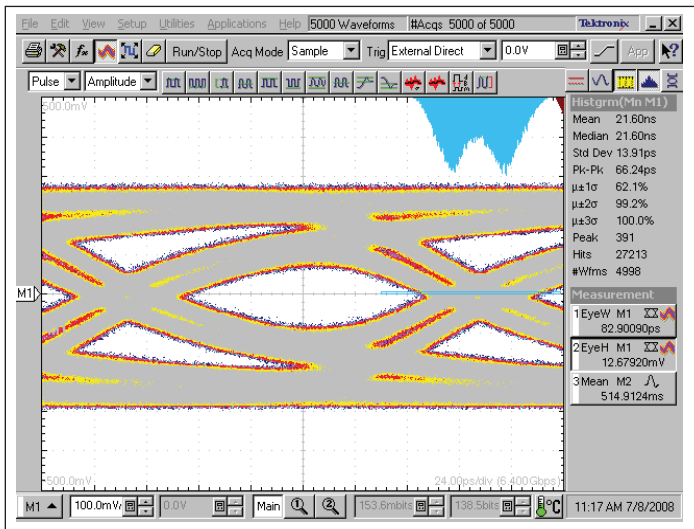
I<sup>2</sup>C Timing



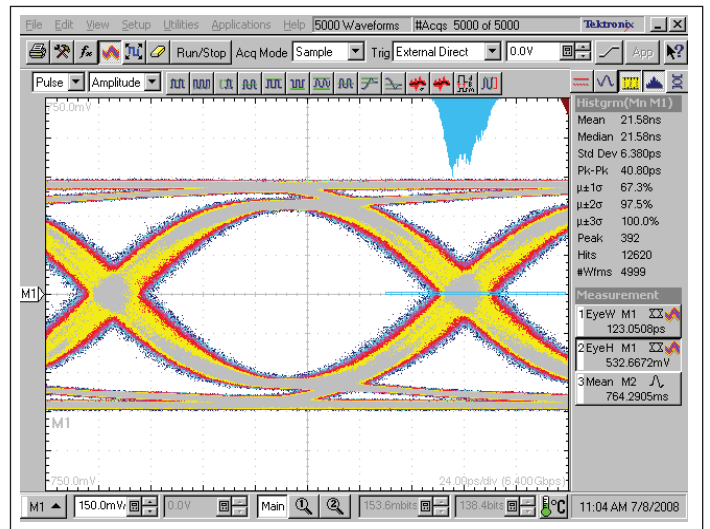
Definition of Differential Voltage and Differential Voltage Peak-to-Peak



Definition of De-emphasis

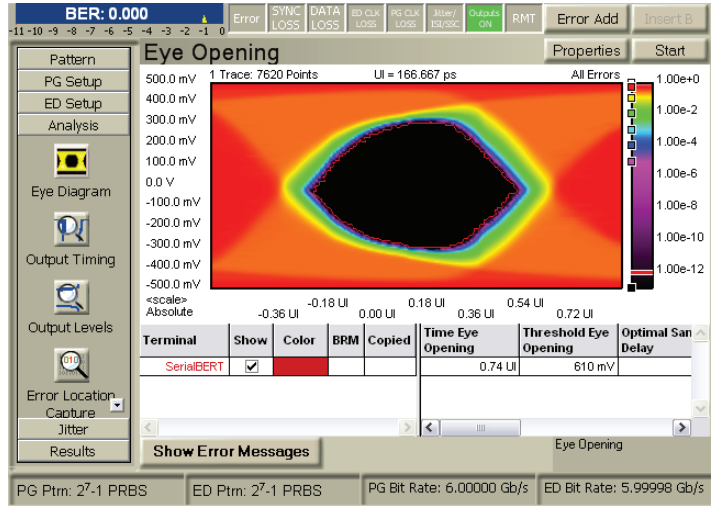
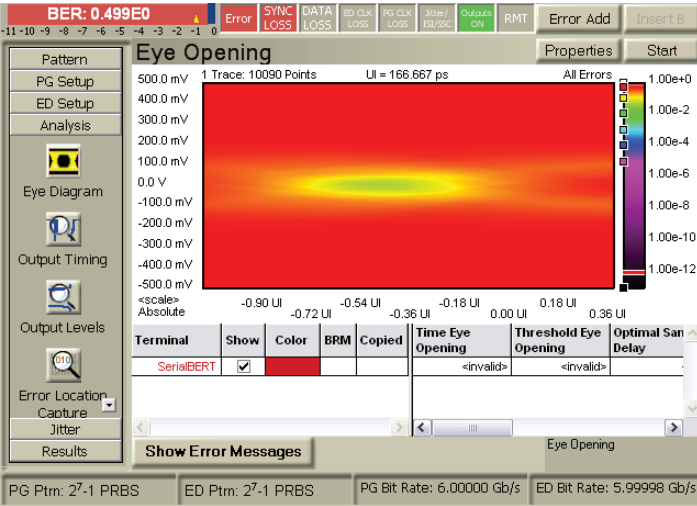


Input Eye



Output Eye

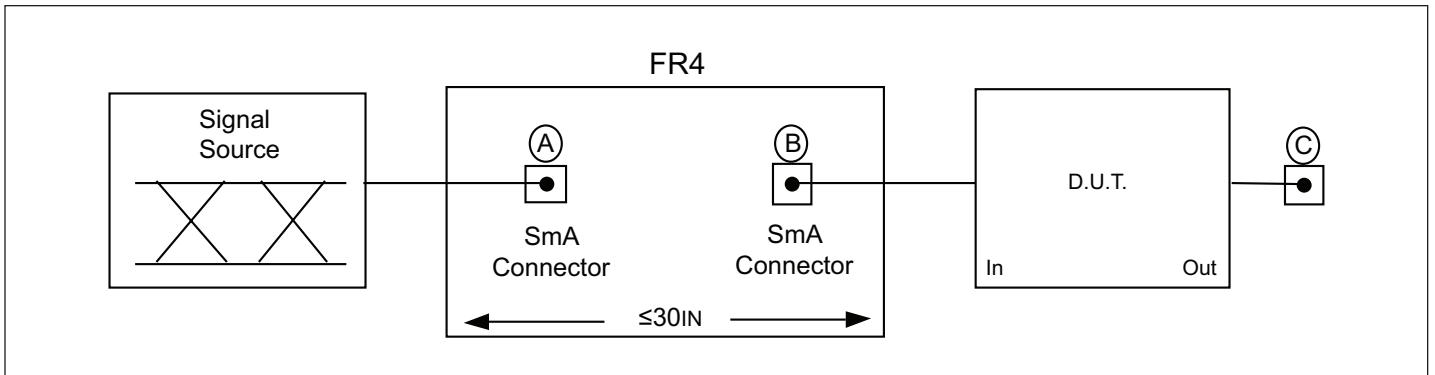
Signal Eyes @10dB input equalization, 24 inch FR4 input trace, 36 inch output cable



Signal Eyes at 13.8dB Input Equalization (EQ=111), 48" FR4 Input Trace and 36" Output Coax cable.

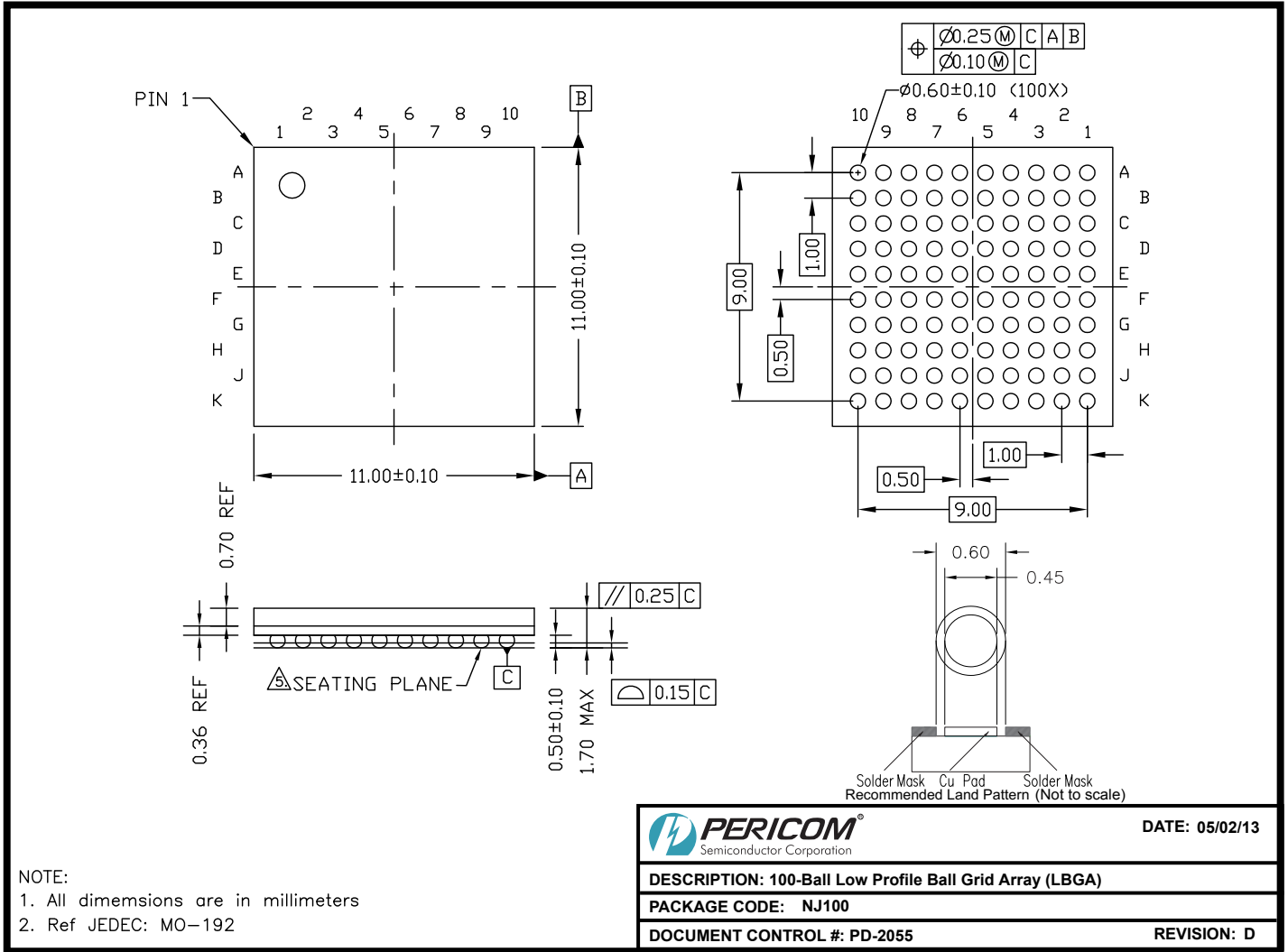


Data Waveforms, 3.0Gbps (left) & 6.0Gbps (right)



AC Test Circuit Referenced in the Electrical Characteristic Table

**Packaging Mechanical: 100-Contact LPGA (NJ)**



NOTE:  
 1. All dimensions are in millimeters  
 2. Ref JEDEC: MO-192

13-0083

Note: For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

**Ordering Information**

| Ordering Number | Package Code | Package Description                         |
|-----------------|--------------|---|
| PI2EQX6814NJE   | NJ           | 100-Ball Low Profile Ball Grid Array (LPGA) |

Notes:

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- E = Pb-free and Green
- X suffix = Tape/Reel