Product Document

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AS3412

Ultra Small ANC Speaker Driver

General Description

The AS3412 is a speaker driver with Ambient Noise Cancelling function for headsets, headphones or ear pieces. They are intended to improve quality of e.g. music listening, a phone conversation etc. by reducing background ambient noise.

The fully analog implementation allows the lowest power consumption, lowest system BOM cost and most natural received voice enhancement otherwise difficult to achieve with DSP implementations. The device is designed to be easily applied to existing architectures.

An internal OTP-ROM can be optionally used to store the microphones gain calibration settings. The AS3412 can be used in different configurations for best trade-off in terms of noise cancellation, required filtering functions and mechanical designs. The AS3412 targeting feed-forward topology is used to effectively reduce frequencies typically up to 2-3 kHz.

The filter loop for the system is determined by measurements, for each specific headset individually, and depends very much on mechanical designs. The gain and phase compensation filter network is implemented with cheap resistors and capacitors for lowest system costs.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of this device are listed below:

Figure 1:
Added Value of Using AS3412

Benefits	Features
• Low noise floor	• Low noise amplifiers
• Integrated music bypass switch	• Depletion mode transistors for passive music bypass
• Smallest ANC form factor	• WL-CSP package (2.2x2.2mm, 0.4mm pitch)

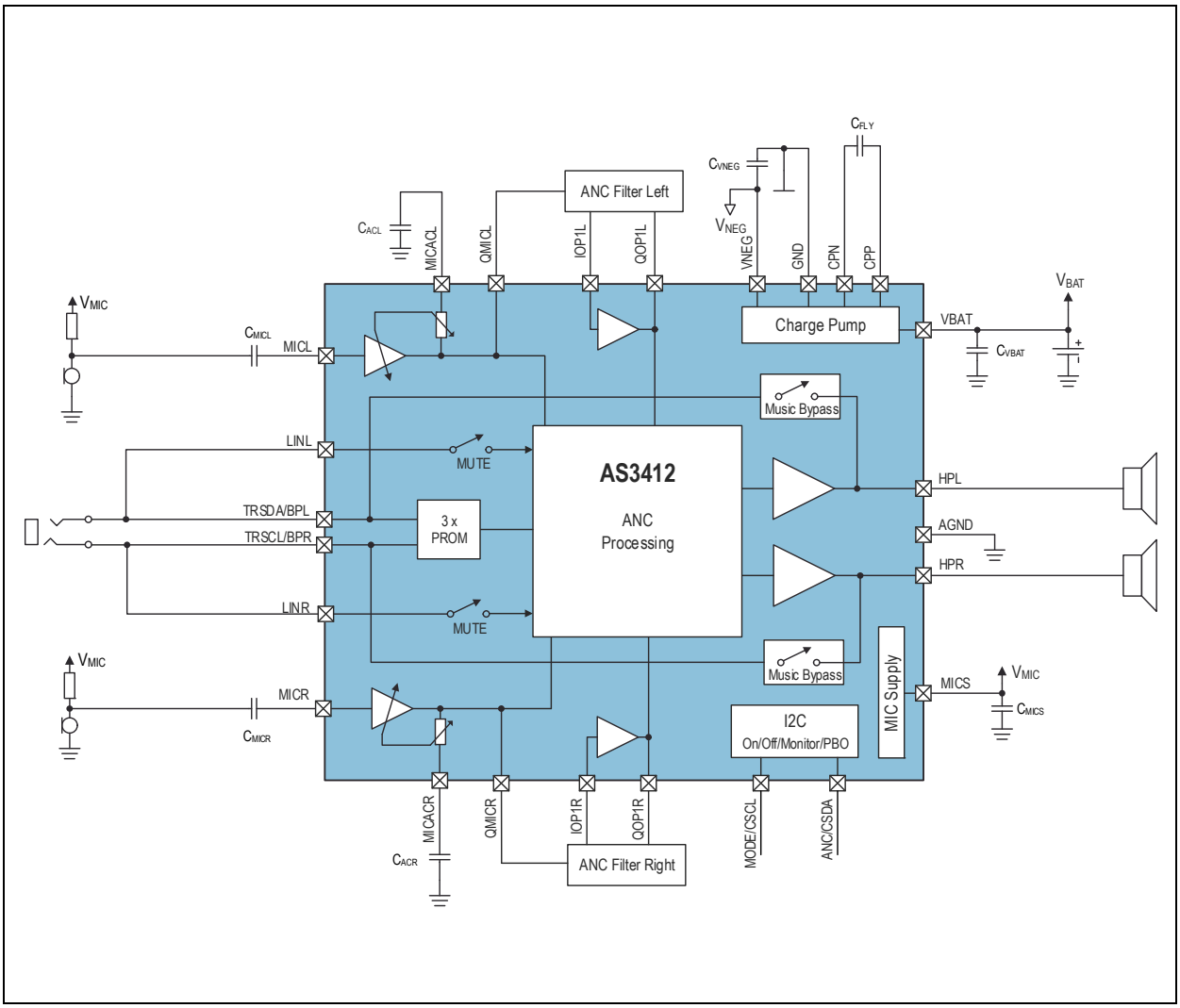
Applications

The devices are ideal for Ear Pieces, Headsets, Hands-Free Kits, Mobile Phones, and Voice Communicating Devices.

Block Diagram

The functional blocks of the AS3412 are shown below:

Figure 2:
Functional Blocks of AS3412

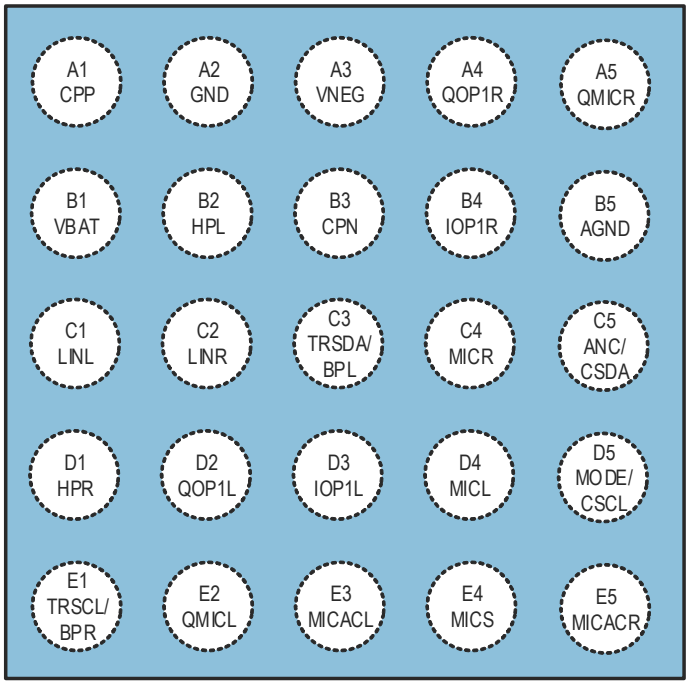


AS3412 Block Diagram: This figure shows the functional blocks of the AS3412.

Pin Assignment

Pin Diagram

Figure 3:
Pin Diagram of AS3412



Pin Description

Figure 4:
AS3412 Pin Assignment

Pin Name	Pin Number	Pin Type	Description
AGND	B5	ANA OUT	Analog reference ground. Has to be connected to GND pin. For better noise performance a star shaped ground concept is the preferred option to connect these pins together.
LINL	C1	ANA IN	Line input EQ left channel.
TRSDA/ BPL	C3	ANA IN/OUT	Data input for production trimming. Can be connected to LINL pin to enable production trimming via 3.5mm audio jack. Furthermore this pin features also music bypass function for the left audio channel in off mode operation in order to replace and external analog switch.

Pin Name	Pin Number	Pin Type	Description
TRSCL/ BPR	E1	ANA IN/OUT	Clock input for production trimming. Can be connected to LINR pin to enable production trimming via 3.5mm audio jack. Furthermore this pin features also music bypass function for the right audio channel in off mode operation in order to replace an external analog switch.
LINR	C2	ANA IN	Line input EQ right channel.
ANC / CSDA	C5	DIG IN	Serial interface data for I^2C interface and ANC control to enable/disable ANC.
MODE / CSCL	D5	DIG IN	Serial Interface Clock for I^2C interface and control pin for power up/down and Monitor mode.
MICACL	E3	ANA OUT	Microphone preamplifier AC coupling ground terminal. This pin requires a 10µF capacitor connected to AGND pin.
MICL	D4	ANA IN	ANC microphone input left channel.
MICS	E4	SUP OUT	Microphone Supply output. This pin needs an output blocking capacitor with 10µF.
MICR	C4	ANA IN	ANC microphone preamplifier input right channel.
MICACR	E5	ANA OUT	Microphone preamplifier AC coupling ground terminal. This pin requires a 10µF capacitor connected to AGND pin.
QMICR	A5	ANA OUT	ANC microphone preamplifier output right channel.
IOP1R	B4	ANA IN	ANC filter OpAmp1 input right channel.
QOP1R	A4	ANA OUT	ANC filter OpAmp1 output right channel.
HPL	B2	ANA OUT	Headphone amplifier output left channel
HPR	D1	ANA OUT	Headphone amplifier output right channel
VBAT	B1	SUP IN	Positive supply terminal of IC.
CPP	A1	ANA OUT	V_{NEG} charge pump flying capacitor positive terminal.
GND	A2	GND	V_{NEG} charge pump ground terminal. Has to be connected to AGND pin. For better noise performance a star shaped ground concept is the preferred option to connect these pins together.
CPN	B3	ANA OUT	V_{NEG} charge pump flying capacitor negative terminal.
VNEG	A3	SUP OUT	V_{NEG} charge pump output.
QOP1L	D2	ANA IN	Filter OpAmp1 output left channel.
IOP1L	D3	ANA OUT	Filter OpAmp1 input left channel.
QMICL	E2	SUP IN	ANC microphone preamplifier output left channel.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings of AS3412

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{GND_MAX}	Ground Terminals	-0.5	0.5	V	Applicable for pin AGND and GND
V_{SUP_MAX}	Supply Voltage to Ground	-0.5	2.1	V	Applicable for pin VBAT
V_{NEG_MAX}	Negative Terminals	-2.0	0.5	V	Applicable for pin VNEG
V_{CP_MAX}	Charge Pump Terminals	V_{NEG}-0.5	V_{NEG}+0.5	V	Applicable for pins CPN and CPP
V_{HP_MAX}	Headphone Pins	V_{NEG}-0.5	V_{NEG}+0.5	V	Applicable for pins HPR and HPL
V_{ANA_MAX}	Analog Pins	V_{NEG}-0.5	V_{NEG}+0.5	V	Applicable for pins LINL, LINR, MICL/R, HPR, HPL, QMICL/R, IOP1x, QOP1x, CPP, CPN, TRSCL/BPR, TRSDA/BPL, MICACL and MICACR
V_{CON_MAX}	Control Pins	V_{NEG}-0.5	5	V	Applicable for pins ANC/CSDA and MODE/CSCL
V_{OTHER_MAX}	Other Pins	V_{NEG}-0.5	5	V	Applicable for pins MICS
I_{SCR}	Input Current (latch-up immunity) (1) (2)	±100		mA	JEDEC 17
Continuous Power Dissipation (T_A = 70°C)					
P_T	Continuous power dissipation	-	tbd	mW	
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 2000		V	JEDEC JESD22-A114C
Temperature Ranges and Storage Conditions					
R_{THJA}	Junction to Ambient Thermal Resistance	tbd	tbd	°C/W	

Symbol	Parameter	Min	Max	Units	Comments
T_J	Operating Junction Temperature		85	°C	
T_{STRG}	Storage Temperature Range	-55	125	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices."
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	1			Unlimited floor lifetime

Note(s):

1. Latch-up test was performed with VBAT supplied and both AGND and GND grounded.
2. VNEG, CPP, CPN, MICACL and MICACR are not Latch-up stressed because these are passive pins.

Electrical Characteristics

V_{BAT} = 1.6V to 1.8V, T_A = -20°C to 85°C. Typical values are at V_{BAT} = 1.6V, T_A = 25°C, unless otherwise specified. All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics of AS3412

Symbol	Parameter	Condition	Min	Max	Unit
T_A	Ambient Temperature Range		-20	85	°C
Supply Voltages					
GND	Reference Ground		0	0	V
V_{BAT}	Battery Supply Voltage		1.6	1.8	V
V_{NEG}	Charge Pump Voltage		-1.8	-1.45	V
V_{DELTA}	Difference of Ground Supplies GND, AGND	To achieve good performance, the negative supply terminals should be connected to a low impedance ground plane.	-0.1	0.1	V
Other Pins					
V_{MICS}	Microphone Supply Voltage	MICS	0	3.7	V
V_{ANALOG}	Analog Pins	MICACL, MICACR,LINR, LINL, HPR, HPL, QMICL, QMICR, IOP1x, and QOP1x	V_{NEG}	V_{BAT}	V
$V_{CONTROL}$	Control Pins	MODE/CSCL, ANC/CSDA	0	3.7	V
V_{CP}	Charge Pump pins	CPN and CPP	V_{NEG}	V_{BAT}	V
V_{TRIM}	Application Trim Pins	TRSCL/BPR and TRSDA/BPL	V_{NEG} -0.3 or -1.8	V_{BAT} +0.5 or 1.8	V
V_{MIC}	Microphone Inputs	MICL and MICR	V_{NEG}	V_{BAT}	V

Figure 7:
Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Block Power Requirements						
I_{OFF}	Off mode current	MODE/CSCL pin low, device switched off	0.4	1	10	µA
I_{SYS}	Reference supply current	V_{BAT} = 1.8V; Bias generation, oscillator, POR; V_{NEG} disabled	0.16	0.25	0.3	mA
I_{MIC}	Mic gain stage current	V_{BAT} = 1.8V; no signal, stereo, normal mode	0.82	1.4	2	mA
		V_{BAT} = 1.8V; no signal, stereo, ECO mode	0.58	1.1	1.4	mA
I_{HP}	Headphone stage current	V_{BAT} = 1.8V; no signal, normal mode	1.5	2.4	3.1	mA
		V_{BAT} = 1.8V; no signal, ECO mode	1.18	2.0	2.9	mA
I_{MICS}	MICS charge pump current	V_{BAT} = 1.8V; no load	0.36	0.5	0.9	mA
		V_{BAT} = 1.6V; no load	0.36	0.4	0.85	mA
I_{OP1}	OP1 supply current	V_{BAT} = 1.8V; OP1L and OP1R enabled, normal mode	0.85	1.25	1.75	mA
		V_{BAT} = 1.8V; OP1L and OP1R enabled, ECO mode	0.65	0.9	1.37	mA
		V_{BAT} = 1.6V; OP1L and OP1R enabled, normal mode	0.8	1.2	1.68	mA
		V_{BAT} = 1.6V; OP1L and OP1R enabled, ECO mode	0.6	0.85	1.32	mA
Typical System Power Consumption						
P_{FF}	Typical power consumption feed forward application	OP1L, OP1R enabled, Microphone supply enabled, no load, V_{BAT}=1.6V		10		mW
P_{FF_ECO}	Typical power consumption feed forward application in ECO mode	All blocks in ECO mode OP1L, OP1R enabled Microphone supply enabled, no load, V_{BAT}=1.6V		8		mW

Electrical Characteristics: Shows the electrical characteristics like typical supply voltages as well as system current consumption.

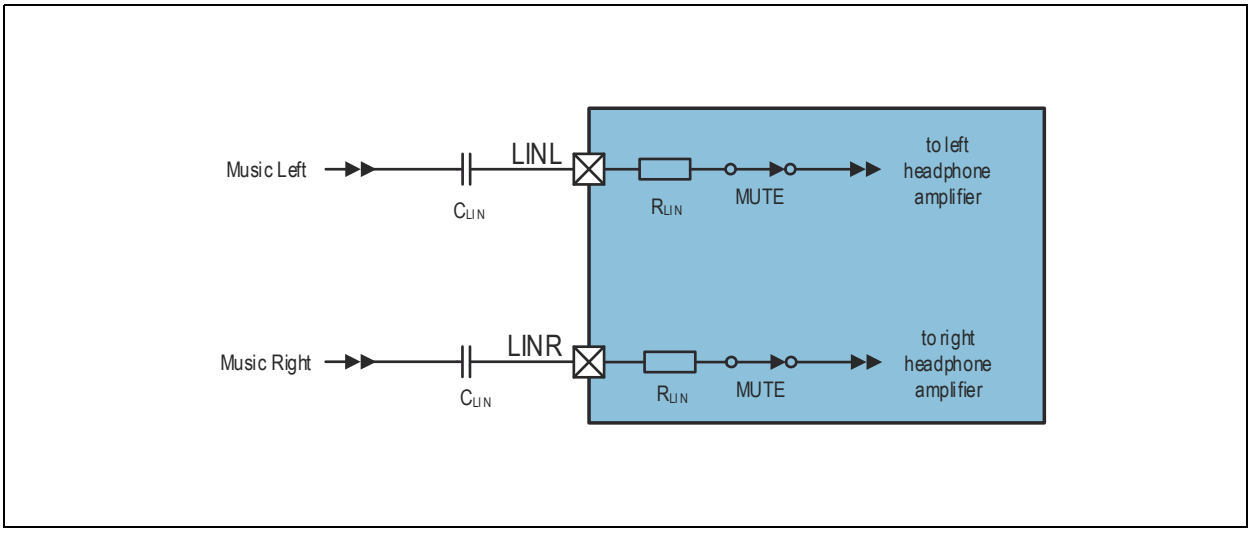
Detailed Description

This section provides a detailed description of the device related components.

Audio Line Input

The chip features one stereo line input for music playback. In monitor mode the line inputs can also be muted in order to stop music playback and increase speech intelligibility.

Figure 8:
Stereo Line Input



Stereo Line Input: This diagram shows the internal structure of the line input.

If there is a high pass function desired in an application, to block very low frequencies that could harm the speaker, or eliminate little offset voltages a simple capacitor C_{LIN} could do this function. The implementation is shown in Figure 8. The correct capacitor value for the desired cut-off frequency can be calculated with the following formula:

(EQ1)
$$C_{LIN} = \frac{1}{2 \cdot \pi \cdot R_{LIN} \cdot f_{cut\_off}}$$

A typical cut-off frequency in an audio application is 20Hz. With an input impedance R_{LIN} of typ. 2k and a desired cut off frequency of 20Hz the input capacitor should be bigger than 4µF. Therefore a typical value of 4.7µF is recommended.

Parameter

V_{BAT}=1.65V, T_A= 25°C unless otherwise specified

Figure 9:
Line Input Parameter

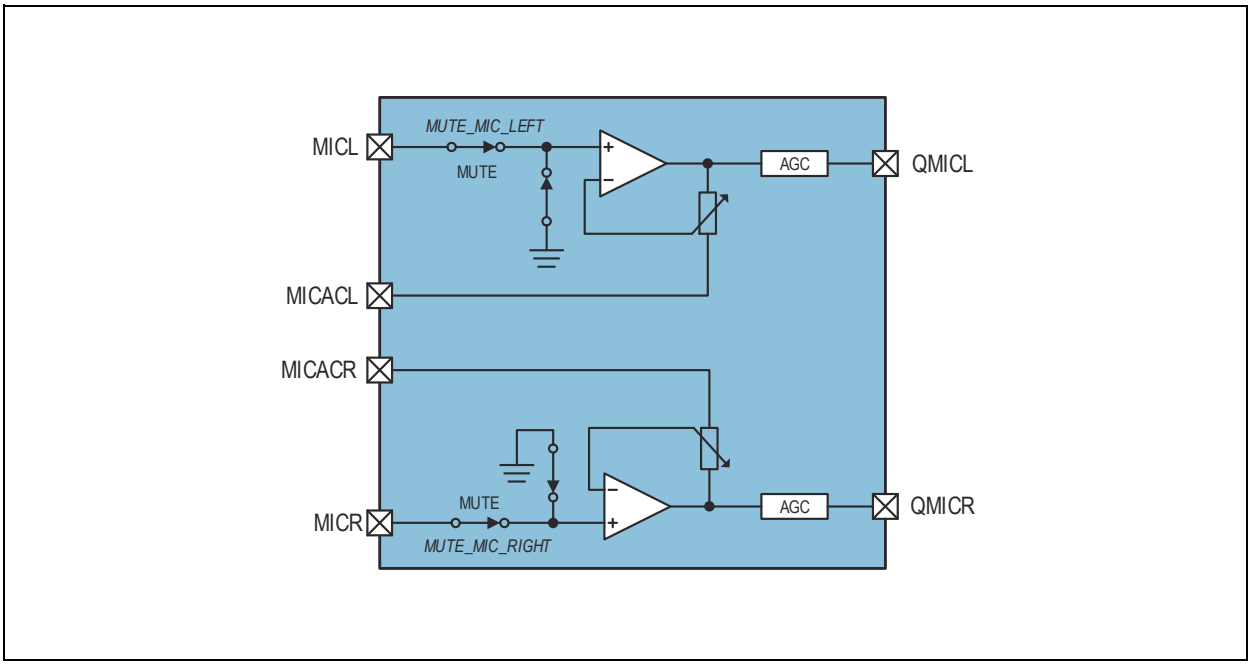
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{LIN}	Input Signal Level			0.9*V_{BAT}		V_{PEAK}
R_{LIN}	Input Impedance			2		kΩ

Line Input Parameter: This table shows the detailed electrical characteristics of the line input.

Microphone Inputs

The AS3412 offers two low noise microphone inputs with full digital control and a dedicated DC offset cancellation pin for each microphone input. In total each gain stage offers up to 63 gain steps of 0.5dB resulting in a gain range from 0dB to +31dB. The microphone gain is stored digitally during production on an OTP memory. Besides the standard microphone gain register for left and right channel, the chip features also two additional microphone gain registers for monitor mode. Thus, in monitor mode, a completely different gain setting for left and right microphone can be selected to implement voice filter functions in order to amplify the speech band for better speech intelligibility.

Figure 10:
Stereo Microphone Input



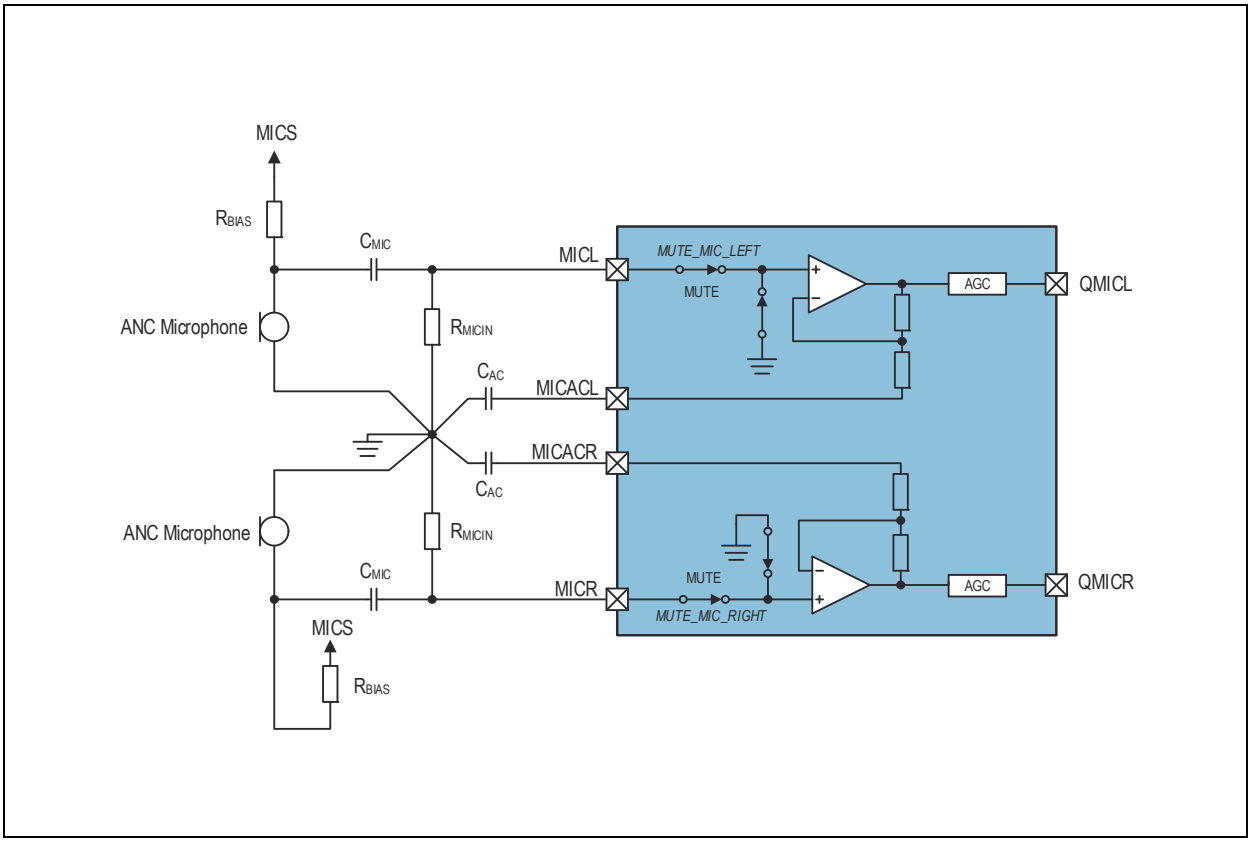
Stereo Microphone Input: This diagram shows the internal structure of the stereo microphone preamplifier including the mute switch as well as the automatic gain control (AGC).

To avoid unwanted start-up pop noise, a soft-start function is implemented for an automatic gain ramping of the device. In case of an overload condition on the microphone input (e.g. high sound pressure level), an internal state machine reduces the microphone gain automatically. For some designs it might be useful to switch off this feature. Especially in feed-back systems very often infrasound can cause an overload condition of the microphone preamplifier which results in low frequency noise. This behavior can be avoided by disabling the AGC function.

Input Capacitor Selection

The microphone preamplifier needs one bias resistor (R_{Bias}) per channel as well as DC blocking capacitors (C_{MIC}). The capacitors C_{AC} are DC blocking capacitors to avoid DC amplification of the non-inverting microphone preamplifier. This capacitor has an influence on the frequency response because the internal feedback resistors create a high pass filter together with the capacitor C_{AC}. The typical application circuit is shown in Figure 11 with all necessary components.

Figure 11:
Microphone Capacitor Selection Circuit



Microphone Capacitor Selection Circuit: This diagram shows a typical microphone application circuit with all necessary components to operate the amplifier.

The corner frequency of this high pass filter is defined with the capacitor C_{AC} and the gain of the headphone amplifier.
Figure 12 shows an overview of typical cut-off frequencies with different microphone gain settings.

Figure 12:
Microphone Cut-Off Frequency Overview

Microphone Gain	R_1	R_2	$F_{cut-off}$
0dB	22.2kΩ	0Ω	1.7Hz
3dB	15716Ω	6484Ω	1.9Hz
6dB	11126Ω	11074Ω	2.2Hz
9dB	7877Ω	14323Ω	2.7Hz
12dB	5576Ω	16623Ω	3.5Hz
15dB	3948Ω	18252Ω	4.5Hz
18dB	2795Ω	19405Ω	6.1Hz
21dB	1979Ω	20221Ω	8.4Hz
24dB	1400Ω	20800Ω	11.5Hz
27dB	992Ω	21208Ω	16.3Hz
30dB	702Ω	21498Ω	22.7Hz

Microphone Cut-Off Frequency Overview: This table shows an overview of the different cut-off frequencies with C_{AC}=10µF, C_{MIC}= 2.2µF and R_{MICIN}=22kΩ of the microphone preamplifier.

Filter Simulations: It is important when doing the ANC filter simulations to include all microphone filter components to incorporate the gain and phase influence of these components.

In the cut-off frequency overview, capacitor C_{AC} was defined as 10µF which results in a rather low cut-off frequency for best ANC filter design. If a different capacitor value is desired in the application, the following formula defines the transfer function of the high pass circuit of the microphone preamplifier:

(EQ2)
$$|A| = \frac{\sqrt{4 \cdot C_{AC}^2 \cdot f^2 \cdot (R_1 + R_2)^2 \cdot \pi^2 + 1}}{\sqrt{4 \cdot C_{AC}^2 \cdot f^2 \cdot R_1^2 \cdot \pi^2 + 1}}$$

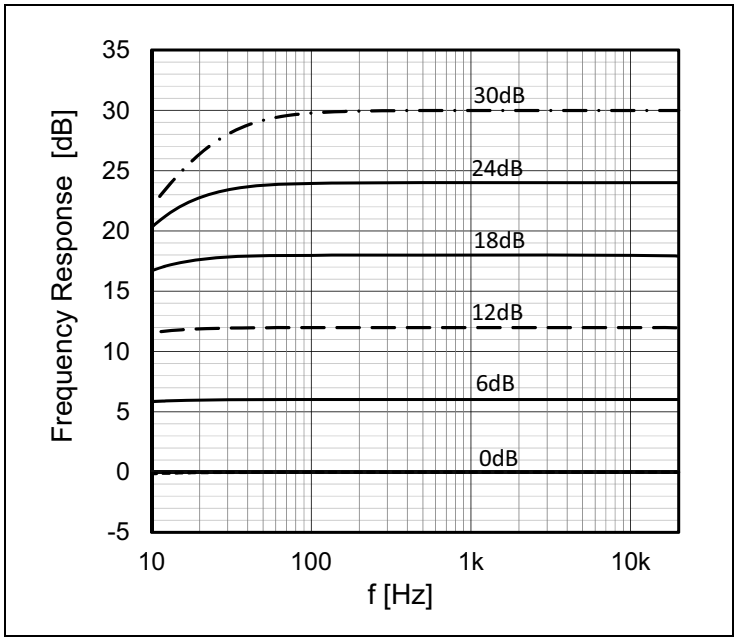
The simplified transfer function does not include the high pass filter defined by C_{MIC} and R_{MICIN}. With the recommended values of 2.2µF for C_{MIC} and 22kΩ for R_{MICIN} this filter can be neglected because of the very low cut-off frequency of 1.5Hz.

The cut-off frequency for this filter can be calculated with the following formula:

(EQ3)
$$f_{cut-off} = \frac{1}{2 \cdot \pi \cdot R_{MICIN} \cdot C_{MIC}}$$

The simulated frequency response for the microphone preamplifier with the recommended component values is shown in Figure 13.

Figure 13:
Simulated Microphone Frequency Response



Microphone Frequency Response: This graph shows the frequency response of the microphone preamplifier with different gain settings with C_{AC}=10µF, C_{MIC}=2.2µF and R_{MICIN}=22kΩ.

In application with PCB space limitations it is also possible to remove the capacitors C_{AC} and connect MICACL and MICACR pins directly to A_{GND}. In this configuration AC coupling of the QMICR and QMICL signals is recommended.

Parameter

V_{BAT}=1.8V, T_A= 25°C, C_{AC}=10µF, C_{MIC}=4.7µF and R_{MICIN}=2.2kΩ unless otherwise specified.

Figure 14:
Microphone Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{MICIN}0$	Input Signal Level	A_{MIC} = 10dB		80		mV_{RMS}
$V_{MICIN}1$		A_{MIC} = 20dB		40		mV_{RMS}
$V_{MICIN}2$		A_{MIC} = 30dB		10		mV_{RMS}
SNR	Signal to Noise Ratio	0dB gain, High quality mode, AGC off		118.5		dB
		10dB gain, High quality mode, AGC off		109		dB
		20dB gain, High quality mode, AGC off		99.5		dB
		0dB gain, ECO mode, AGC off		117		dB
		10dB gain, ECO mode, AGC off		107		dB
		20dB gain, ECO mode, AGC off		98		dB
$V_{NOISE-A}$	A-Weighted Output Noise Floor	0dB gain, 20Hz – 20kHz bandwidth, high quality		1.2		µV
		10dB gain, 20Hz – 20kHz bandwidth, High quality		4.2		µV
		20dB gain, 20Hz – 20kHz bandwidth, High quality		13.5		µV
		0dB gain, 20Hz – 20kHz bandwidth, ECO mode		1.4		µV
		10dB gain, 20Hz – 20kHz bandwidth, ECO mode		4.6		µV
		20dB gain, 20Hz – 20kHz bandwidth, ECO mode		14.8		µV
I_{MIC}	Block Current Consumption	V_{BAT} = 1.8V; no signal, stereo, normal mode	0.82	1.4	2	mA
		V_{BAT} = 1.8V; no signal, stereo, ECO mode	0.58	1.2	1.4	mA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
A_{MIC}	Programmable Gain	Discrete logarithmic gain steps	0		+31	dB
	Gain Steps Size			0.5		dB
	Gain Step Precision				0.2	dB
Δ_{AMIC}	Gain Ramp Rate	V_{PEAK} related to V_{BAT} or V_{NEG}		1		ms/step
V_{ATTACK}	Limiter Activation Level	V_{PEAK} related to V_{BAT} or V_{NEG} 64 @ 0.5dB		0.40		1
V_{DECAY}	Limiter Release Level			0.31		1
$A_{MICLIMIT}$	Limiter Minimum Gain			0		dB
t_{ATTACK}	Limiter Attack Time			5		µs/step
t_{DECAY}	Limiter Decay Time			1		ms/step

Microphone Parameter: This table shows the detailed electrical characteristics of the microphone preamplifier gain stage.

Figure 15:
Microphone Frequency Response

Microphone Frequency Response: This graph shows the frequency response of the microphone preamplifier with different gain settings without R_{MICIN} resistor, C_{AC} capacitor (MICACx pin connected to A_{GND}) and C_{MIC}=10uF.

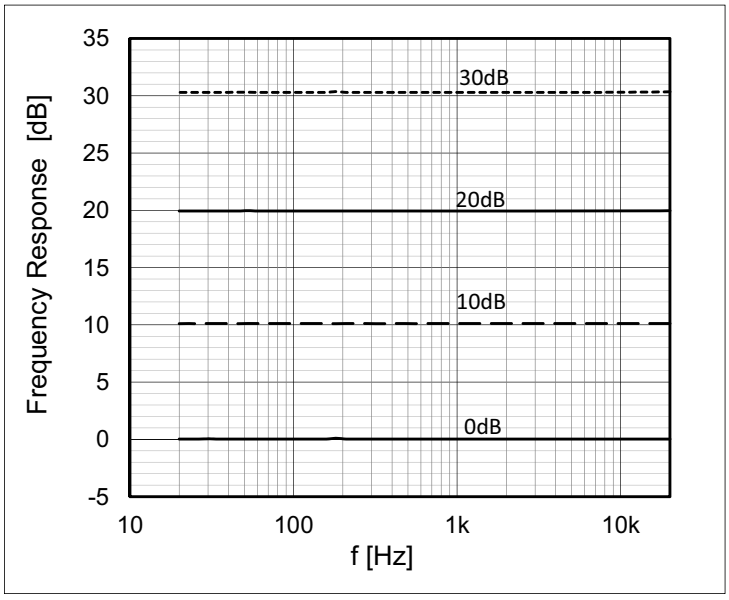


Figure 16:
Microphone THD+N vs. V_{input}

Microphone THD+N vs. Vinput: This graph shows the A-weighted THD+N versus input voltage of the microphone preamplifier with 0dB gain and V_{BAT}=1.8V.

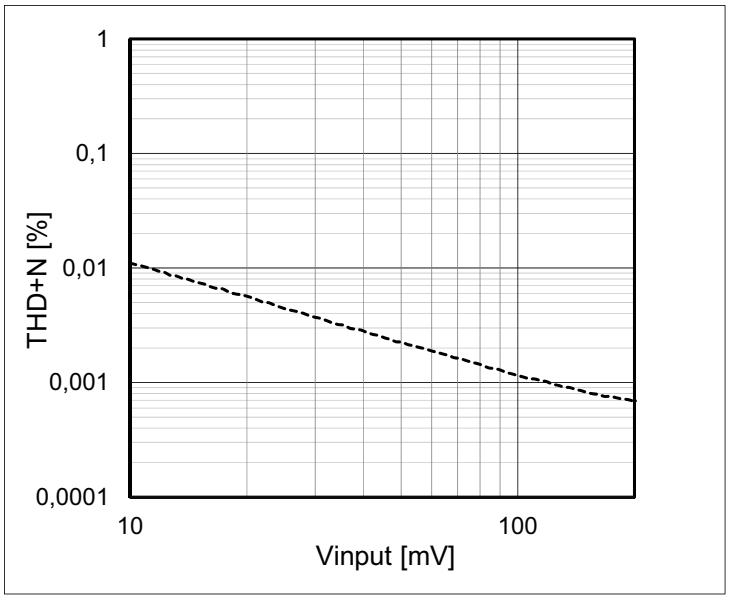
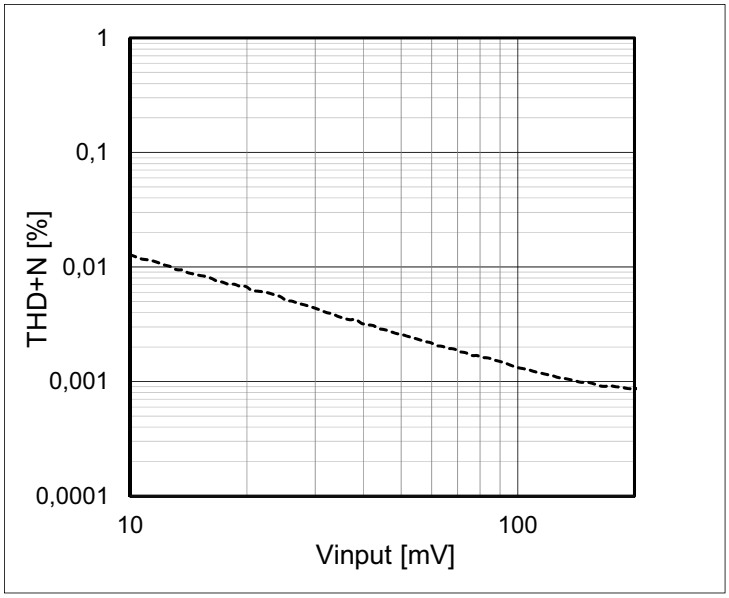


Figure 17:
Microphone THD+N vs. V_{input} ECO Mode

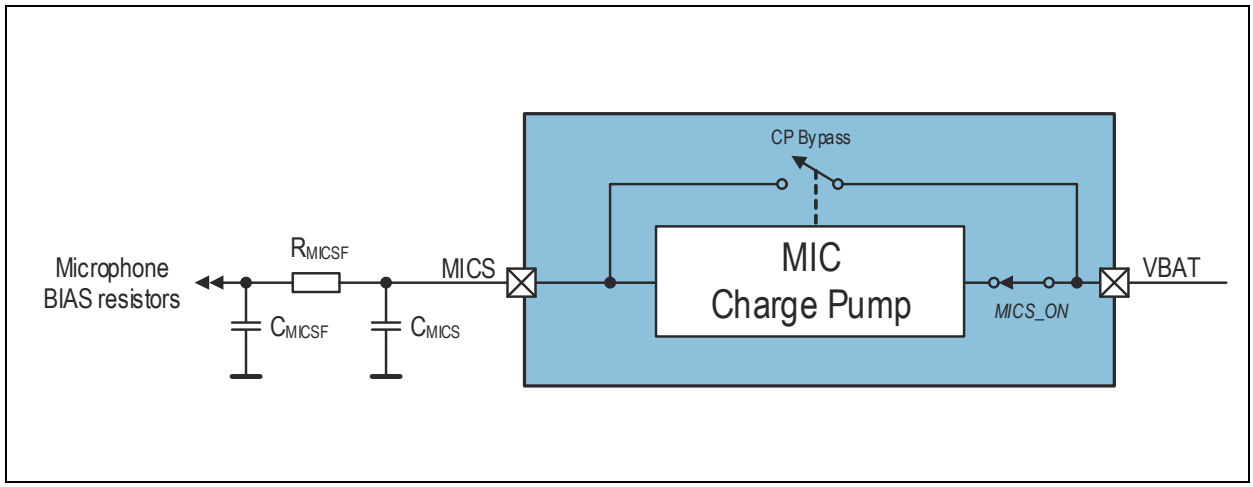
Microphone THD+N vs. Vinput: This graph shows the A-weighted THD+N versus input voltage of the microphone preamplifier with 0dB gain and V_{BAT}=1.8V. The amplifier runs in ECO mode.



Microphone Supply

The AS3412 features an integrated microphone supply charge pump. This charge pump provides the proper microphone supply voltage even with a 1.8V chip supply voltage in order to increase the sensitivity of the microphone.

Figure 18:
Microphone Supply



Therefore the integrated charge pump generates a microphone supply voltage which is typically 2.7V. The microphone supply voltage is also used to switch off the integrated music bypass switch of the AS3412 is in active mode. Therefore, during normal operation the microphone supply must not be switched off if the TRSDA/BPL and TRSCL/BPR pins are in use.

Bypass Switch Operation: When using the TRSDA/BPL and TRSCL/BPR pins you must not switch off the microphone supply!

Parameter

V_{BAT}=1.8V, T_A= 25°C, C_{MICS} = 22µF, C_{MICSF} = 47µF and R_{MICSF} = 220Ω unless otherwise specified.

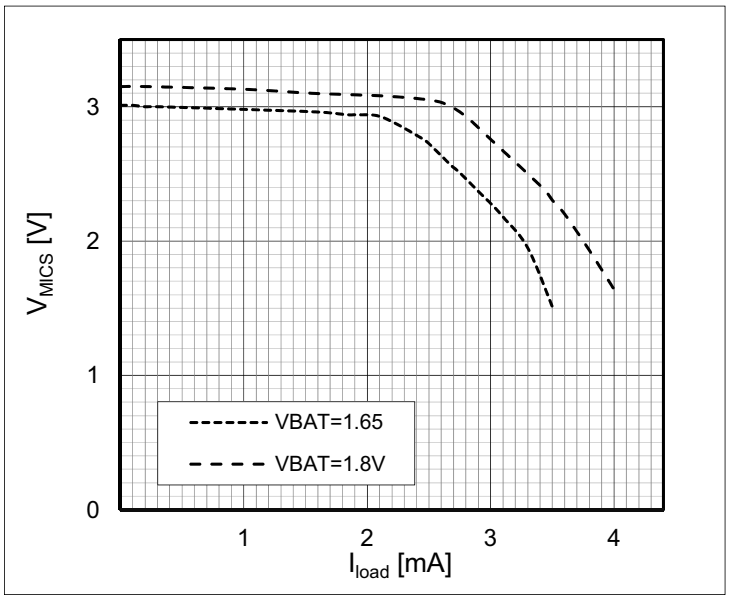
Figure 19:
Microphone Supply Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{MICS}	Microphone Supply Voltage	V_{BAT} = 1.8V, no load		3.4		V
		V_{BAT} = 1.65V, no load		3.2		V
I_{MICS}	Block Current Consumption	V_{BAT} = 1.8V; no load	0.36	0.5	0.9	mA
		V_{BAT} = 1.65V; no load	0.36	0.4	0.85	mA
$V_{Noise-A}$	Microphone Supply Noise	A-Weighted, 500µA load		1.4		µV
		A-Weighted, 550µA load, only C_{MICS} = 22uF assembled		11		µV
		A-Weighted, 500µA load, only C_{MICS} = 10uF assembled		15		µV

Microphone Supply Parameter: This table shows the detailed electrical characteristics of the microphone supply.

Figure 20:
Microphone Supply Load Characteristic

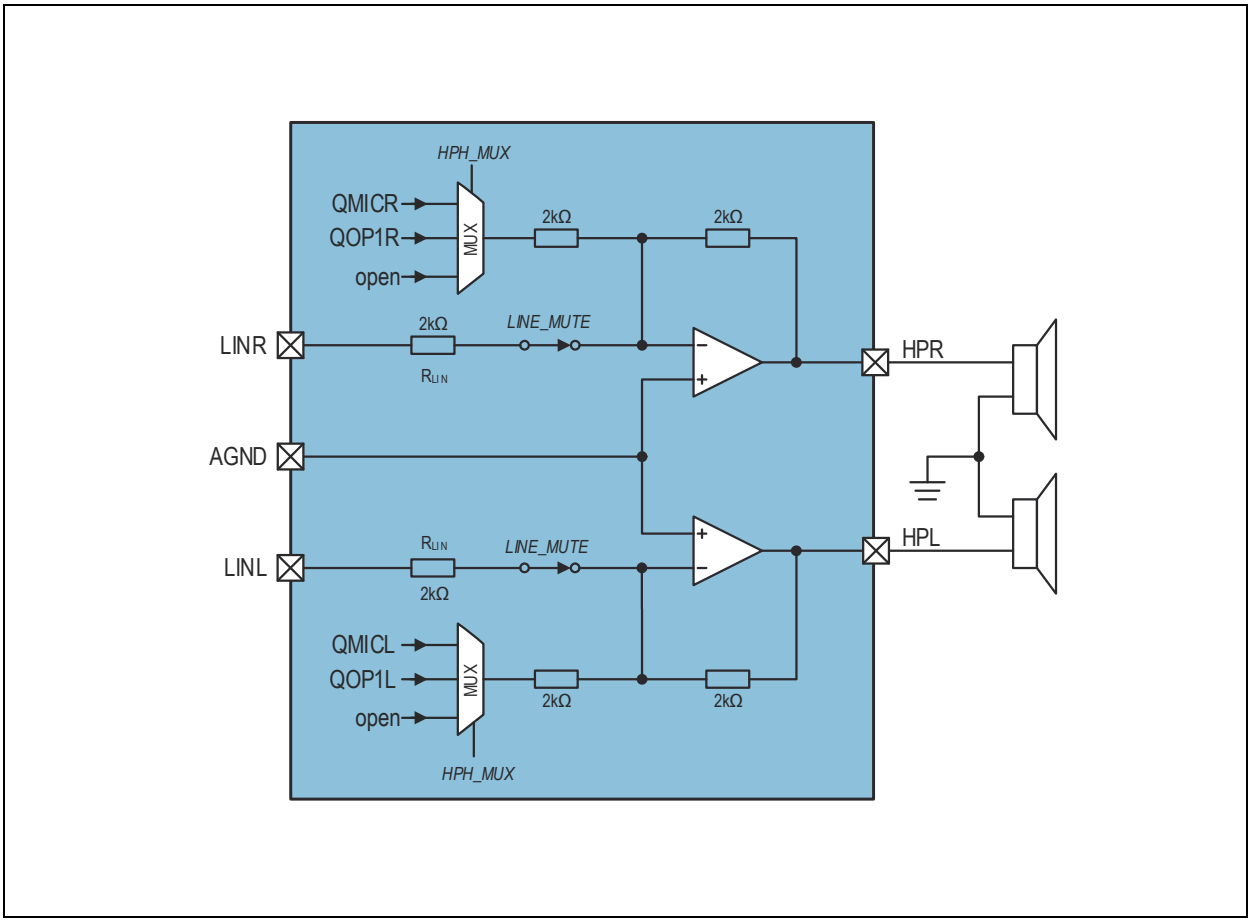
Microphone Supply Load Characteristic: This diagram shows output voltage of the microphone supply vs. output load on the microphone supply.



Headphone Amplifier

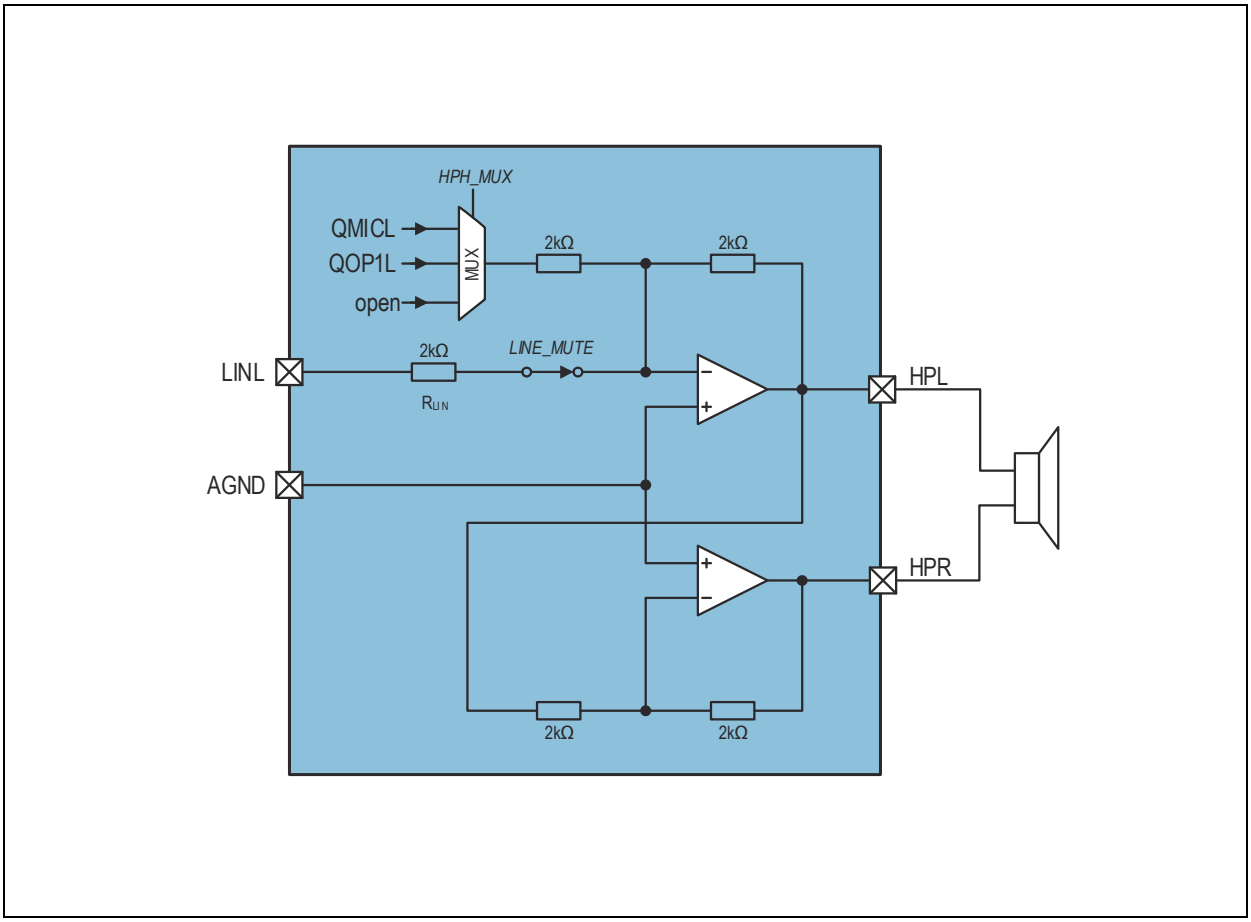
The headphone amplifier is a true ground output using V_{NEG} as negative supply. It is designed to feature an output power of 2x34mW @ 32Ω load. For higher output requirements, the headphone amplifier is also capable of operating in bridged mode. In this mode the left output is carrying the inverted signal of the right output shown in Figure 22. With a V_{BAT} voltage of 1.8V, a maximum output power of 90mW can be achieved. This is required for over- and on ear headsets with higher output power requirements. The amplifier itself features various input sources. The line input signal is directly connected to the headphone amplifier. The input multiplexer supports three different input signals which can be configured according to the *HPH_MUX* register. The "Open" setting is being used to disable the active noise cancelling function.

Figure 21:
Headphone Amplifier Single Ended



Headphone Amplifier Single Ended: This figure shows the block diagram of the headphone amplifier including the integrated music bypass switches as well as the summation input of the amplifier in single ended configuration.

Figure 22:
Headphone Amplifier Differential



Headphone Amplifier Differential: This figure shows the block diagram of the headphone amplifier including the integrated music bypass switches as well as the summation input of the amplifier in differential output mode.

Parameter

V_{BAT} =1.8V, T_A= 25°C, unless otherwise specified.

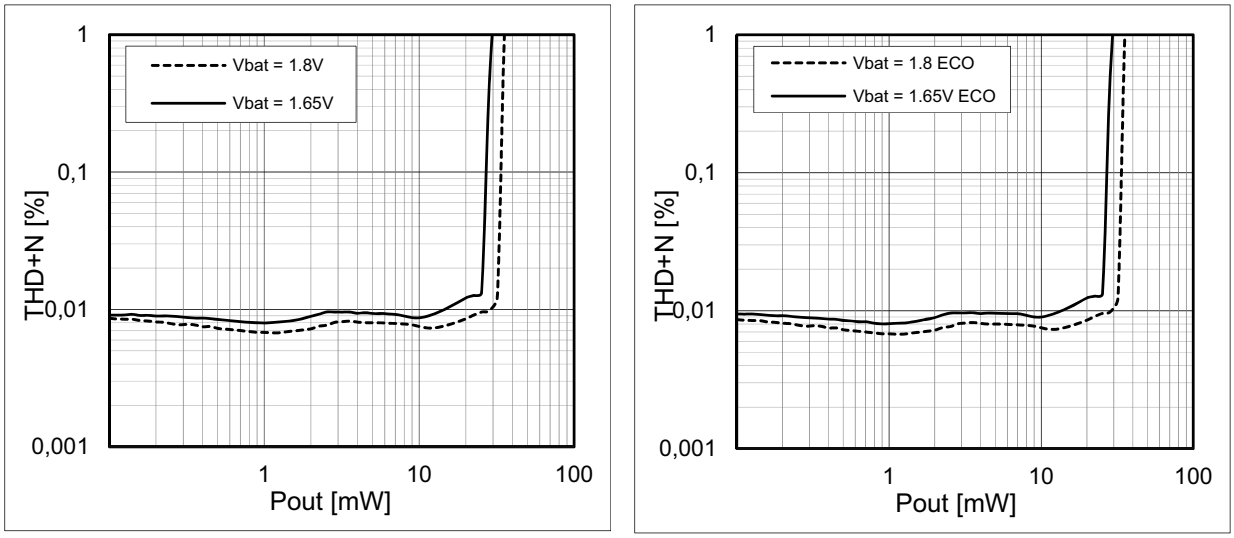
Figure 23:
Headphone Amplifier Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{L_HP}	Load Impedance	Stereo mode	16	32		Ω
		Mono	32			Ω
C_{L_HP}	Load Capacitance	Stereo mode			100	pF
P_{HP}	Nominal Output Power Stereo Mode	V_{bat} = 1.8V; 32Ω load; THD<0.1%		34		mW
		V_{bat} = 1.65V; 32Ω load; THD<0.1%		29		mW
		V_{bat} = 1.8V; 16Ω load; THD<0.1%		50		mW
		V_{bat} = 1.65V; 16Ω load; THD<0.1%		41		mW
P_{HP_BRIDGE}	Nominal Output Power Differential Mode	V_{bat} = 1.8V; 32Ω load		90		mW
		V_{bat} = 1.65V; 32Ω load		75		mW
I_{HPH}	Supply current	V_{BAT} = 1.8V; no signal, normal mode	1.5	2.4	3.1	mA
		V_{BAT} = 1.8V; no signal, ECO mode	1.18	2	2.9	mA
P_{SRRHP}	Power Supply Rejection Ratio	1kHz		100		dB
SNR	Signal to Noise Ration	High Quality Mode, Line Input -> HPH stereo in phase test signal; 32Ω load; V_{BAT} = 1.8V;		111.5		dB
		High Quality Mode, Line Input -> HPH stereo out of phase test signal; 32Ω load; V_{BAT} = 1.8V;		112.5		dB
		ECO Mode, Line Input -> HPH stereo in phase test signal; 32Ω load; V_{BAT} = 1.8V;		109.5		dB
		ECO Mode, Line Input -> HPH stereo out of phase test signal; 32Ω load; V_{BAT} = 1.8V;		110.5		dB
Channel Separation		32Ω load		93		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{Noise-A}$	Output Noise Floor A-Weighted	High Quality Mode; 32Ω load; *HP_MUX* = nc; LINx connected to ground		2.5		µV
		ECO Mode; 32Ω load; *HP_MUX* = nc; LINx connected to ground		3.1		µV

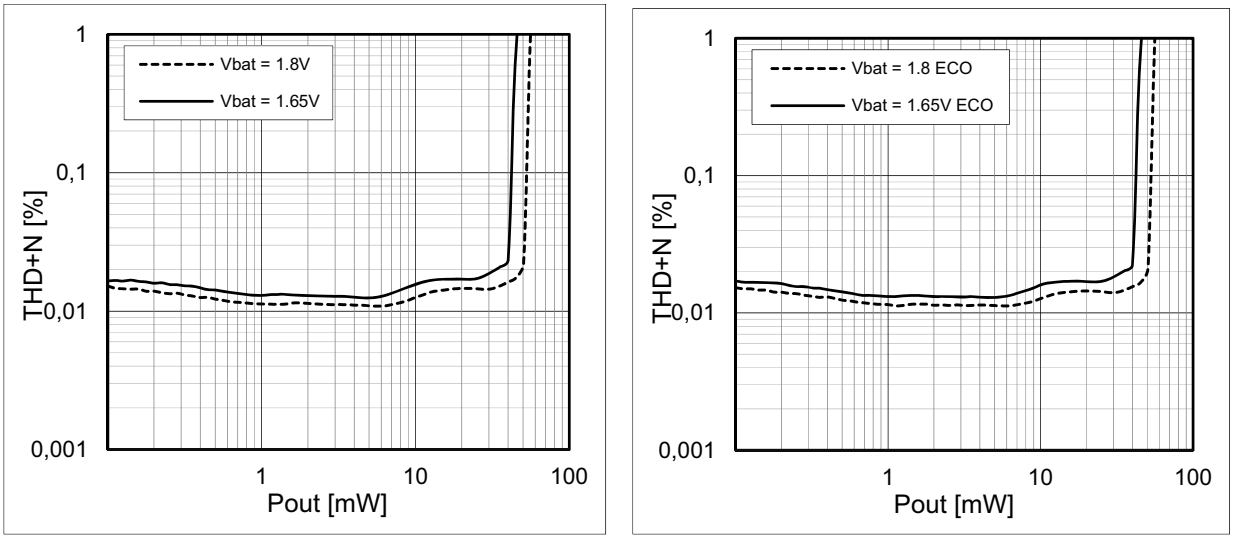
Headphone Amplifier Parameter: This table shows the detailed electrical characteristics of the headphone amplifier like output power, SNR and channel separation.

Figure 24:
Headphone THD+N vs. Output Power 32Ω Stereo



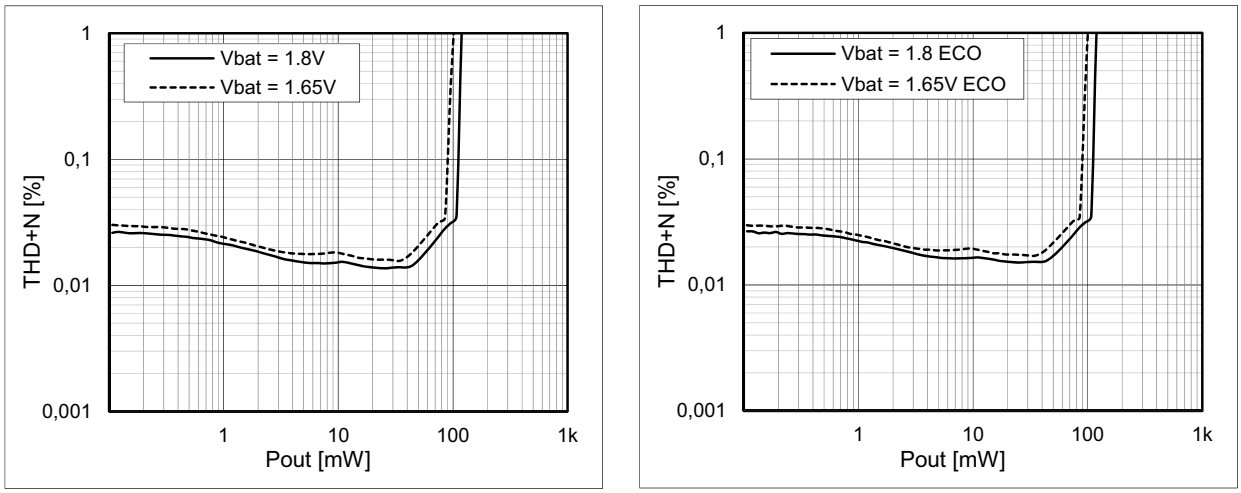
Headphone THD+N vs. Output Power: These figures shows the THD+N measurements of the headphone amplifier with different supply voltages in normal mode and ECO mode. The amplifier gain is 0dB with 32Ω load.

Figure 25:
Headphone THD+N vs. Output Power 16Ω Stereo



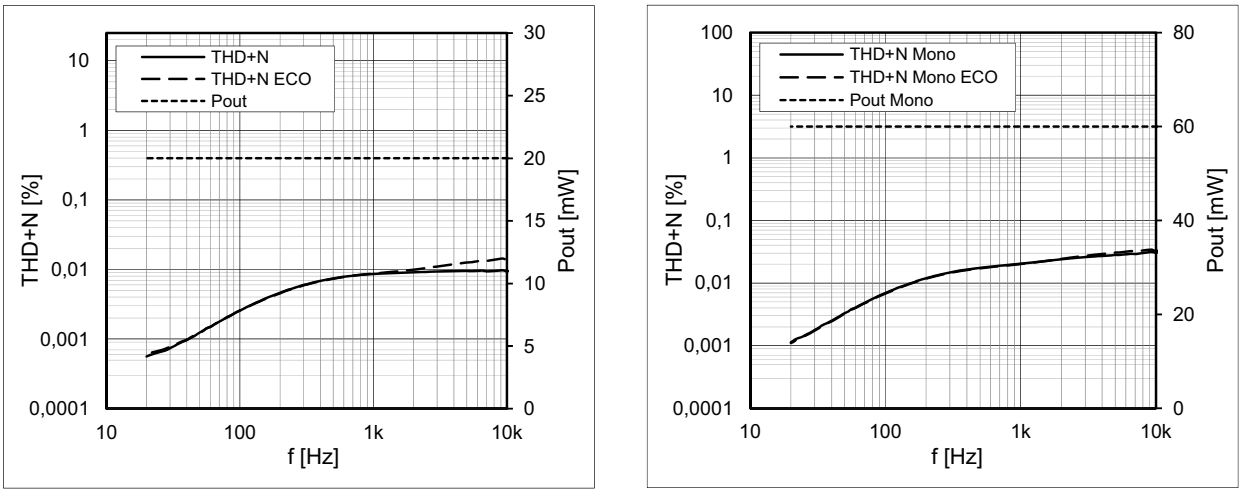
Headphone THD+N vs. Output Power: These figures shows the THD+N measurements of the headphone amplifier with different supply voltages in normal mode and ECO mode. The amplifier gain is 0dB with 16Ω load.

Figure 26:
Headphone THD+N vs. Output Power 32Ω Mono



Headphone THD+N vs. Output Power: These figures shows the A-weighted THD+N measurements of the headphone amplifier with different supply voltages in normal mode and ECO mode. The amplifier gain is 6dB with 32Ω load in mono configuration.

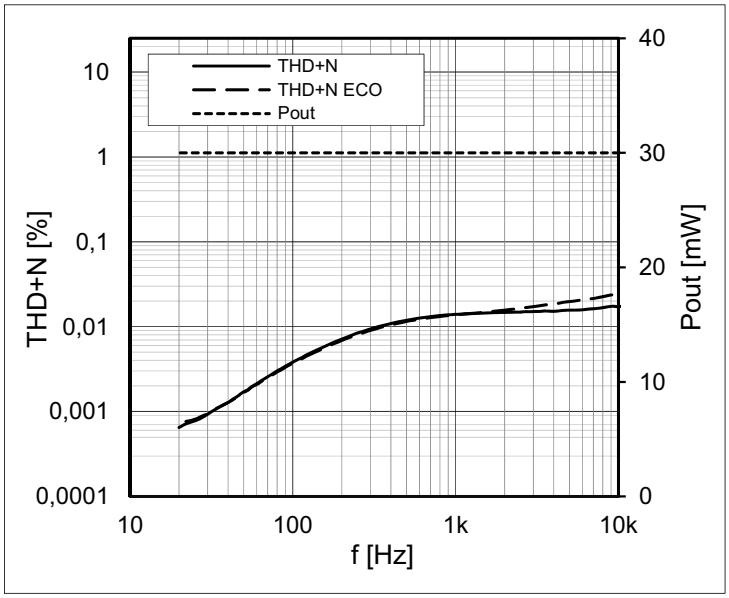
Figure 27:
Headphone THD+N vs. Frequency 32Ω Stereo/Mono



Headphone THD+N vs. Frequency: These figures shows the A-weighted THD+N measurements over frequency in stereo and mono differential mode with V_{BAT}=1.8V. The amplifier gain is 0dB and the load in both modes is 32Ω with 1mW and 5mW output power.

Figure 28:
Headphone THD+N vs. Frequency 16Ω Stereo

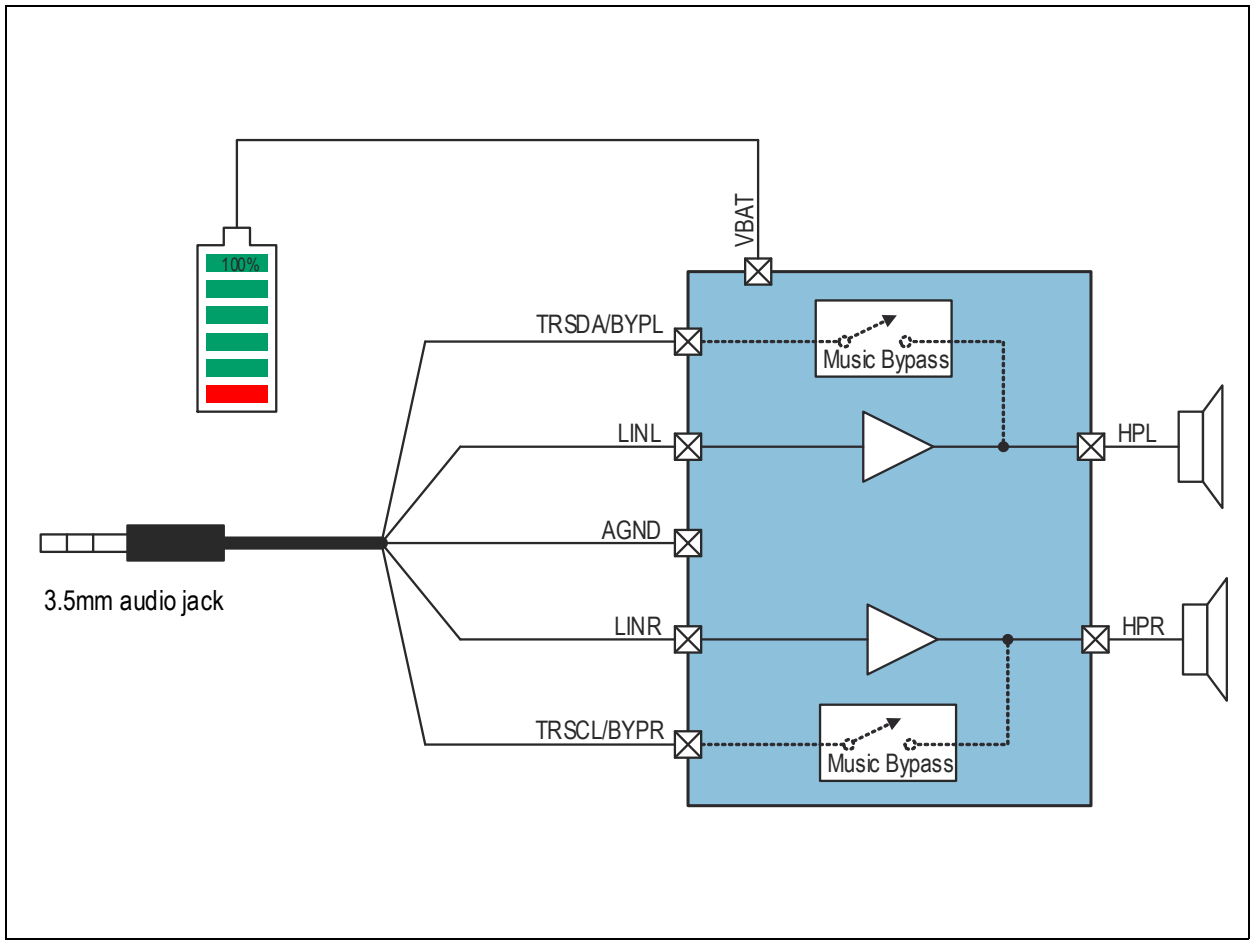
Headphone THD+N vs. Frequency:
These figures shows the A-weighted THD+N measurements over frequency in stereo mode with V_{BAT}=1.8V. The amplifier gain is 0dB and the load is 16Ω.



Integrated Music Bypass Switch

If the AS3412 is switched off, the device features a unique integrated music bypass function. The bypass switches can be used to replace a mechanical switch to bypass the music signal in off mode or if the headset runs out of battery. Figure 29 shows the basic music playback path of the AS3412 with a full battery. In this mode the line input signal is feed to the headphone amplifier. The integrated bypass switches are automatically disabled in this operation mode.

Figure 29:
Bypass Mode Inactive

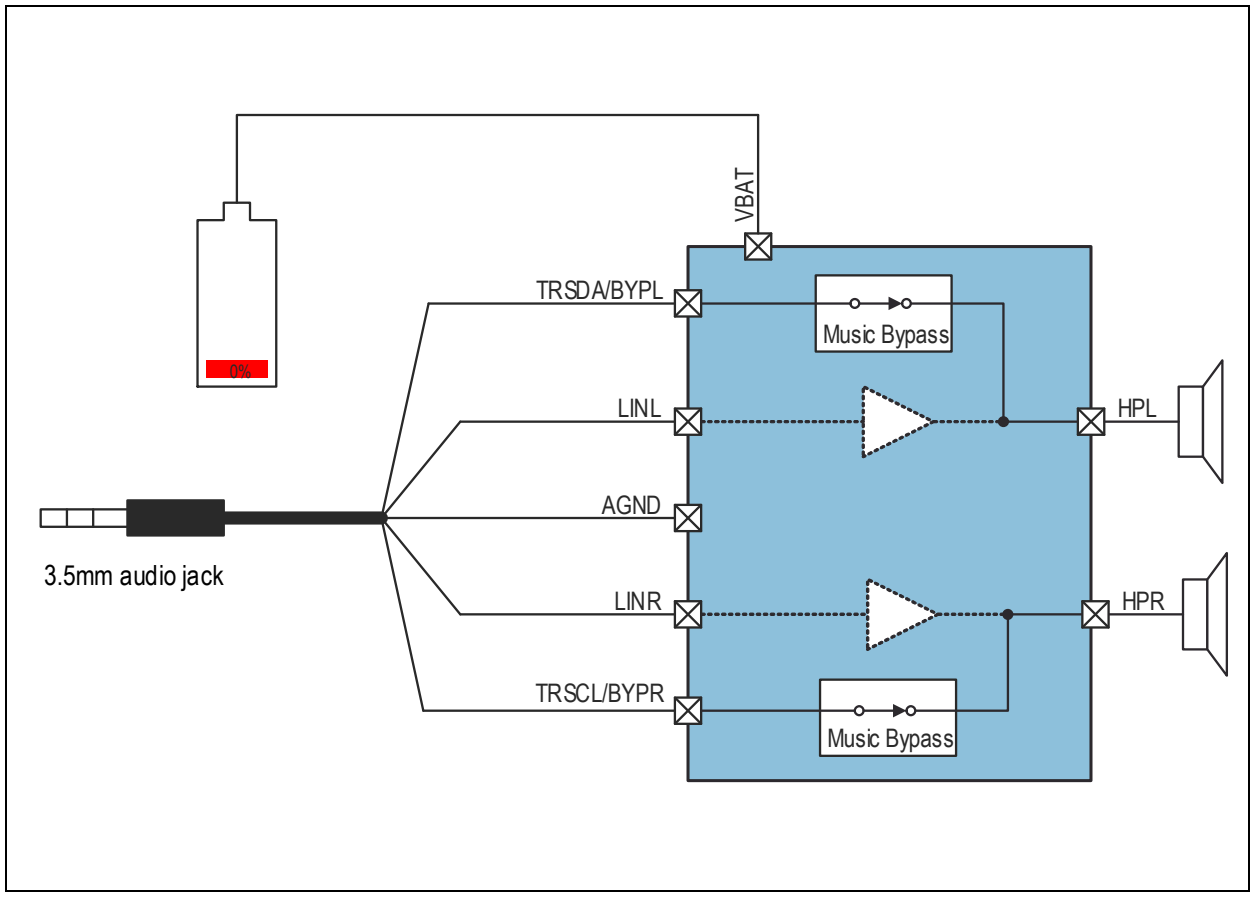


Bypass Mode Active: This block diagram shows the general music playback path of AS3412 with the integrated music bypass switches disabled.

Figure 30 shows the AS3412 in off mode with an empty battery. This is basically the same use case as no battery at all. In this mode the internal bypass switch becomes active. The headphone amplifier is not powered because the headset has run out of battery and the bypass switch becomes active. Thus the music signal coming from the 3.5mm audio jack is routed through the ANC chip, without any power source connected to the device, to the speakers.

Integrated Bypass Switch: The integrated bypass switch works even without any battery connected to the device. It helps to reduce BOM costs and PCB area. Furthermore it facilitates new industrial designs to ANC solutions.

Figure 30:
Bypass Mode Active



Bypass Mode Inactive: This block diagram shows the general music playback path of AS3412 with the integrated music bypass switches enabled. The device has no supply any more but music playback is still possible via the internal bypass switches.

Parameter

V_{BAT} =0V, T_A= 25°C, unless otherwise specified.

Figure 31:
Bypass Switch Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{Switch}	Impedance	Power down		1.5		Ω
THD	Total Harmonic Distortion	0dBV input signal, 32Ω load		-90		dB
		0dBV input signal, 16Ω load		-80		dB

Bypass Switch Parameter: This table shows the detailed electrical characteristics of the integrated bypass switch.

Figure 32:
Bypass THD+N vs. Output Power 16Ω Load

Bypass THD+N vs. Output Power: This graph shows A-weighted THD+N characteristics of the integrated bypass switch for 16Ω load.

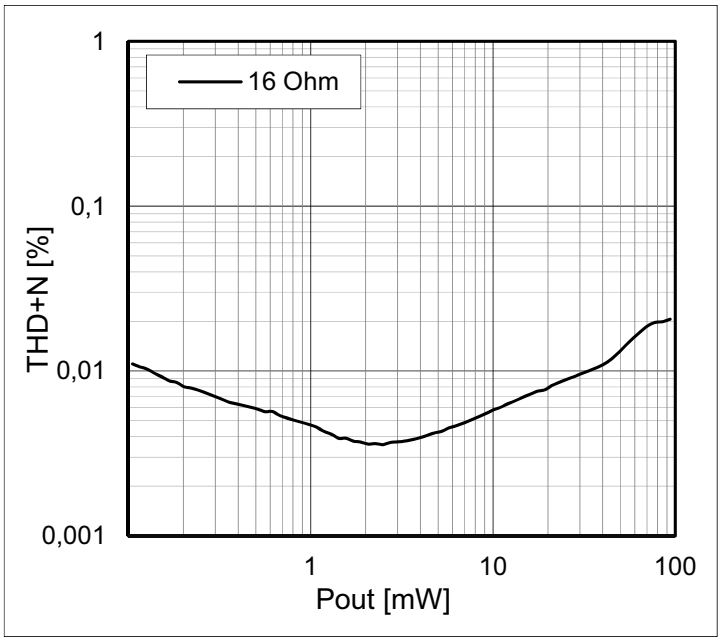
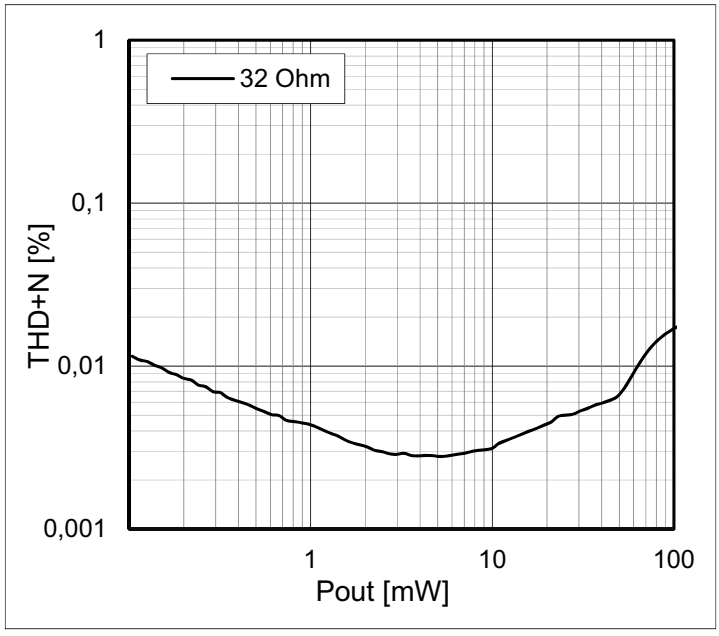


Figure 33:
Bypass THD+N vs. Output Power 32Ω Load

Bypass THD+N vs. Output Power: This graph shows A-weighted THD+N characteristics of the integrated bypass switch for 32Ω load.

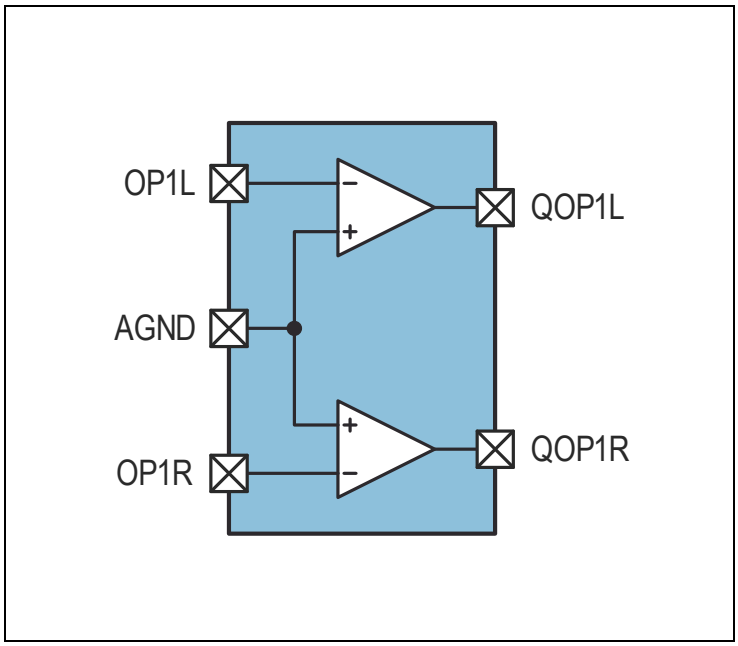


Operational Amplifier

The AS3412 offers one general purpose operational amplifier for feed-forward ANC applications. The amplifier is used to develop the gain- and phase compensation filter for the ANC signal path.

Figure 34:
Operational Amplifiers

Operational Amplifier: This figure shows the block diagram of the operational amplifiers to be used for ANC filter design.



Parameter

V_{BAT} =1.8V, T_A= 25°C, R_{input} = R_{FB} = 1kΩ unless otherwise specified.

Figure 35:
Operational Amplifier Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{LIN}	Input Signal Level	Gain=0dB		0.9*V_{BAT}	V_{BAT}	V_{PEAK}
SNR	Signal to Noise Ratio	10kΩ load, Gain = 0dB(1), V_{BAT}=1.8V, High Quality Mode		122.5		dB
		10kΩ load, Gain = 0dB, V_{BAT}=1.65V High Quality Mode		121.5		dB
		10kΩ load, Gain = 0dB, V_{BAT}=1.8V, ECO Mode		121		dB
		10kΩ load, Gain = 0dB, V_{BAT}=1.65V, ECO Mode		119.5		dB
I_{OP1}	Block Current Consumption	V_{BAT} = 1.8V; OP1L and OP1R enabled, normal mode	0.85	1.25	1.75	mA
		V_{BAT} = 1.8V; OP1L and OP1R enabled, ECO mode	0.65	0.9	1.37	mA
		V_{BAT} = 1.65V; OP1L and OP1R enabled, normal mode	0.8	1.2	1.68	mA
		V_{BAT} = 1.65V; OP1L and OP1R enabled, ECO mode	0.6	0.85	1.32	mA
$V_{NOISE-A}$	Input Referred Noise Floor A-Weighted	High Quality Mode		900		nV
		ECO Mode		1.1		µV
V_{offset}	DC offset voltage	Gain = 0dB			2	mV
C_L	Load Capacitance				100	pF
A_{Loop}	Open Loop Gain	100Hz		120		dB
R_L	Load Impedance		1			kΩ

Operational Amplifier: This table shows the detailed electrical characteristics of the operational amplifiers to be used for ANC signal processing.

Note(s):

1. SNR figure measured with 20dB gain to minimize audio analyzer noise floor

Figure 36:
Operational Amplifier Frequency Response

Operational Amplifier Frequency Response: This graph shows the frequency response of the operational amplifiers with 0dB gain in normal and ECO mode.

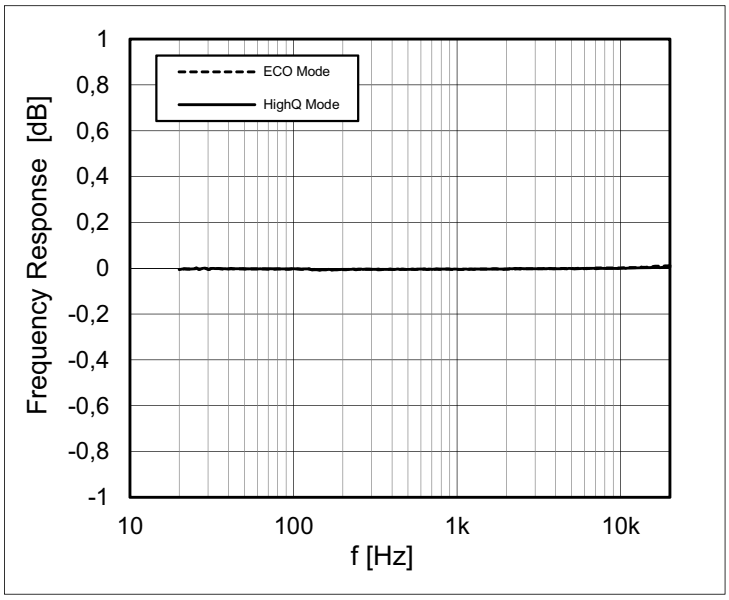
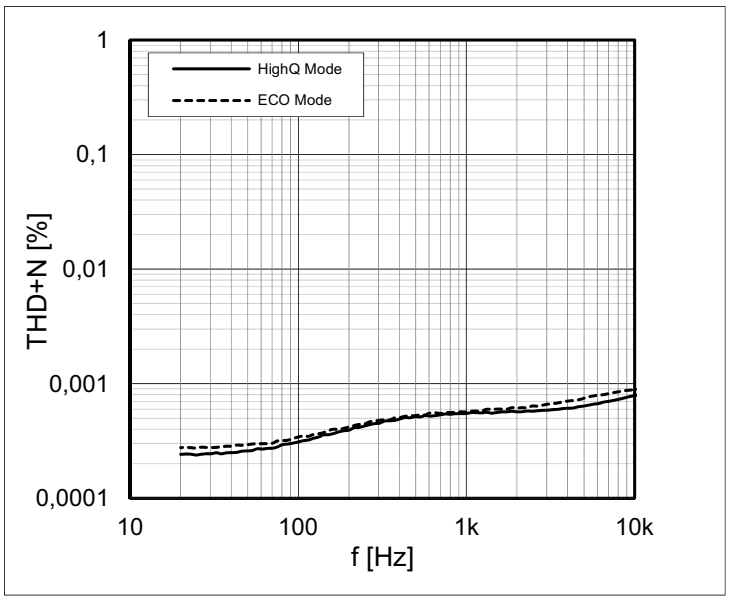


Figure 37:
Operation Amplifier THD+N vs. Frequency V_{BAT} = 1.8V

Operation Amplifier THD+N vs. Frequency: The diagram shows the A-weighted THD+N measurement of the line input amplifier with 0dB gain and V_{BAT}=1.8V.



System

The system block handles the power up and power down sequencing as well as the mode switching.

Power Up/Down Conditions

The chip powers up when one of the following conditions is true:

Figure 38:
Power Up Conditions

#	Source	Description
1	MODE pin	In stand-alone mode, MODE pin has to be driven high for >2ms to turn on the device
2	I^2C start	In I^2C mode, an I^2C start condition turns on the device

Power Up Conditions: This table shows the available power up conditions of the AS3412.

The chip automatically shuts off if one of the following conditions arises:

Figure 39:
Power Down Conditions

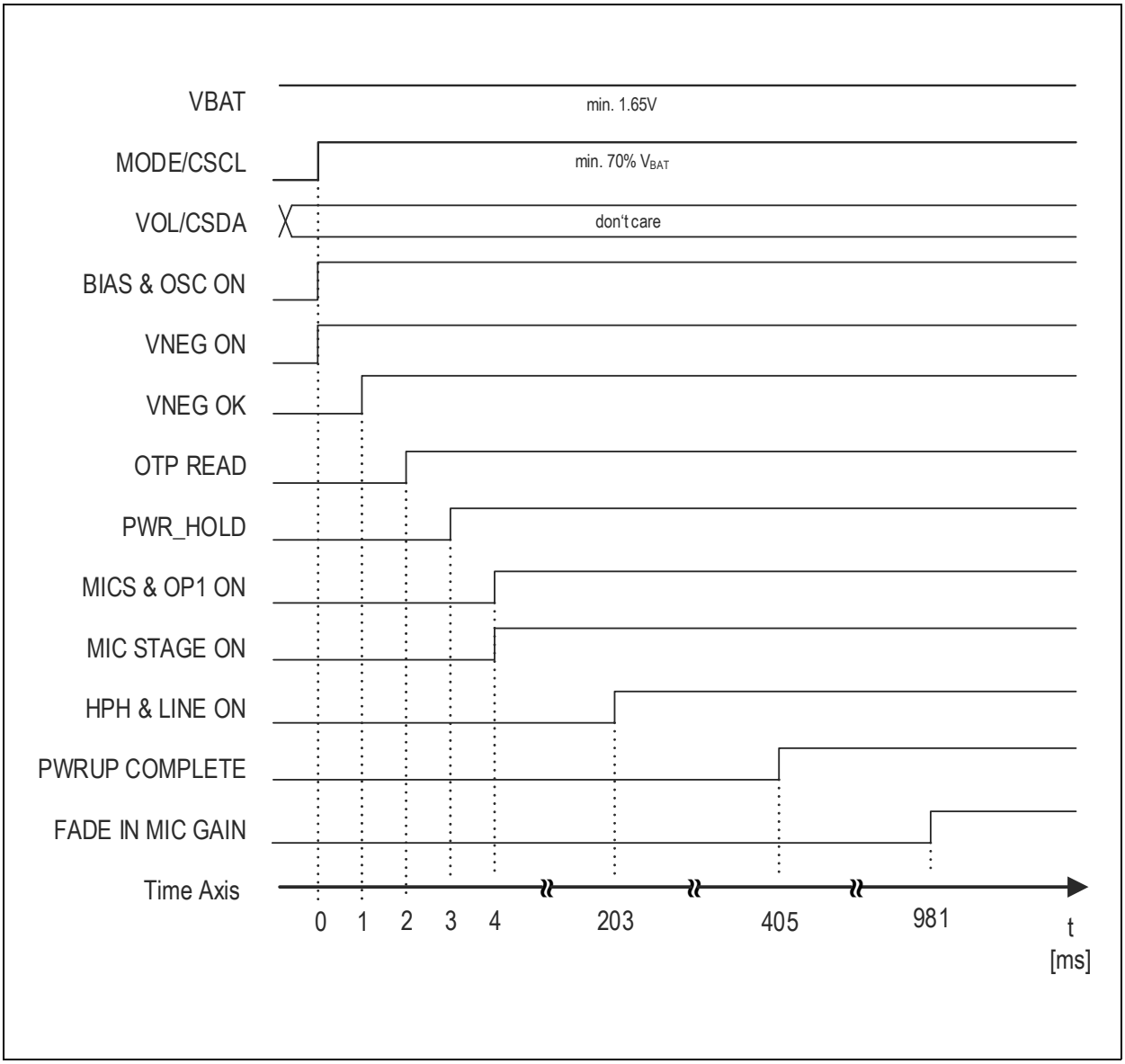
#	Source	Description
1	MODE pin	Slider Mode: Mode pin has to be driven low for 10ms to turn off Push Button Mode: Mode pin has to be driven high for >2.4sec to turn off
2	Serial Interface	Power down by serial interface by clearing the PWR_HOLD bit. (Please mind that the I^2C_MODE bit has to be set before clearing the PWR_HOLD bit for security reasons)
3	V_{NEG} CP OVC	Power down if V_{NEG} is higher than the V_{NEG} off-threshold

Power Down Conditions: This table shows the available power down conditions of the AS3412.

Start-Up Sequence

The AS3412 has a defined startup sequence. Once the AS3412 MODE pin is pulled high, the device initiates the automatic startup sequence shown in Figure 40.

Figure 40:
Start-Up Sequence



Start-Up Sequence: This timing diagram shows the startup sequence of the AS3412 in detail.

Operation Modes

If the AS3412 is in stand-alone mode (no I²C control), the device can work in different operation modes. An overview of the different operation modes is shown in Figure 41.

Figure 41:
Operation Modes

MODE	Description
OFF	Chip is turned off.
ANC	Chip is turned on and active noise cancellation is active
MONITOR	In monitor mode, a different (normally higher) microphone preamplifier gain can be configured to get an amplification of the ambient noise. To get rid of the low pass filtering needed for the noise cancellation, the headphone input multiplexer can be set to a different (typically MIC) source to increase speech intelligibility. In addition, the Line Input can be muted to further enhance speech intelligibility. If the device is operated in I²C mode, it is also possible to enter the monitor mode by setting the MON_MODE bit in register 0x3D.
PBO	The Playback Only Mode is a special mode that disables the noise cancelling function and just keeps the line input amplifier as well as the headphone amplifier active.

Operation Modes: This table gives an overview of the different operation modes of the AS3412.

With the AS3412 the design engineer has different options to enter the described operation modes shown in Figure 41. In addition to the different switch and push button connections described in the following three chapters, it is also important to configure the chipset accordingly. Figure 42 shows the required register configuration settings to enable the different AS3412 control modes.

Figure 42:
User Interface Control Modes

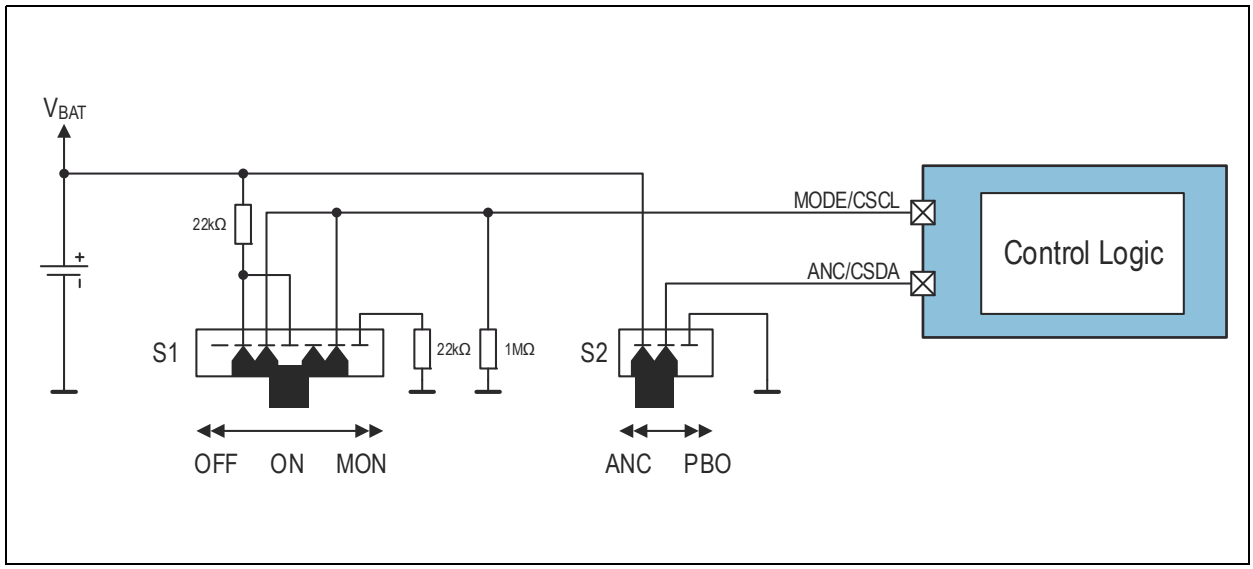
MODE	Register Name	
	SLIDE_PWR_UP	SLIDER_MON
Button Mode	0	0
Do not use	0	1
Slider Mode	1	0
Full Slider Mode	1	1

Stand Alone Operation Mode: Shows the different operation modes that can be selected with push button control or slide switch control.

Full Slider Mode

Full Slider Mode enables the AS3412 to be connected to two slide switches for Power, ANC and Monitor Mode control. To enable this operation mode both bits, SLIDE_PWR_UP and SLIDER_MON, have to be set to '1'. The typical connection of the slide switches is shown in Figure 43.

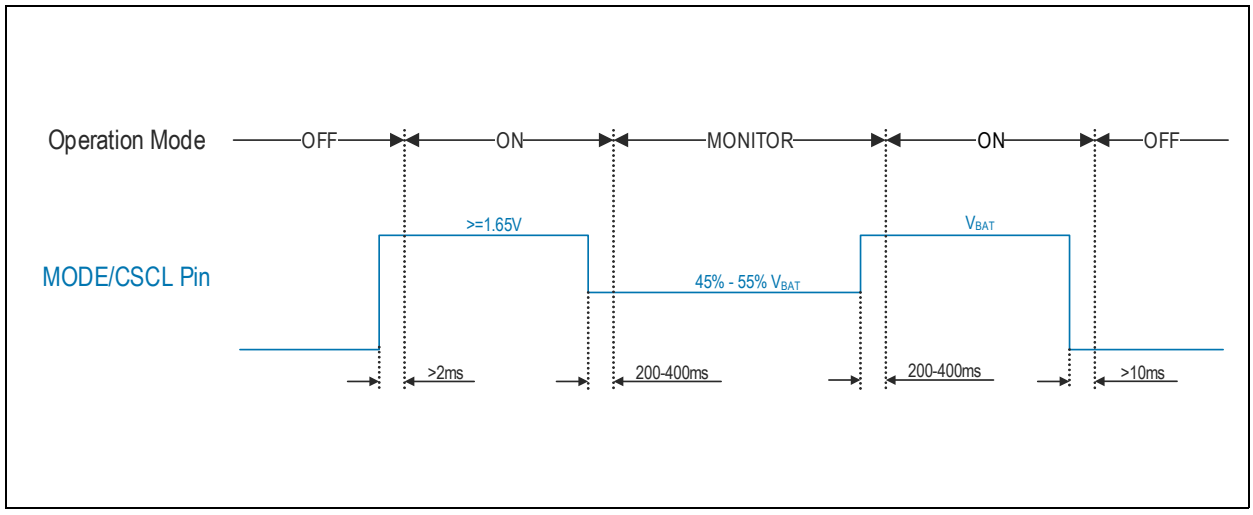
Figure 43:
Full Slider Mode



Full Slider Mode: The diagram shows the external connection of the switches in full slider mode.

In Full Slider Mode the MODE/CSCL pin can detect three different input levels to distinguish between different operating modes: On, Off and Monitor mode. The timing diagram with all relevant information is shown in Figure 44.

Figure 44:
Full Slider Mode Timing Diagram

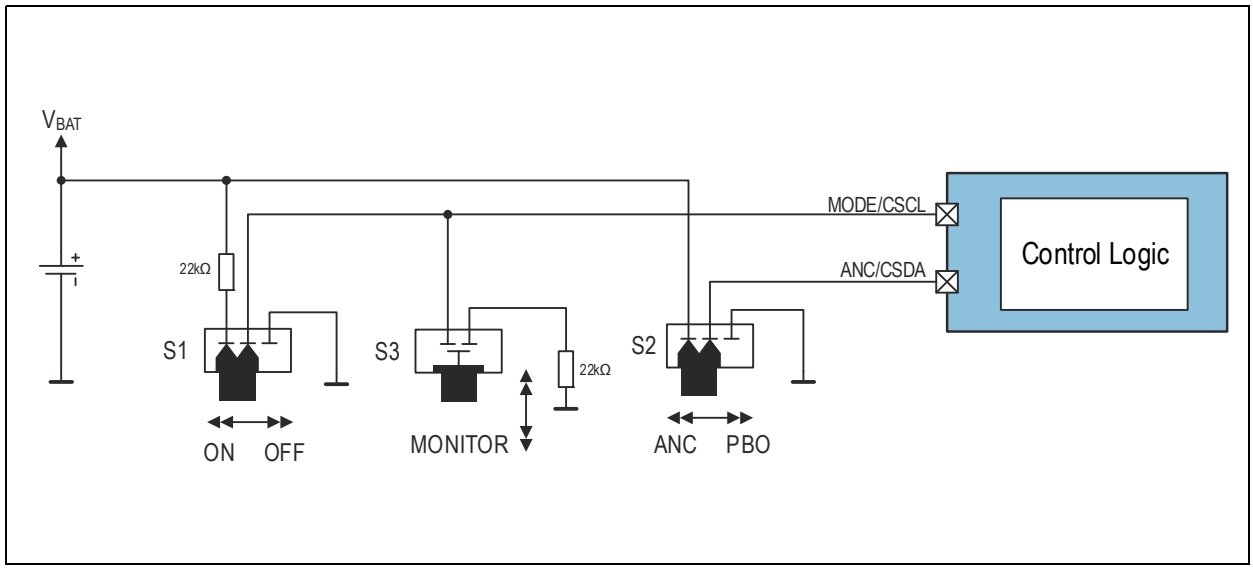


Full Slider Mode Timing Diagram: The diagram shows the necessary pin voltages and timings for different operation modes in Full Slider Mode configuration.

Slider Mode

Slider Mode is similar to Full Slider Mode with the only difference that it is possible to use a push button (S3) to enable and disable the Monitor Mode. Be aware that for Slider Mode operation bit *SLIDE_PWR_UP* has to be set to '1' and the *SLIDER_MON* bit has to be set to '0'.

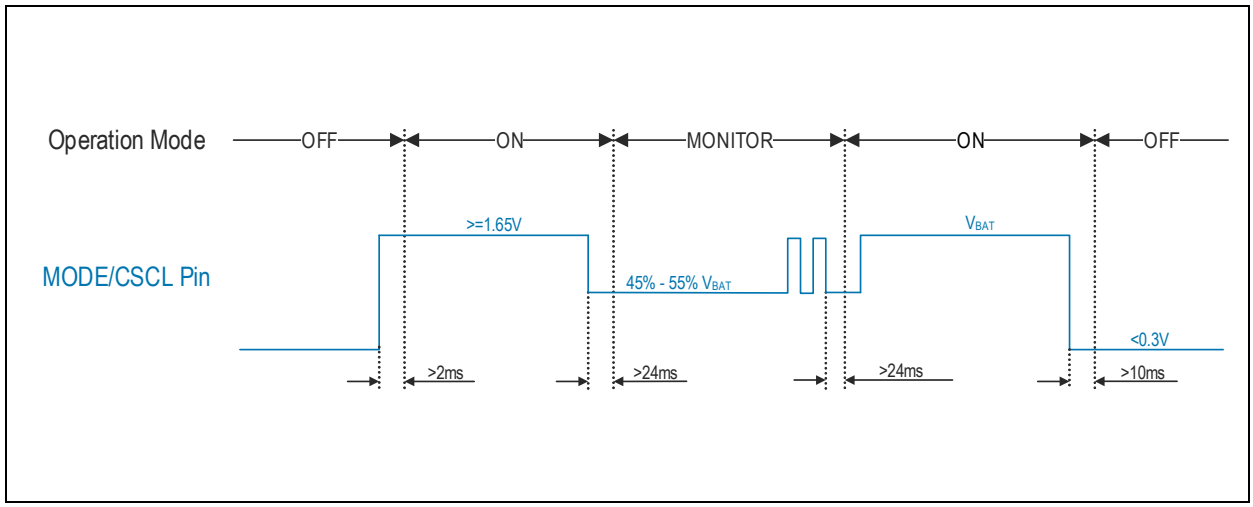
Figure 45:
Slider Mode



Slider Mode: The diagram shows the external connection of the switches and push button in slider mode.

The advantage of this mode compared to Full Slider Mode is the automatic hold function of the Monitor Mode. Once the push button S3 is pressed the device enters monitor mode. This mode stays active until the user pushes the button again.

Figure 46:
Slider Mode Timing Diagram

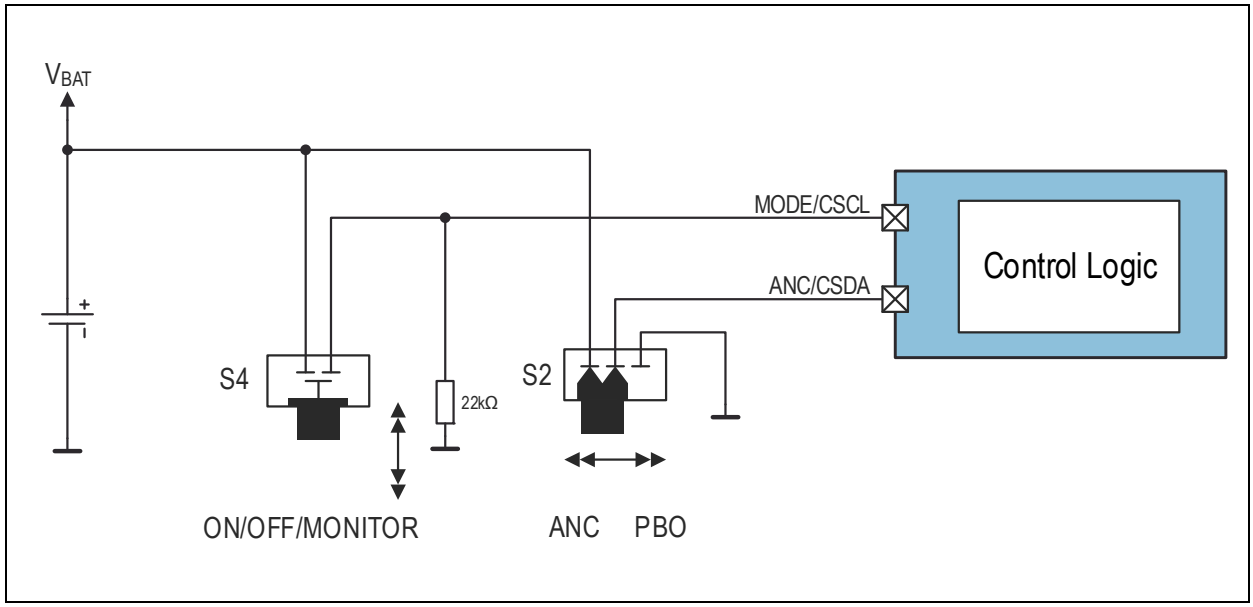


Slider Mode Timing Diagram: The diagram shows the necessary voltages and timings for different operation modes in Slider Mode configuration.

Push Button Mode

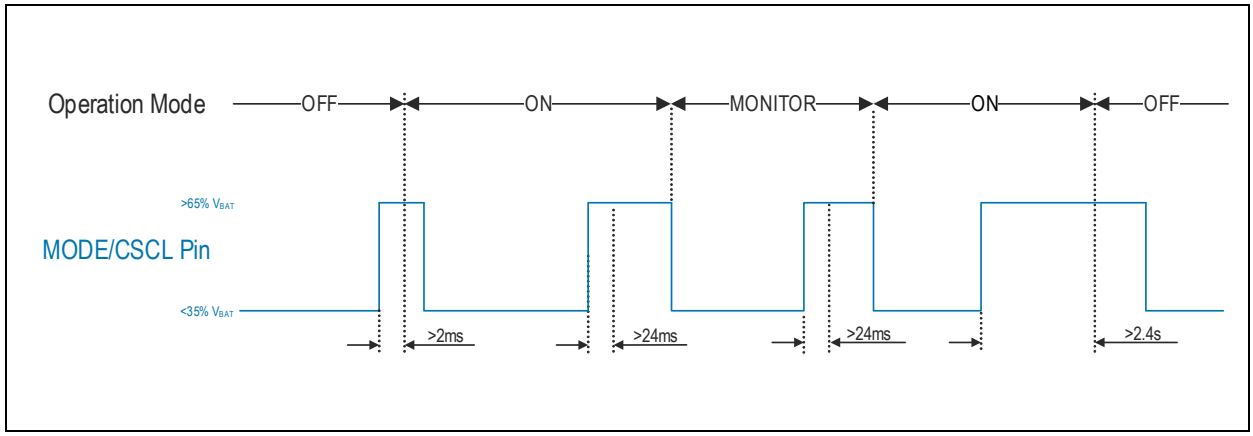
Push Button mode allows the user to control the device with a single normally open (NO) push button. A simple key press powers up the AS3512. Once the device is running, a long key press (~2.4 seconds) shuts the device down. As long as the device is active a short key press enters monitor mode. The monitor mode can be deactivated with a second, short key press. A timing diagram of this function is shown in Figure 48. If the monitor mode function is not desired, it is possible to deactivate the monitor mode by setting the bit *DISABLE_MONITOR* in register 0x15. The typical connection of the push button to the AS3412 is shown in Figure 47.

Figure 47:
Push Button Mode



Push Button Mode: The diagram shows the external connection of the switches and push button in slider mode.

Figure 48:
Push Button Timing Diagram

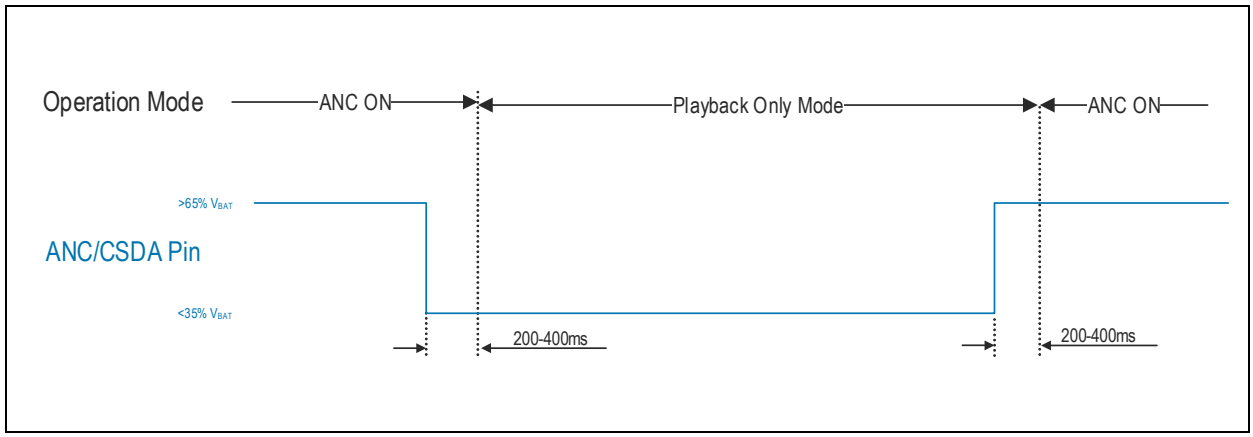


Push Button Mode Timing Diagram: The diagram shows the necessary voltages and timings for different operation modes in Push Button configuration.

Playback Only Mode

The active noise cancelling feature of the AS3412 can also be disabled with the ANC/CSDA pin. The ANC/CSDA pin has to be pulled high to enable the ANC function during startup (ANC MODE). If the pin is connected to ground, the chip enters playback only mode (PBO MODE) in which the ANC function is disabled. The operating mode of the line input mute switch, as well as the mixer input, can be defined in register *PBO_MODE*. The microphone amplifier shuts down automatically, but it is possible to control the operational amplifiers in this mode separately. Typically only the line input amplifiers and the headphone amplifier are enabled in the playback only mode. If this function is not desired you just need to pull the pin high through a 22kΩ resistor.

Figure 49:
Playback Only Mode Timing Diagram

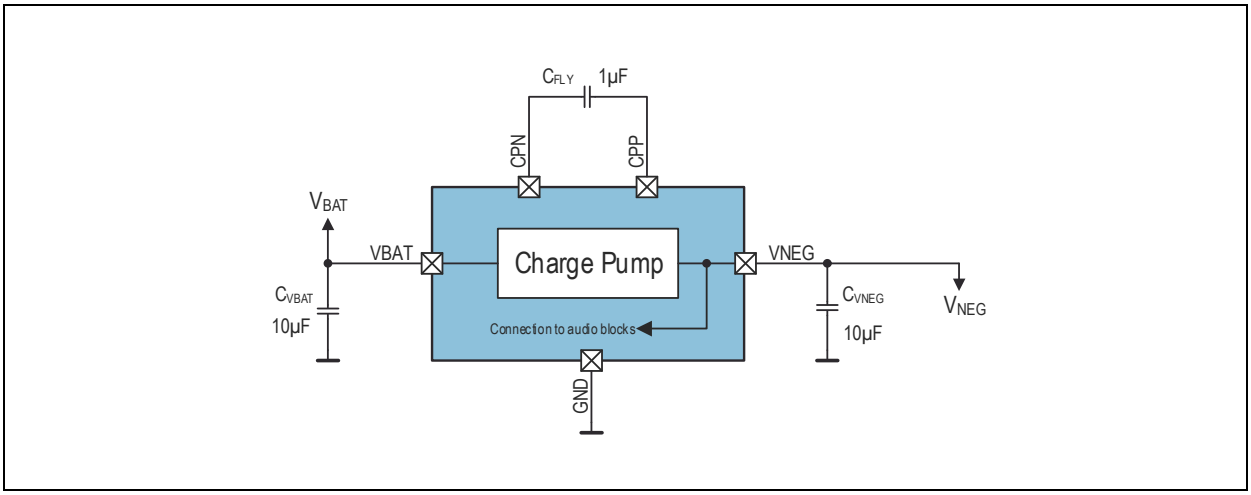


Playback Only Mode Timing Diagram: The diagram shows the necessary voltages and timings for different operation modes in Playback Only Mode.

V_{NEG} Charge Pump

The V_{NEG} charge pump uses one external 1µF ceramic capacitor (C_{FLY}) to generate a negative supply voltage out of the input voltage to supply all audio related blocks. This allows a true-ground headphone output with no need of external DC-decoupling capacitors.

Figure 50:
V_{NEG} Charge Pump



V_{NEG} Charge Pump: This figure shows the block diagram of the V_{NEG} charge pump that supplies all audio blocks of the AS3412.

The charge pump typically requires an additional input capacitor, C_{VBAT} of 10µF and output capacitor, C_{VNEG}, with the same size as the input capacitor. The flying capacitor, C_{FLY}, should be 1µF.

Parameter

V_{BAT} =1.8V, T_A= 25°C, unless otherwise specified.

Figure 51:
V_{NEG} Charge Pump Parameter

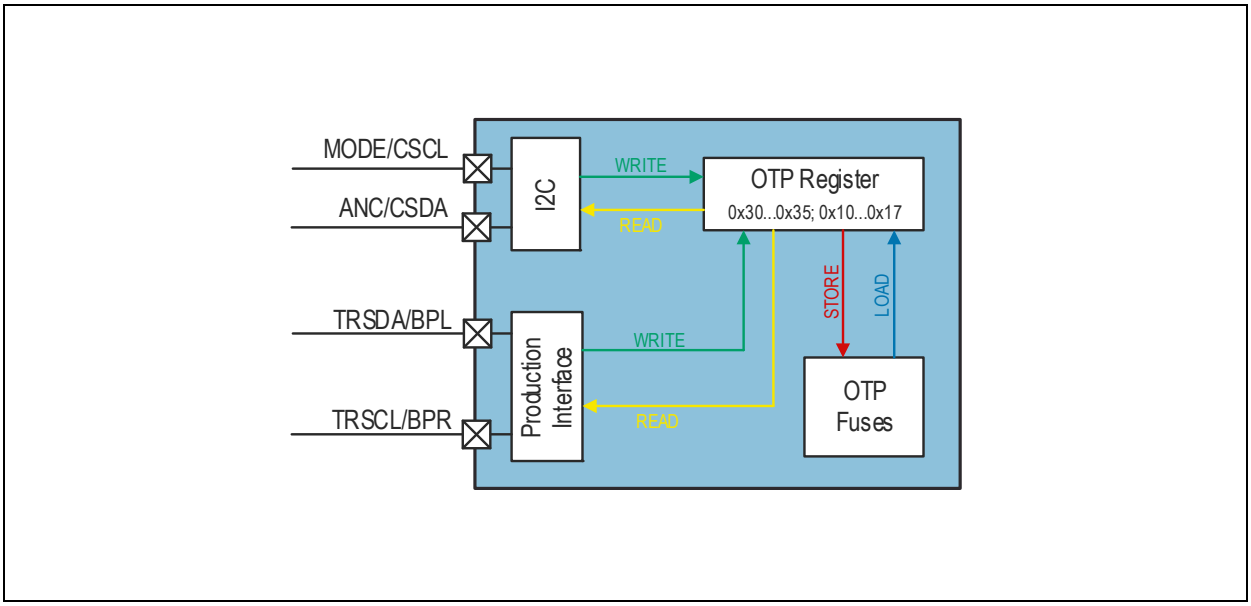
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input voltage	V_{BAT}	1.65		1.8	V
V_{OUT}	Output voltage	V_{NEG}	-1.45		-1.8	V
C_{FLY}	External flying capacitor			1		µF
C_{VBAT}	V_{BAT} input capacitor			10		µF
C_{VNEG}	V_{NEG} output capacitor			10		µF

VNEG Charge Pump Parameter: This table describes the electrical characteristics of the V_{NEG} charge pump.

OTP Memory and Internal Registers

The OTP (one-time programmable) memory consists of OTP registers (0x10 - 0x17 and 0x30 - 0x35) and OTP fuses. The OTP registers can be written as often as wanted but they are volatile memory cells. It is possible to access the OTP registers using the I^2C interface for “soft programming” the part or via the production programming interface pins (TRSDA and TRSCL). In order to store chip configuration data to the ANC chip, the OTP registers are linked together with the OTP fuses shown in Figure 52. The OTP fuse block is a shadow register of the OTP registers that are nonvolatile memory cells. These registers store chip parameters during power-down. Programming the fuses can be done three times and is a permanent change. In order to configure the ANC chip during startup the OTP fuse content is loaded to the OTP registers. The AS3412 offers 3 OTP fuse sets for storing the microphone gain making it possible to change the gain 2 times for re-calibration or other purposes. In order to determine the right register settings for microphone gain in production, as well as in the engineering design phase, the non-volatile OTP registers should be used without OTP programming. This allows you to configure all registers as many times as desired to find the best microphone gain calibration value. Once all the right register settings have been found, the OTP fuse block should be used to store these settings.

Figure 52:
Register Access



Register Access: This diagram shows the OTP and register architecture of the AS3412.

A single OTP cell can be programmed only once. By default, the cell is “0”; a programmed cell contains a “1”. Because it is not possible to reset a programmed bit from “1” to “0”, multiple OTP writes are possible, but only additional un-programmed “0”-bits can be programmed to “1”.

Independent of the OTP programming, it is possible to overwrite the OTP register temporarily if the chip is controlled via I^2C. The chip configuration can be stored for example in the flash memory of a Bluetooth- or wireless chipset and can be loaded to the ANC chip during startup of the device via the I^2C interface. Because the OTP fuses upload their contents into the OTP register at power-up, the new OTP settings from the microcontroller will overwrite the default settings of the AS3412. All I^2C OTP registers settings can be changed as many times as desired, but will be lost during power off.

OPT Registers and Fuses: The OTP registers are volatile memory cells which lose the content once the device is switched off. Multiple read and write commands are possible but in order to store chip settings during power off mode, the OTP fuses have to be used.

The OTP memory can be accessed in the following ways:

- LOAD Operation

  The LOAD operation reads the OTP fuses and loads the contents into the OTP register. A LOAD operation is automatically executed after each power-on-reset.

- WRITE Operation

  The WRITE operation allows a temporary modification of the OTP register. It does not program the OTP. This operation can be invoked multiple times and will remain set while the chip is supplied with power and while the OTP register is not modified with another WRITE or LOAD operation.

- READ Operation

  The READ operation reads the contents of the OTP register, for example to verify a WRITE command or to read the OTP memory after a LOAD command.

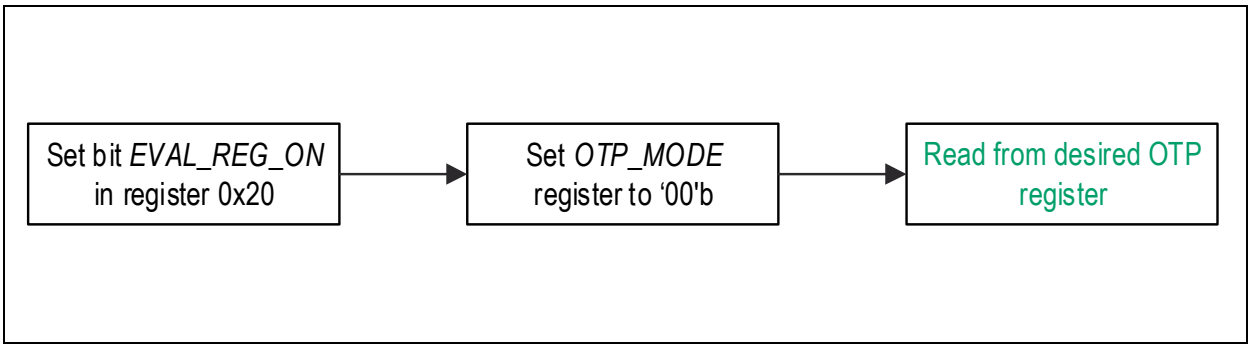
- STORE Operation

  The STORE operation programs the contents of the OTP register permanently into the OTP fuses. Don't use old or nearly empty batteries for programming the fuses.

OTP Read/Write and Load Access

With the OTP register architecture of the AS3412 it is important to know how to access the registers for reading and writing. Before an I²C read command can be sent there are two registers that have to be configured prior to the desired I²C read command. The flow chart in Figure 53 shows the correct read access sequence. The first step is to configure the *EVAL_REG_ON* register. This register enables access to the *OTP_MODE* register. The *OTP_MODE* register defines whether you want to read or write to the OTP registers. By setting the *OTP_MODE* register '00' we select OTP read access. Once the *OTP_MODE* register has been configured you can start reading from the OTP registers.

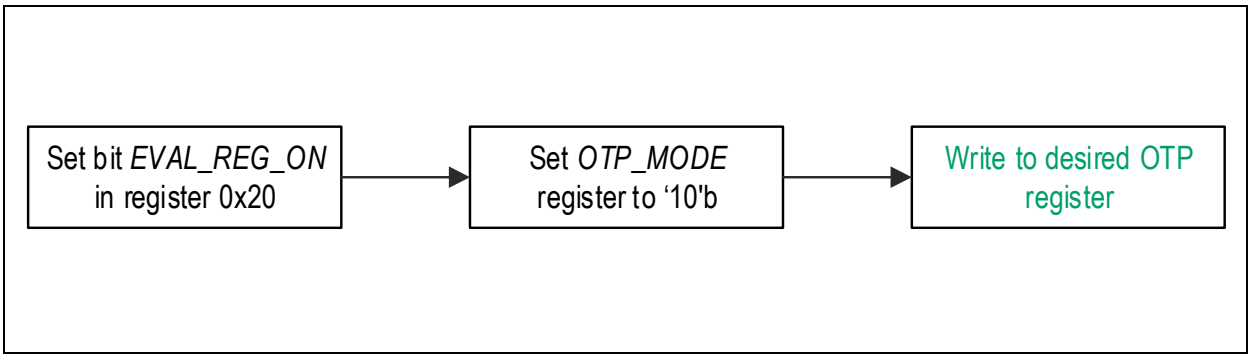
Figure 53:
OTP Read Access Flow Chart



OTP Read Access Flow Chart: This flow chart shows how to successfully read from an OTP register via the I²C or production trimming interface.

The principle for writing to a register is basically the same. The only difference is the configuration of the *OTP_MODE* register, shown in Figure 54. The first step is to enable the *OTP_MODE* register by setting the *EVAL_REG_ON* register to '1'. The next step is to configure the *OTP_MODE* register to '10' in order to select OTP write access. Now you can start writing to any OTP register of AS3412.

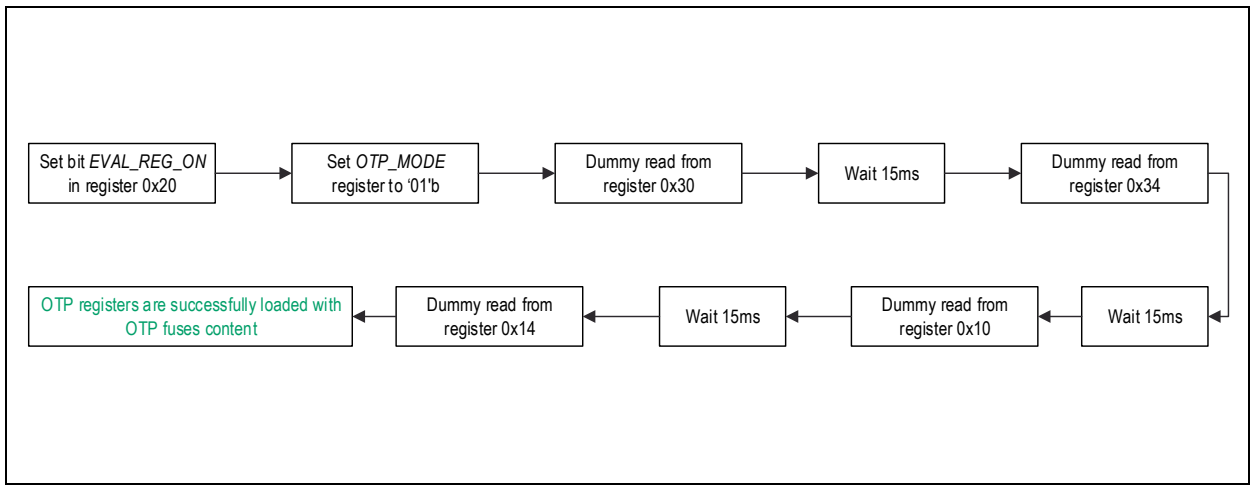
Figure 54:
OTP Write Access Flow Chart



OTP Write Access Flow Chart: This flow chart shows how to successfully write to an OTP register via the I²C or production trimming interface.

If you want to read out the OTP fuse content, the OTP load function is necessary. In order to load the OTP fuse content to the OTP registers, a special sequence is necessary, as shown in Figure 55.

Figure 55:
OTP Load Access Flow Chart

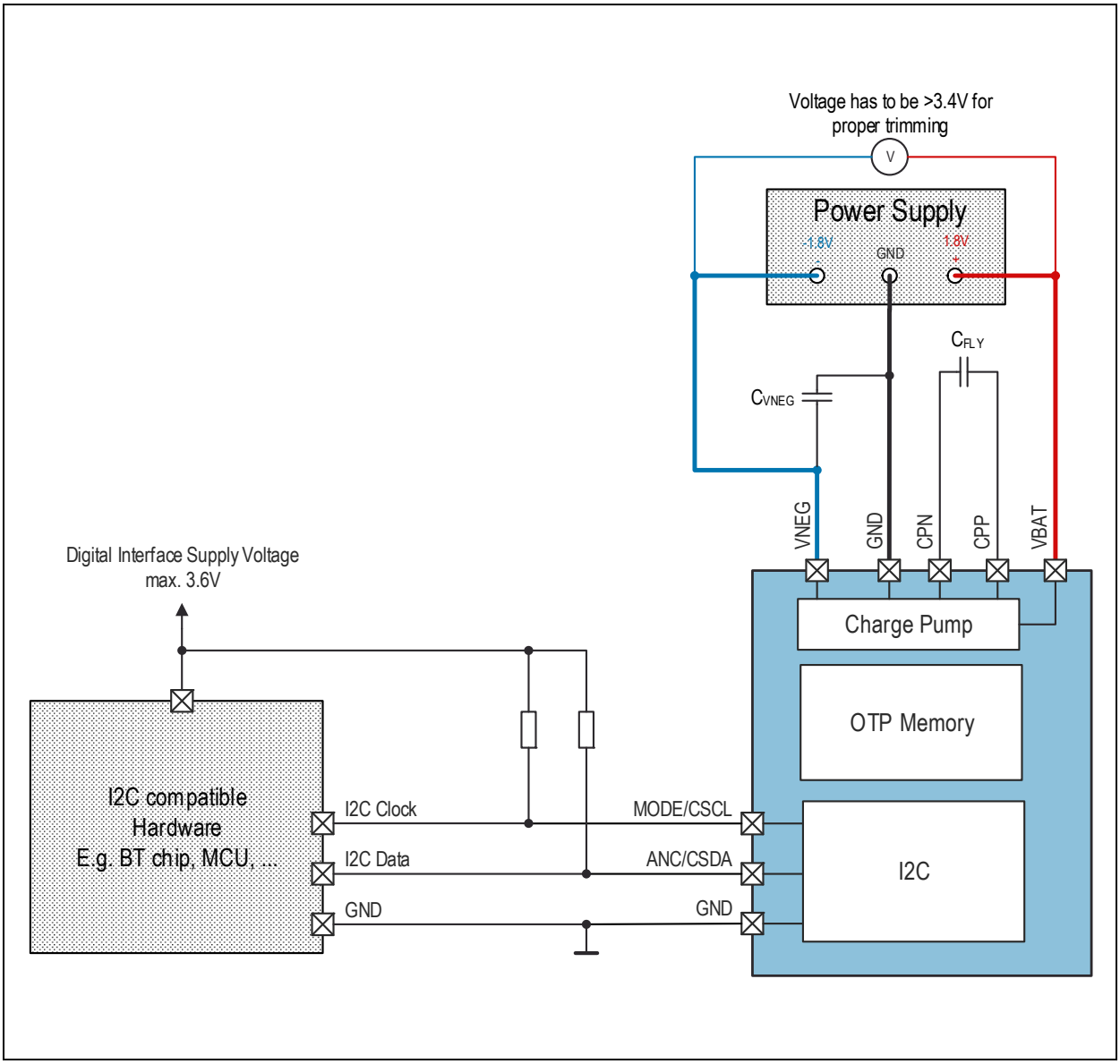


OTP Load Access Flow Chart: This flow chart shows how to successfully load the OTP fuse content back to the OTP register via the I²C or production trimming interface.

OTP Fuse Process

Many wireless applications, like Bluetooth single chips support programmable solutions, as well as ROM versions. As such, it is necessary for ROM versions to store microphone gain compensation data and the general ANC configuration inside the ANC chip. This is necessary because there is no other way to configure the ANC chip during startup. In order to guarantee successful trimming of AS3412 it is necessary to provide a decent environment for the trimming process. Figure 56 shows a principal block diagram for trimming the AS3412 properly in production using the I²C interface. The most important block is the external power supply. Usually it is possible to trim the AS3412 with a single supply voltage of min. 1.8V in laboratory environment, but as soon as it comes to mass production V_{NEG} supply buffering is highly recommended. As highlighted in the block diagram, it is mandatory to get a voltage difference between V_{POS} and V_{NEG} of 3.4V (minimum) to guarantee proper trimming of the device, therefore it is possible to buffer it externally with a negative power supply. The V_{NEG} voltage applied to VNEG pin must be lower than the voltage generated by the charge pump. This means if the typical V_{NEG} output voltage is -1.5V you can apply externally -1.7V. The charge pump enters then automatically skip mode.

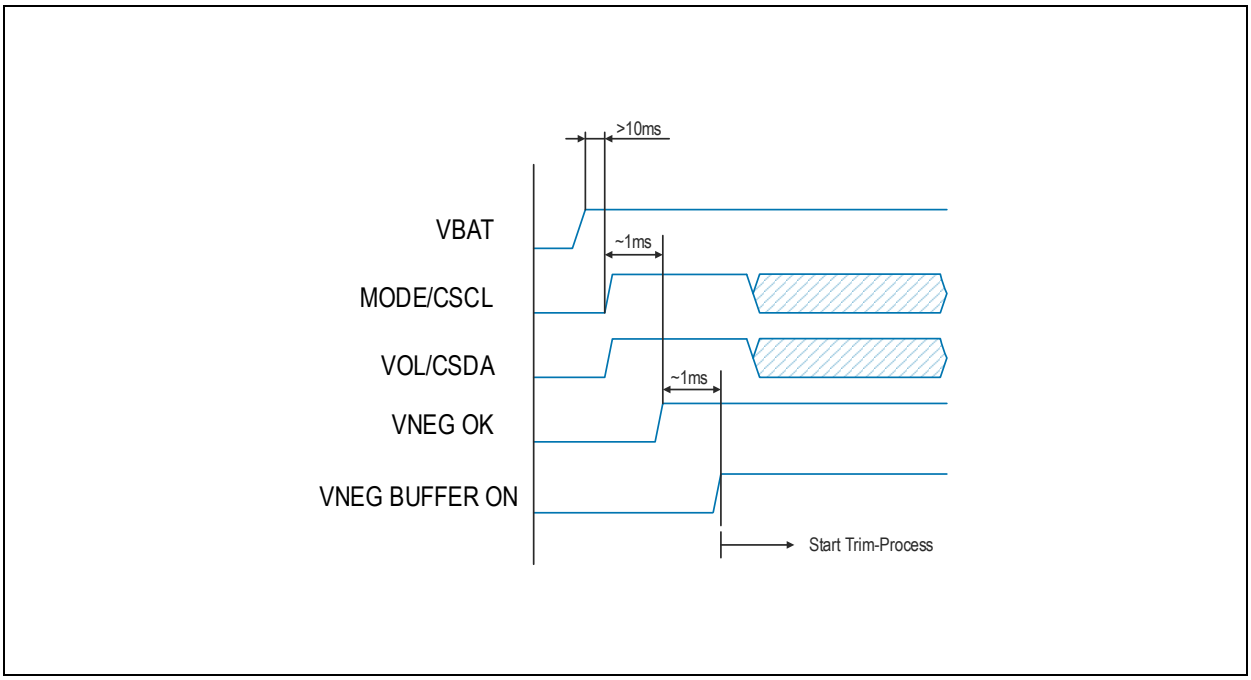
Figure 56:
Production Environment I²C Interface Trimming



I²C Trimming: This block diagram shows a general overview of the production environment when storing the register settings to the AS3412 using a standard I²C interface.

Timing is important, to avoid latch-up, when using an external buffer and switching on the ANC device. The timing diagram in Figure 57 shows that it is important that there is a certain delay requirement between VBAT and the MODE /CSCL pin. This delay is mandatory in order to guarantee that the device starts up properly. The MODE /CSCL pin powers up the ANC device. The whole sequence to power up the internal charge pump of the AS3412 takes approximately 1ms. Once V_{NEG} is settled the external V_{NEG} buffer (e.g. power supply) can be enabled in order to support the charge pump especially during the trim process.

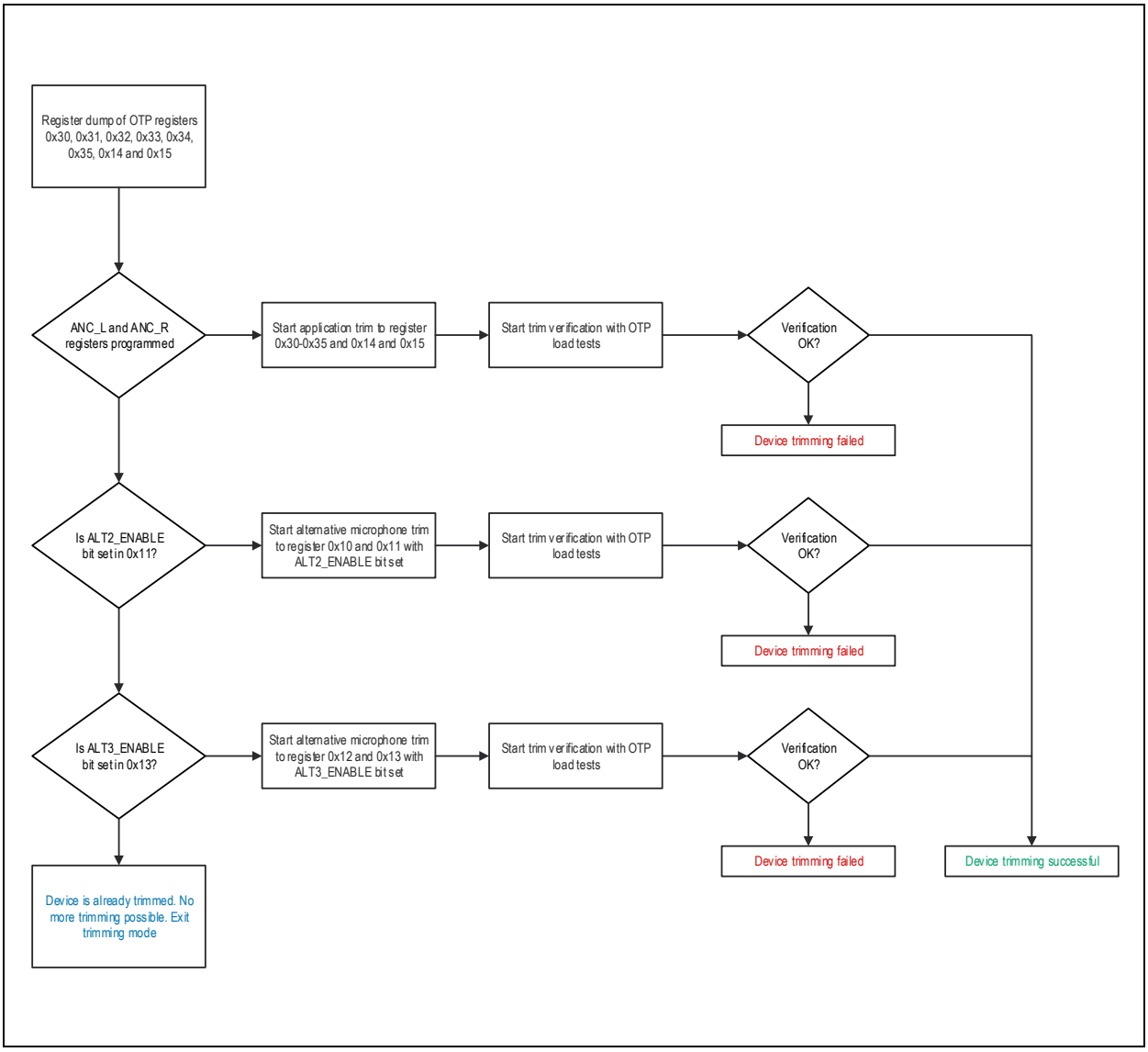
Figure 57:
Timing Diagram V_{NEG} Buffering



VNEG Buffer Timing: This timing diagram shows how to buffer the V_{NEG} supply during the OTP programming process.

To guarantee a successful trimming process it is important to follow the predefined trimming sequence shown in Figure 57. As a first step it is important to do a register dump of all OTP registers. This register backup in your system memory is a backup of all register settings and is necessary for verification after the trim process to make sure that all bits are trimmed correctly. Once the register dump has been done it is important to check registers 0x30 and 0x31. These registers typically indicate if the device is already trimmed or not. If both registers have the value 0x80 you can enter the trim mode and start the trimming process. Once trimming is done, the most important step is comparing the values trimmed to the device with the original register dump performed just before we started the actual trimming process. If the verification was successful we know that all bits have been trimmed correctly. What is important to mention is that the AS3412 has a couple of test bits inside which are by default set to '1'. We do not recommend overwriting these bits. Furthermore, it is important to know that it is not possible to change bits once they are trimmed. It is not possible to change a bit from '1' back to zero. If an additional trimming is done it is only possible to change bits from '0' to '1'. It is important that all necessary bits are trimmed exactly like in the block diagram shown in Figure 58.

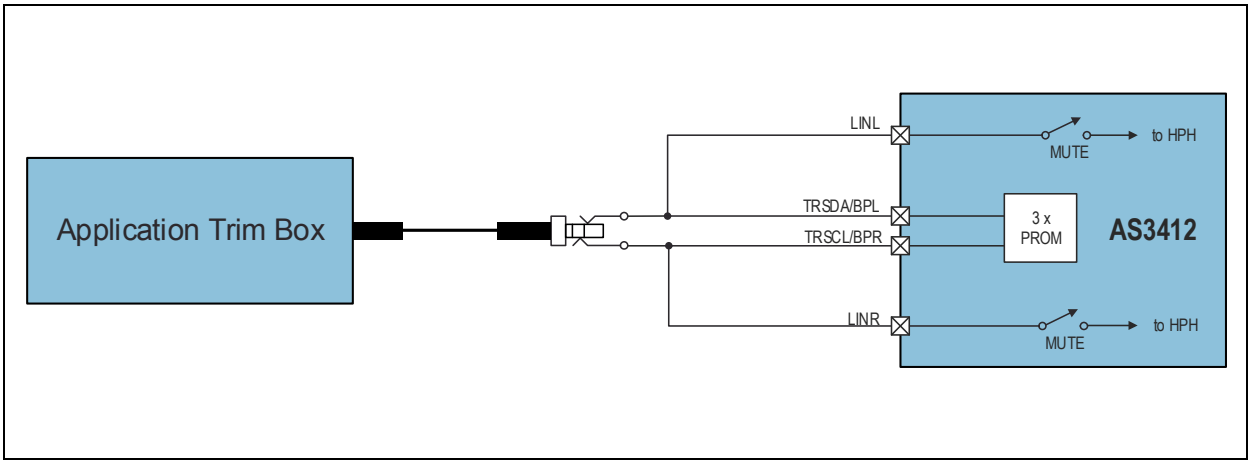
Figure 58:
OTP Programming Process



OTP Programming: This flow chart describes the OTP programming process in detail.

Besides production trimming using the I^2C interface, the AS3412 features a second unique trimming mechanism. This very special mode enables the analog music inputs of the AS3412 to become a production trimming input.

Figure 59:
Production Trim Box



Production Trim Box: This block diagram shows the connection of the Trim Box enabling the audio inputs to become a trim input for mass production.

With this new system, there is no need for mechanical potentiometers any more. Up to now, operators in production use screw drivers to fine tune the ANC performance of each headset. The disadvantage of this is reliability and cost of potentiometers. Additionally, operators are not always precise in their work, thus yielding inconsistent results. With the new production trimming system from ams there are no mechanical potentiometers required. The operator connects a 3.5mm audio jack to a trimming box and this box enables the audio input of the headset to become the ANC tuning input. This new feature also helps industrial designers of headset because there are no more considerations concerning leakage holes for the old mechanical trimming. Thus, the headset can be fully assembled and ready for the ANC test system at the end of the manufacturing process. The trim box can be easily controlled with an RS232 interface so it is also possible to create fully automated trimming systems. For further details please contact our local sales office; they can provide you with source code examples and application notes.

2 Wire Serial Interface

In order to configure the device using the evaluation software or a MCU the AS3412 features a serial two wire interface. The I²C address for the device can be found in Figure 60.

Figure 60:
I²C Slave Address

7 Bit I²C Address	8 Bit Read Address	8 Bit Write Address
0x47	0x8F	0x8E

I²C Slave Address Table: Shows the I²C address of the AS3412.

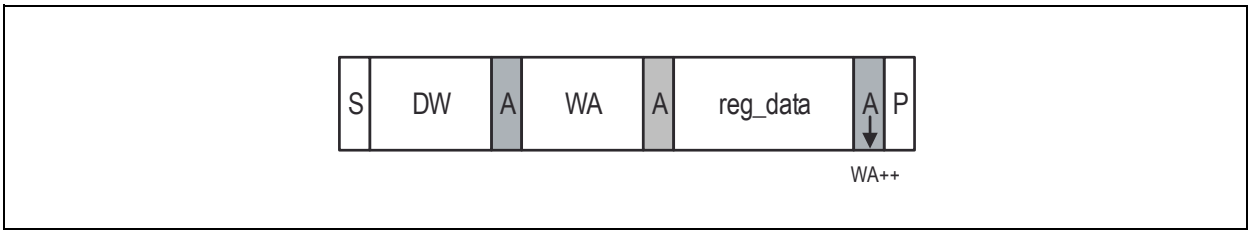
Protocol

Figure 61:
I²C Serial Interface Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 1110b (8Eh)
DR	Device address for read	R	1000 1111b (8Fh)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	during acknowledge
	AS3412 (=slave) transmits data		
	AS3412 (=slave) receives data		

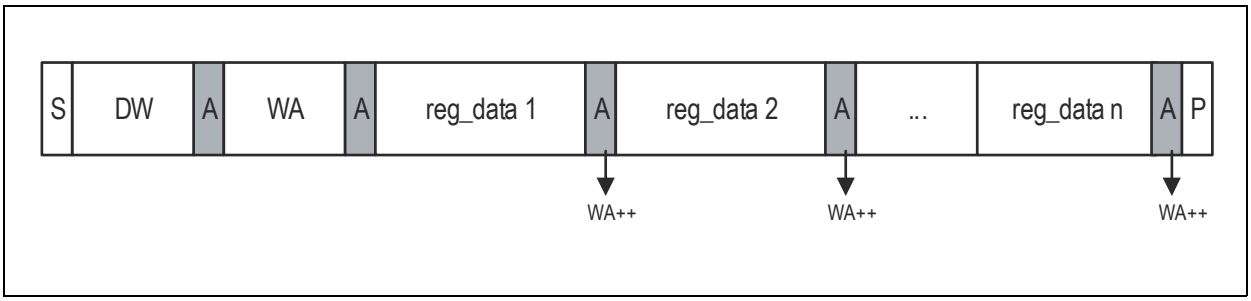
Symbol Definition: The table shows the symbol definitions being used in the explanations for the data transfer between master and slave.

Figure 62:
Byte Write



Byte Write: This figure shows the sequence for a byte write command.

Figure 63:
Page Write

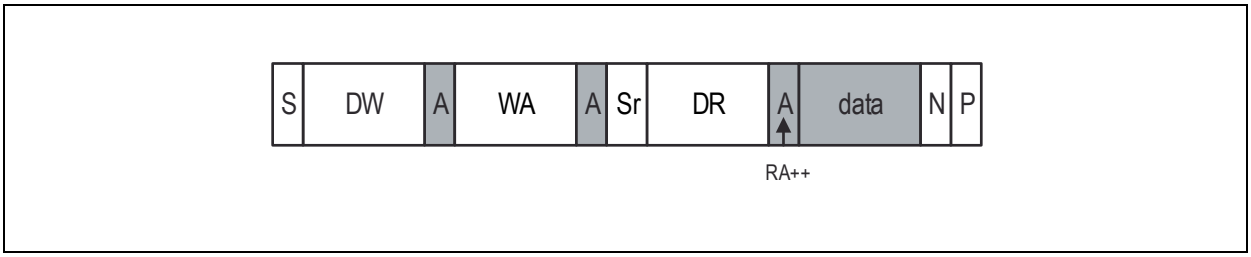


Page Write: This figure shows the sequence for a page write command.

Byte Write and Page Write formats are used to write data to the slave. The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes to subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 64:
Random Read



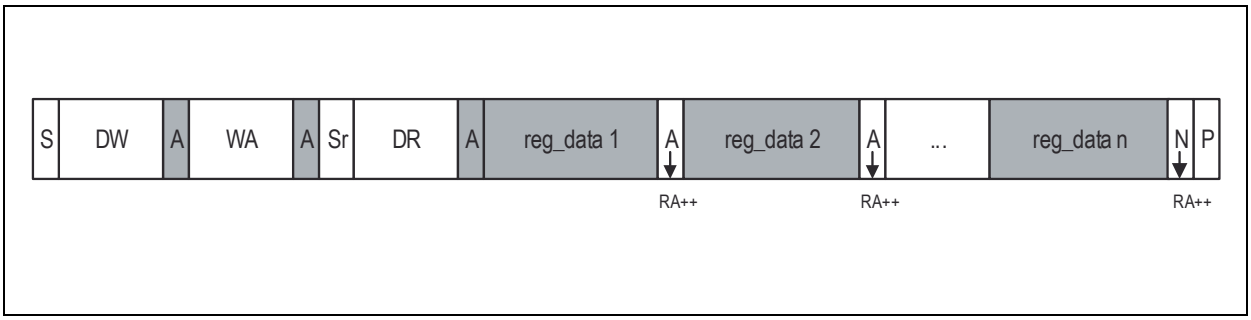
Random Read: This figure shows the I²C sequence for a random read function.

Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

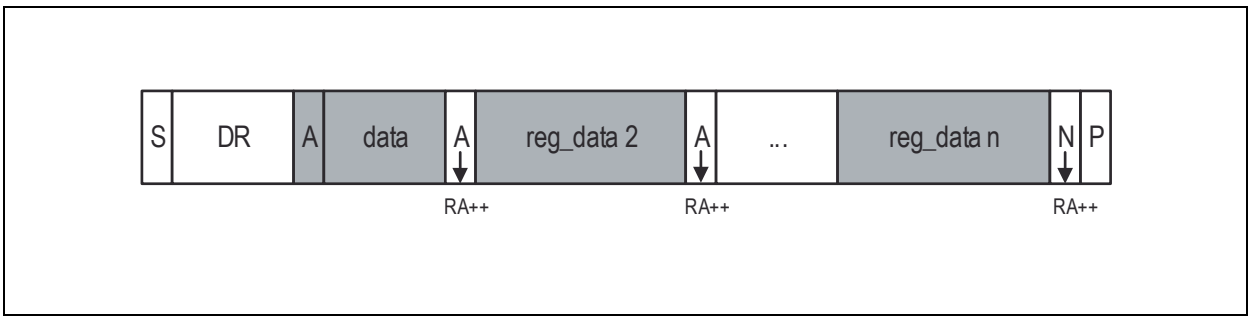
Figure 65:
Sequential Read



Sequential Read: This figure shows the read sequence for a sequential read command.

Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. Different from the Random Read, for a sequential read, the transferred register-data bytes are responded with an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and then generate the STOP condition.

Figure 66:
Current Address Read

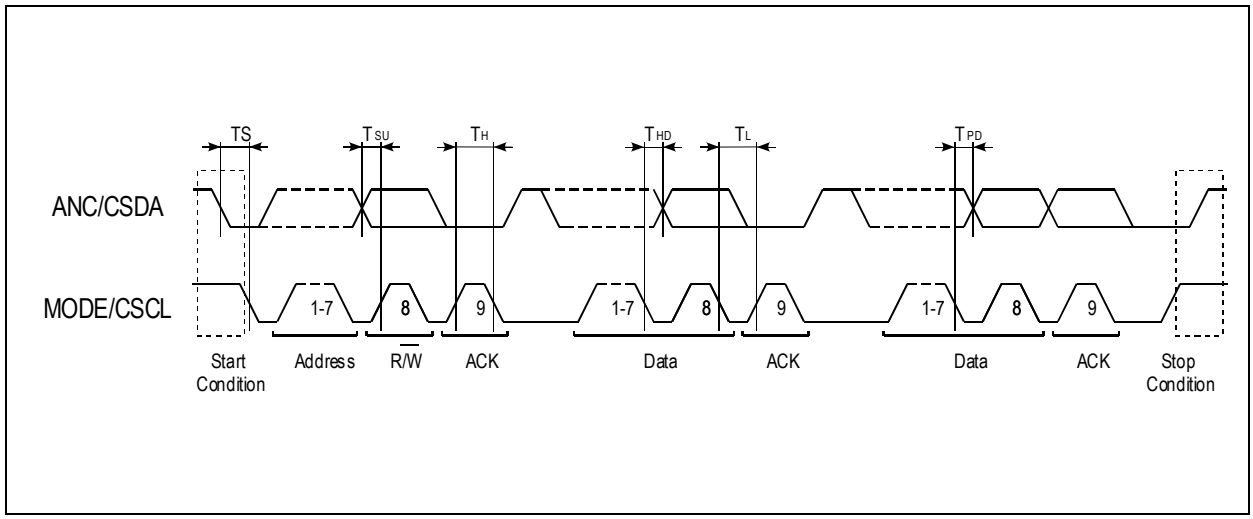


Current Address Read: This figure shows the I^2C read sequence.

To keep the access time as short as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes have to be responded with an acknowledge from the master. For termination of the transmission, the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

Parameter

Figure 67:
I²C Serial Timing



I²C Serial Timing: This figure shows the I²C timing diagram.

V_{BAT} =1.8V, T_A=25°C, unless otherwise specified.

Figure 68:
I²C Serial Interface Parameter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CSL}	CSCL, CSDA Low Input Level	(max 30% V_{BAT})	0	-	0.42	V
V_{CSH}	CSCL, CSDA High Input Level	CSCL, CSDA (min 70% V_{BAT})	1.16	-		V
HYST	CSCL, CSDA Input Hysteresis		200	450	800	mV
V_{OL}	CSDA Low Output Level	at 3mA	-	-	0.4	V
Tsp	Spike insensitivity		50	100	-	ns
T_H	Clock high time	max. 400kHz clock speed	500			ns
T_L	Clock low time	max. 400kHz clock speed	500			ns
T_{SU}		CSDA has to change T_{SU} before rising edge of CSCL	250	-	-	ns
T_{HD}		No hold time needed for CSDA relative to rising edge of CSCL	0	-	-	ns
TS		CSDA H hold time relative to CSDA edge for start/stop/rep_ start	200	-	-	ns
T_{PD}		CSDA prop delay relative to low going edge of CSCL		50		ns

I²C Serial Interface Parameter: This table shows the serial interface timing parameter.

Register Description

Register Overview

Figure 69:
Register Overview

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
System Registers									
20h	SYSTEM	DESIGN_VERSION<3:0> 1111				EVAL_REG_ON	-	-	PWR_HOLD
21h	PWR_READ	-	LOW_BAT	PWRUP COMPLETE	HPH_ON	MIC_ON	-	MICS_CP_ON	MICS_ON
2h-2Fh	Reserved								
OTP Registers									
10h	ANC_R2	TEST_BIT_1	-	MICR_VOL_OTP2<5:0> Gain from MICR to QMICR or Mixer = 0dB...+31dB; MUTE and 63 steps of 0.5dB					
11h	ANC_L2	ALT2_ENABLE	-	MICL_VOL_OTP2<5:0> Gain from MICL to QMICL or Mixer = 0dB...+31dB; MUTE and 63 steps of 0.5dB					
12h	ANC_R3	TEST_BIT_2	-	MICR_VOL_OTP3<5:0> Gain from MICR to QMICR or Mixer = 0dB...+31dB; MUTE and 63 steps of 0.5dB					
13h	ANC_L3	ALT3_ENABLE	-	MICL_VOL_OTP3<5:0> Gain from MICL to QMICL or Mixer = 0dB...+31dB; MUTE and 63 steps of 0.5dB					
14h	ANC_MODE	HPH_MUX<1:0> 0: MIC; 1: OP1; 2: Do not use; 3: Not connected		-	LIN_MUTE	-	-	OP1R_ON	OP1L_ON

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
15h	MON_MODE	MON_HPH_MUX<1:0> 0: MIC; 1: OP1; 2: Do not use; 3: -		-	MON_LIN_ MUTE	-	-	SLIDER_MON	DISABLE_ MONITOR
16h	PBO_MODE	TEST_BIT_4	NO_PBO	-	PBO_LIN_MUTE	-	-	PBO_OP1R_ ON	PBO_OP1L_ ON
17h	ECO	SLIDE_PWR_ UP	-	-	-	ENABLE_HPH_ ECO	ENABLE_MIC_ ECO	-	ENABLE_ OPAMP_ECO
30h	ANC_R	TEST_BIT_3.1	-	MICR_VOL<5:0> Gain from MICR to QMICR or Mixer = 0dB...+31dB; MUTE and 63 steps of 0.5dB					
31h	ANC_L	TEST_BIT_6	-	MICL_VOL<5:0> Gain from MICL to QMICL or Mixer = 0dB...+31dB; MUTE and 63 steps of 0.5dB					
32h	MIC_MON_R	-	-	MICR_MON<5:0> Gain from MICR to QMICL/R = 0dB...+31dB; MUTE and 63 steps of 0.5dB if MON_MODE is active					
33h	MIC_MON_L	-	-	MICL_MON<5:0> Gain from MICL to QMICL/R = 0dB...+31dB; MUTE and 63 steps of 0.5dB if MON_MODE is active					
34h	MODE_1	MICS_CP_OFF	MICS_OFF	MIC_AGC_ON	MIC_OFF	-	CP_OFF	HPH_OFF	-
35h	MODE_2	TEST_BIT_7	-	-	-	MICS_DC_OFF	DELAY_HPH_ MUX	HPH_MODE 0: Stereo 1: Mono Differential	I2C_MODE

Addr	Name	b7	b6	b5	b4	b3	b2	b1	b0
Evaluation Registers									
3Dh	EVAL	EVAL_ON	-	-	MASTER_ LIN_MUTE	MON_MODE	PBO_MODE	MICR_MUTE	MICL_MUTE
3Eh	CONFIG_1					EXTBURNCLK			
3Fh	CONFIG_2			TM34	BURNSW	TM_REG34-35	TM_REG30-33	OTP_MODE<1:0> 0: READ; 1: LOAD; 2: WRITE; 3: BURN	

Register Overview: This table provides a handy overview of all AS3412 registers.

Detailed Register Description

System Registers

Figure 70:
SYSTEM Register Description

Name	Address	Default Value
SYSTEM	0x20	81h
This register contains control bits for monitor mode, OTP register and power up/down functions.		

Bit	Bit Name	Default	Access	Bit Description
7:4	DESIGN_VERSION	1111	R	Design version number to identify the design version of the AS3412. 1111: for chip version 1v0
3	EVAL_REG_ON	0	R/W	This register controls read and write access to the OTP register banks. **0: Normal operation** 1: Enables writing to register 0x3D, 0x3E and 0x3F to configure the OTP and set the access mode.
0	PWR_HOLD	1	R/W	This bit allows an MCU using the I^2C interface a power down of the AS3412. A start condition on the I^2C interface will wake up the device again. This function works only if the I2C_MODE bit is set before you write this register. 0: Power up hold is cleared and chip powers down **1: It is automatically set to on after power on**

Figure 71:
PWR_SET Register Description

Name	Address	Default Value
PWR_READ	0x21	0x3F
A readout of this register returns the status of each block o f the chip.		

Bit	Bit Name	Default	Access	Bit Description
6	LOW_BAT	x	R	V_{BAT} supervisor status **0: V_{BAT} is above brown out level** 1: V_{BAT} has reached brown out level
5	PWRUP_ COMPLETE	x	R	Power-up sequencer status **0: Power-up sequence incomplete** 1: Power-up sequence completed
4	HPH_ON	0	R	This register returns the power status of the headphone amplifier. **0: Headphone amplifier switched off** 1: Headphone amplifier switched on
3	MIC_ON	0	R	This register returns the power status of the microphone preamplifier. **0: Microphone preamplifier switched off** 1: Microphone preamplifier switched on
1	MICS_CP_ON	0	R	This register returns the power status of the microphone charge pump. **0: Microphone charge pump switched off** 1: Microphone charge pump switched on
0	MICS_ON	0	R	This register returns the power status of the microphone supply (MICS). **0: Microphone supply switched off** 1: Microphone supply switched on

OTP Register

Figure 72:
ANC_R2 Register Description

Name	Address	Default Value
ANC_R2	0x10	80h
The ANC_R2 register configures the gain for the right microphone input. This register is the first alternative microphone gain register for OTP programming in case the ANC_R register is already programmed.		

Bit	Bit Name	Default	Access	Bit Description
7	TEST_BIT_1	1	R	Test register. Please do not write this register.
5:0	MICR_VOL_ OTP2<6:0>	000 0000	R/W	Volume settings for right microphone input, adjustable in 63 steps of 0.5dB **00 0000: MUTE** 00 0001: 0 dB gain 00 0010: 0.5dB gain 00 0011: 1.0dB gain … 11 1110: 30.5dB gain 11 1111: 31dB gain

Figure 73:
ANC_L2 Register Description

Name	Address	Default Value
ANC_L2	0x11	00h
The ANC_L2 Register configures the gain for the left microphone input. This register is the first alternative microphone gain register for OTP programming in case the ANC_L register is already programmed.		

Bit	Bit Name	Default	Access	Bit Description
7	ALT2_ENABLE	0	R/W	In case the register is being used for microphone programming this bit has to be set. The bit is being used by the internal state machine of the AS3412 to determine which alternative microphone gain register has to be used during startup. **0: Microphone registers 0x10 and 0x11 are not active** 1: Microphone registers 0x10 and 0x11 are active. Gain settings in registers 0x30 and 0x31 are ignored
5:0	MICL_VOL_ OTP2<6:0>	000 0000	R/W	Volume settings for left microphone input, adjustable in 63 steps of 0.5dB **00 0000: MUTE** 00 0001: 0dB gain 00 0010: 0.5dB gain 00 0011: 1.0dB gain … 11 1110: 30.5dB gain 11 1111: 31dB gain

Figure 74:
ANC_R3 Register Description

Name	Address	Default Value
ANC_R3	0x12	80h
The ANC_R3 Register configures the gain for the right microphone input. This register is the second alternative microphone gain register for OTP programming in case the ANC_R and ANC_R2 registers are already programmed.		

Bit	Bit Name	Default	Access	Bit Description
7	TEST_BIT_6	1	R	Test register. Please do not write this register.
5:0	MICR_VOL_ OTP3<6:0>	000 0000	R/W	Volume settings for right microphone input, adjustable in 63 steps of 0.5dB **00 0000: MUTE** 00 0001: 0dB gain 00 0010: 0.5dB gain 00 0011: 1.0dB gain … 11 1110: 30.5dB gain 11 1111: 31dB gain

Figure 75:
ANC_L3 Register Description

Name	Address	Default Value
ANC_L3	0x13	00h
The ANC_L3 Register configures the gain for the left microphone input. This register is the second alternative microphone gain register for OTP programming in case the ANC_L and ANC_L2 registers are already programmed.		

Bit	Bit Name	Default	Access	Bit Description
7	ALT3_ENABLE	0	R/W	In case the register is being used for microphone programming this bit has to be set. The bit is being used by the internal state machine of the AS3412 to determine which alternative microphone gain register has to be used during startup. **0: Microphone registers 0x12 and 0x13 are not active** 1: Microphone registers 0x12 and 0x13 are active. Gain settings in registers 0x30, 0x31, 0x10 and 0x11 are ignored.
5:0	MICL_VOL_ OTP3<6:0>	000 0000	R/W	Volume settings for left microphone input, adjustable in 63 steps of 0.5dB **00 0000: MUTE** 00 0001: 0dB gain 00 0010: 0.5dB gain 00 0011: 1.0dB gain … 11 1110: 31dB gain 11 1111: 31dB gain

Figure 76:
ANC_MODE Register Description

Name	Address	Default Value
ANC_MODE	0x14	00h
The ANC_MODE register controls various settings for the chipset in active noise cancelling mode like which amplifiers are enabled as well as which audio inputs are active.		

Bit	Bit Name	Default	Access	Bit Description
7:6	HPH_MUX<1:0>	00	R/W	This register selects the ANC input source for the headphone amplifier in ANC mode. Depending on the register setting the outputs of microphone preamplifier or OPAMP1 can be connected to the headphone amplifier input. It is also possible to disconnect all ANC input sources which is sometimes desired in monitor mode. **00: QMIC outputs are connected to HPH input** 01: OP1 outputs are connected to HPH input 10: Do not use this setting 11: Nothing connected to HPH input except line input in case it is enabled.
4	LIN_MUTE	0	R/W	This bit mutes the line input signal. If the bit is set the line input signal is disconnected from the headphone amplifier. **0: Line input signal enabled** 1: Line input signal muted
1	OP1R_ON	0	R/W	This register enables the right channel of OPAMP 1 in ANC mode. **0: Right OP1 is switched off** 1: Right OP1 is switched on
0	OP1L_ON	0	R/W	This register enables the left channel of OPAMP 1 in ANC mode. **0: Left OP1 is switched off** 1: Left OP1 is switched on

Figure 77:
MONITOR_MODE Register Description

Name	Address	Default Value
MONITOR_MODE	0x15	00h
The MONITOR_MODE register controls various settings for the chipset in monitor mode like line input monitor mode attenuation as well as which audio inputs are active.		

Bit	Bit Name	Default	Access	Bit Description
7:6	MON_HPH_ MUX<1:0>	00	R/W	This register selects the ANC input source for the headphone amplifier in monitor mode. Depending on the register setting the outputs of microphone preamplifier, OPAMP1, OPAMP2 can be connected to the headphone amplifier input. **00: QMIC outputs are connected to HPH input** 01: OP1 outputs are connected to HPH input 10: Do not use this setting 11: Nothing connected to HPH input except line input.
4	MON_LIN_MUTE	0	R/W	This bit mutes the audio line input pin in Monitor mode. **0: Line input enabled in Monitor mode** 1: Line input muted in Monitor mode
1	SLIDER_MON	0	R/W	This bit enables the Full Slider Mode configuration. Please mind that this bit must not be set without setting SLIDE_PWR_UP to '1'. **0: Slider Mode activated** 1: Full Slider Mode activated
0	DISABLE_ MONITOR	0	R/W	This bit disables the monitor mode in push button control mode. **0: Monitor mode enabled** 1: Monitor mode disabled

Figure 78:
PBO_MODE Register Description

Name	Address	Default Value
PBO_MODE	0x16	0x00
The PBO_MODE register controls various settings for the chipset in playback only mode like which amplifiers are enabled as well as which audio inputs are active.		

Bit	Bit Name	Default	Access	Bit Description
7	TEST_BIT_4	1	R	Test register. Please do not write this register.
6	NO_PBO	0	R/W	This bit disables the playback only mode function. No external pull up resistor is required on ANC / CSDA pin is necessary if this bit is set to '1' **0: Playback only mode enabled** 1: Playback only mode disabled
4	PBO_LIN_MUTE	0	R/W	This bit enables the eco mode of the microphone preamplifier. **0: Power save function disabled** 1: Power save function enabled
1	PBO_OP1R_ON	0	R/W	This register enables the right channel of OPAMP 1 in playback only mode. **0: Right OP2 is switched off** 1: Right OP2 is switched on
0	PBO_OP1L_ON	0	R/W	This register enables the left channel of OPAMP 1 in playback only mode. **0: Left OP2 is switched off** 1: Left OP2 is switched on

Figure 79:
ECO Register Description

Name	Address	Default Value
ECO	0x17	0x00
This register controls the economic (ECO) mode for all analog audio blocks. Furthermore it includes also other general settings.		

Bit	Bit Name	Default	Access	Bit Description
7	SLIDE_PWR_UP	0	R/W	This bit enables the slide switch control mode of the AS3512. If this bit is programmed the device can be powered up and powered down via a slide switch. **0: Slide switch control disabled** 1: Slide switch control enabled
3	ENABLE_HPH_ ECO	0	R/W	This bit enables the eco mode of the headphone amplifier. **0: Power save function disabled** 1: Power save function enabled
2	ENABLE_MIC_ ECO	0	R/W	This bit enables the eco mode of the microphone amplifier. **0: Power save function disabled** 1: Power save function enabled
0	ENABLE_OPAMP_ ECO	0	R/W	This bit enables the eco mode of the operational amplifier amplifiers for ANC filter design. **0: Power save function disabled** 1: Power save function enabled

Figure 80:
ANC_R Register Description

Name	Address	Default Value
ANC_R	0x30	80h
The ANC_R Register configures the gain for the right microphone input.		

Bit	Bit Name	Default	Access	Bit Description
7	TEST_BIT_5	1	R/W	Please do not write this register.
5:0	MICR_VOL<5:0>	000 0000	R/W	Volume settings for right microphone input, adjustable in 63 steps of 0.5dB **00 0000: MUTE** 00 0001: 0dB gain 00 0010: 0.5dB gain 00 0011: 1dB gain … 11 1110: 30dB gain 11 1111: 31dB gain

Figure 81:
ANC_L Register Description

Name	Address	Default Value
ANC_L	0x31	0x80
The ANC_L Register configures the gain for the left microphone input.		

Bit	Bit Name	Default	Access	Bit Description
7	TEST_BIT_6	1	R/W	Please do not write this register.
5:0	MICL_VOL_ OTP<5:0>	000 0000	R/W	Volume settings for left microphone input, adjustable in 63 steps of 0.5dB **00 0000: MUTE** 00 0001: 0dB gain 00 0010: 0.5dB gain 00 0011: 1.0dB gain … 11 1110: 30.5dB gain 11 1111: 31dB gain

Figure 82:
MIC_MON_R Register Description

Name	Address	Default Value
MIC_MON_R	0x32	0x00
This register controls the microphone gain in monitor mode for the right microphone channel.		

Bit	Bit Name	Default	Access	Bit Description
5:0	MICR_MON<5:0>	00 0000	R/W	Monitor mode gain setting for right microphone input adjustable in 63 steps of 0.5dB **00 0000: MUTE** 00 0001: 0.5dB gain 00 0010: 1dB gain 00 0011: 1.5dB gain … 11 1110: 30.5dB gain 11 1111: 31dB gain

Figure 83:
MIC_MON_L Register Description

Name	Address	Default Value
MIC_MON_L	0x33	0x00
This register controls the microphone gain in monitor mode for the left microphone channel.		

Bit	Bit Name	Default	Access	Bit Description
5:0	MICL_MON<5:0>	00 0000	R/W	Monitor mode gain setting for left microphone input adjustable in 63 steps of 0.5dB **00 0000: MUTE** 00 0001: 0.5dB gain 00 0010: 1dB gain 00 0011: 1.5dB gain … 11 1110: 30.5dB gain 11 1111: 31dB gain

Figure 84:
MODE_1 Register Description

Name	Address	Default Value
MODE_1	0x34	0x00
This register controls miscellaneous settings of the AS3512.		

Bit	Bit Name	Default	Access	Bit Description
7	MICS_CP_OFF	0	R/W	This bit controls the microphone supply charge pump. The microphone charge pump has a second function besides the bias voltage generation for microphones. It is also used to disable the integrated music bypass switch if the AS3412 is active. In case the integrated bypass switch is used in an application the MICS_CP_OFF bit must not be set to '1'. **0: Microphone supply charge pump enabled** 1: Microphone supply charge pump disabled
6	MICS_OFF	0	R/W	This bit controls the microphone supply. In case this bit is set to '1' the MICS pin is disconnected from the internal microphone supply. **0: Microphone supply switched on** 1: Microphone supply switched off
5	MIC_AGC_ON	0	R/W	This bit disables the automatic gain control of the microphone preamplifier. **0: AGC disabled** 1: AGC enabled
4	MIC_OFF	0	R/W	This bit powers down the microphone preamplifier. **0: Microphone preamplifier enabled** 1: Microphone preamplifier disabled
2	CP_OFF	0	R/W	This bit disables the V_{NEG} charge pump in case there is already a negative supply present in a system. **0: V_{NEG} charge pump enabled** 1: V_{NEG} charge pump enabled
1	HPH_OFF	0	R/W	This bit allows the user to power down headphone amplifier in case it is not used in the final application in order to save system power. **0: Headphone amplifier enabled** 1: Headphone amplifier disabled

Figure 85:
MODE_2 Register Description

Name	Address	Default Value
MODE_2	0x35	0x00
This register controls miscellaneous settings of the AS3512.		

Bit	Bit Name	Default	Access	Bit Description
7	TEST_BIT_7	1	R/W	Test register. Please do not write this register.
3	MICS_DC_OFF	0	R/W	This bit disables the internal microphone supply discharge function if the microphone supply is switched off. **0: MICS discharge enabled** 1: MICS discharge disabled
2	DELAY_HPH_MUX	0	R/W	With this bit it is possible to delay the HPH_MUX setting during startup of the device to avoid unwanted pop noise in case of long charging times of external components. **0: HPH_MUX_OTP delay disabled** 1: HPH_MUX_OTP delay enabled
1	HPH_MODE	0	R/W	This register controls the operating mode of the headphone amplifier. The headphone amplifier supports single ended mode and differential mode. In differential output mode the right audio signal path is the active input signal for the headphone amplifier. **0: Stereo single ended mode** 1: Mono differential mode
0	I2C_MODE	0	R/W	This bit enables I^2C power down of the AS3412. **0: I^2C power down disabled** 1: I^2C power down enabled via PWR_HOLD bit.

Evaluation Register

Figure 86:
EVAL Register Description

Name	Address	Default Value
EVAL	0x3D	0x00
This register enables miscellaneous operating modes, that are typically controlled via slide switch or push button, for evaluation purposes or MCU controlled applications.		

Bit	Bit Name	Default	Access	Bit Description
4	MASTER_LIN_ MUTE	0	R/W	This register is the master register for the line input mute function. No matter in what operating mode the device is working the LINE_MUTE bit overrules any other setting in any operation mode. **0: Line Input master mute disabled** 1: Line Input master mute enabled
3	MON_MODE	0	R/W	This bit enables the monitor mode of AS3415/35 which can normally be enabled by pulling the MODE pin to VBAT/2. In case an MCU is connected to the device the Monitor mode can be enabled by setting this bit. **0: Monitor mode deactivated** 1: Monitor mode activated
2	PBO_MODE	0	R/W	This bit enables the playback mode of AS3412 which can normally be enabled by pulling the ANC pin to 0V. In case an MCU is connected to the device Monitor mode can be enabled by setting this bit. **0: Monitor mode deactivated** 1: Monitor mode activated
1	MICR_MUTE	0	R/W	This register is the master mute register for the left microphone amplifier. No matter in what operating mode the device is working the MICL_MUTE bit overrules any other setting in any operation mode. **0: Mute disabled** 1: Mute enabled
0	MICL_MUTE	0	R/W	This register is the master mute register for the left microphone amplifier. No matter in what operating mode the device is working the MICR_MUTE bit overrules any other setting in any operation mode. **0: Mute disabled** 1: Mute enabled

Figure 87:
CONFIG_1 Register Description

Name	Address	Default Value
CONFIG_1	0x3E	0x00
This bit controls the OTP programming clock source.		

Bit	Bit Name	Default	Access	Bit Description
3	EXTBURNCL	0	R/W	This register controls the clock source for OTP programming. Typically the internal clock is being used for OTP programming. **0: External burn clock disabled** 1: External burn clock enabled

Figure 88:
CONFIG_2 Register Description

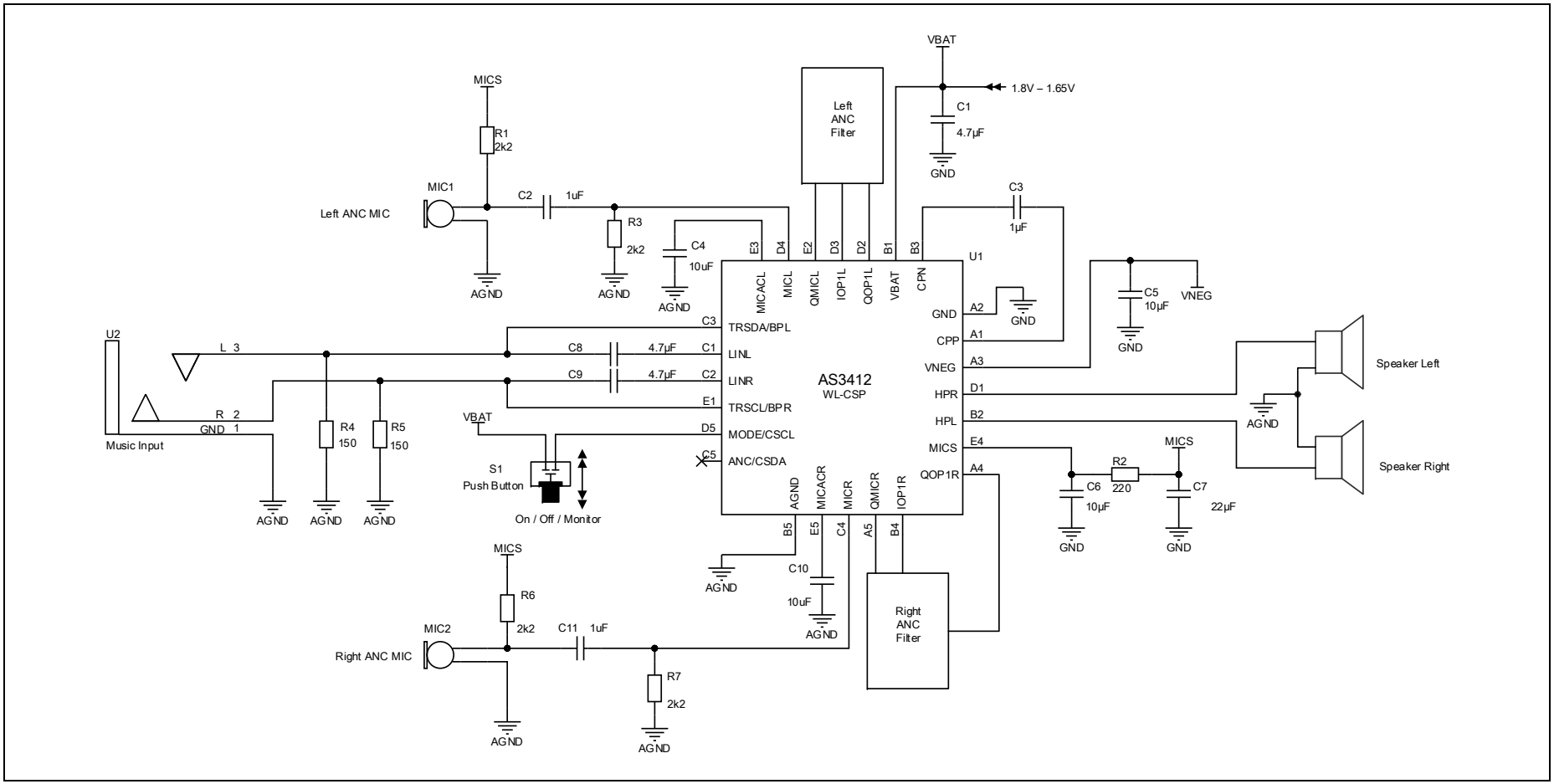
Name	Address	Default Value
CONFIG_2	0x3F	0x00
This register controls the register access to all OTP registers. In order to get access to these registers it is necessary to set EVAL_REG_ON bit to '1'.		

Bit	Bit Name	Default	Access	Bit Description
5	TM34	0	R/W	This Register defines the register bank selection for register 0x30-0x35 and 0x10-0x17. Depending on TM34 you can select either between Register bank 0x10-0x17 or 0x30h-0x34. **0: Test mode Registers 14h-17h and 10h-13h disabled test mode Registers 30h-33h and 34h-37h enabled** 1: Test mode Registers 14h-17h and 10h-13h enabled test mode Registers 30h-33h and 34h-37h disabled
4	BURNSW	0	R/W	This register controls the internal buffer switch from line input to V_{NEG} for V_{NEG} buffering during OTP programming. **0: BURN switch disabled** 1: BURN switch enabled
3	TM_REG34-35	0	R/W	**0: Register 34h-35h disabled Register 14h-17h disabled** 1: Register 34h-35h enabled Register 14h-17h enabled
2	TM_REG30-33	0	R/W	**0: Register 30h-33h disabled Register 10h-13h disabled** 1: Register 30h-33h enabled Register 10h-13h enabled
1:0	OTP_MODE<1:0>	00	R/W	This register controls the OTP access. **00: READ** 01: LOAD 10: WRITE 11: BURN

Application Information

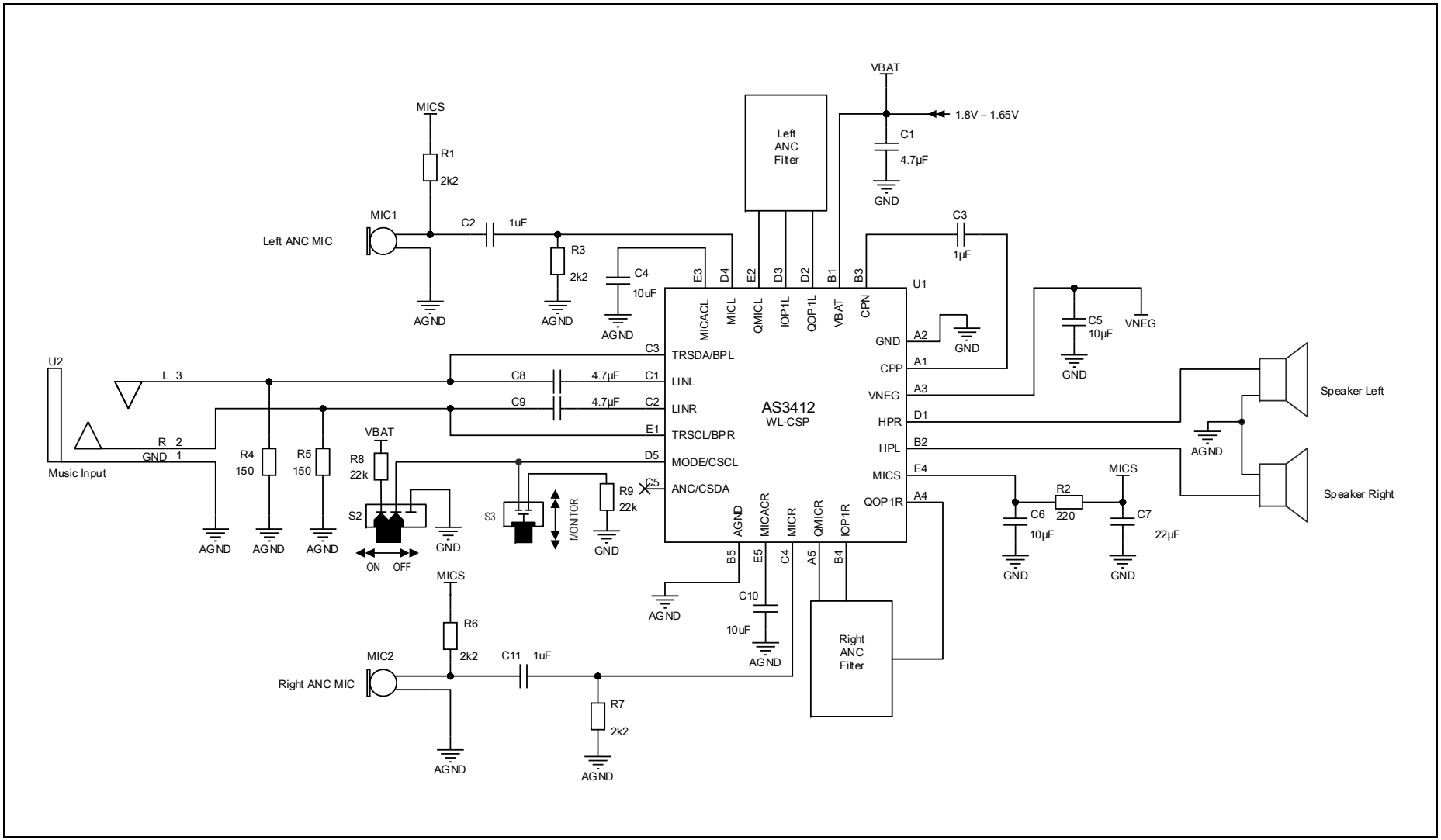
Schematic

Figure 89:
Push Button Operation Mode – Application Example



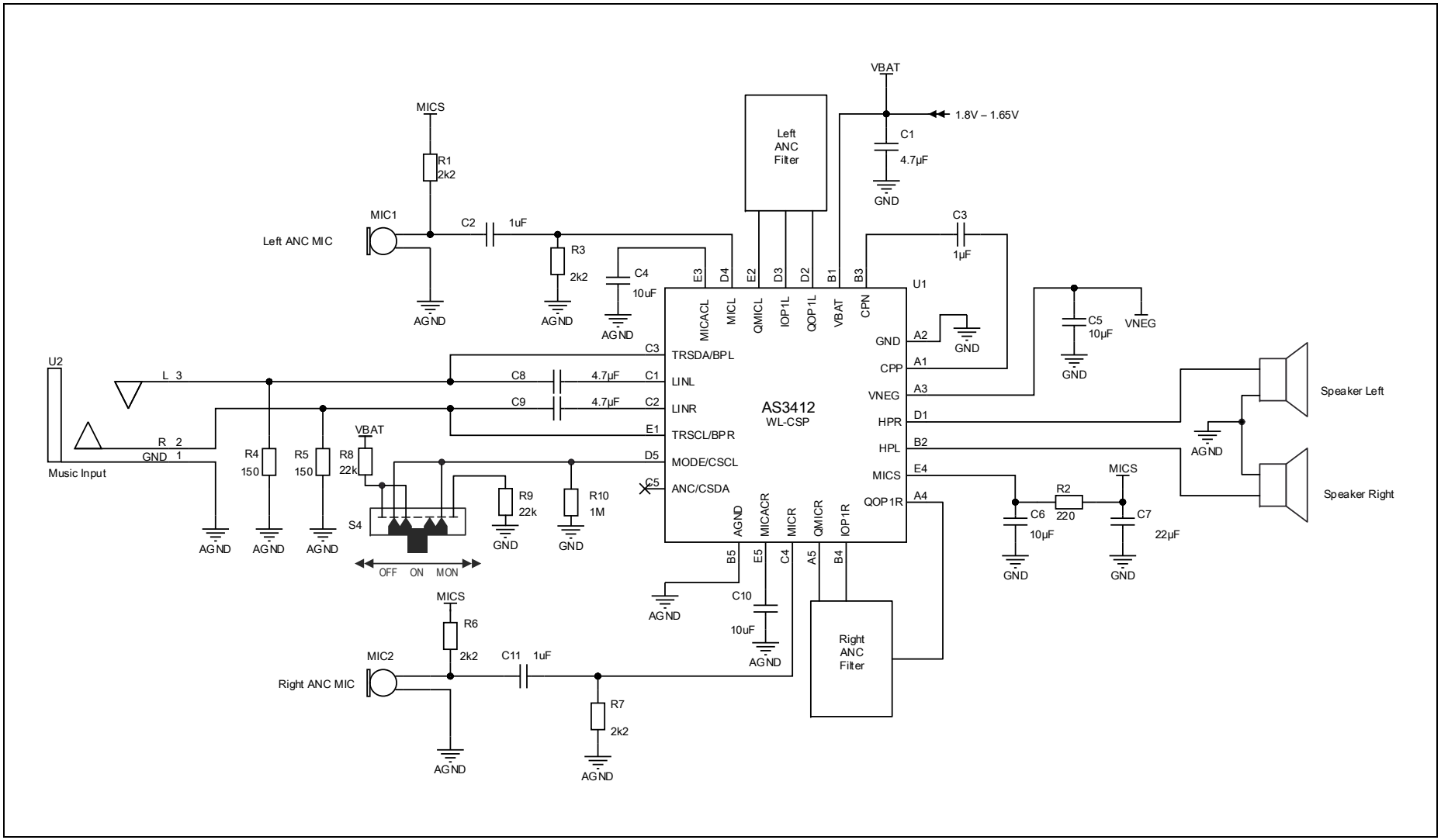
Push Button Operation Mode – Application Example: This application example shows the typical schematic in push button configuration for a Feed-Forward ANC headset. A single push button can control the headset. For details on Push Button control please refer to chapter Operation Modes.

Figure 90:
Slider Operation Mode – Application Example



Slider Operation Mode – Application Example: This application example shows the typical schematic in Slider configuration for a Feed-Forward ANC headset. A 3 pole slider is being used to switch the AS3412 on and off. A push button is used to enter Monitor mode.

Figure 91:
Full Slider Operation Mode – Application Example



Full Slider Operation Mode – Application Example: This application example shows the typical schematic in Full Slider configuration for a Feed-Forward ANC headset. A multi pole slide switch is being used to switch the AS3412 on, off and enter Monitor mode.

External Components

This chapter provides detailed information concerning recommended external components such as capacitors and resistors.

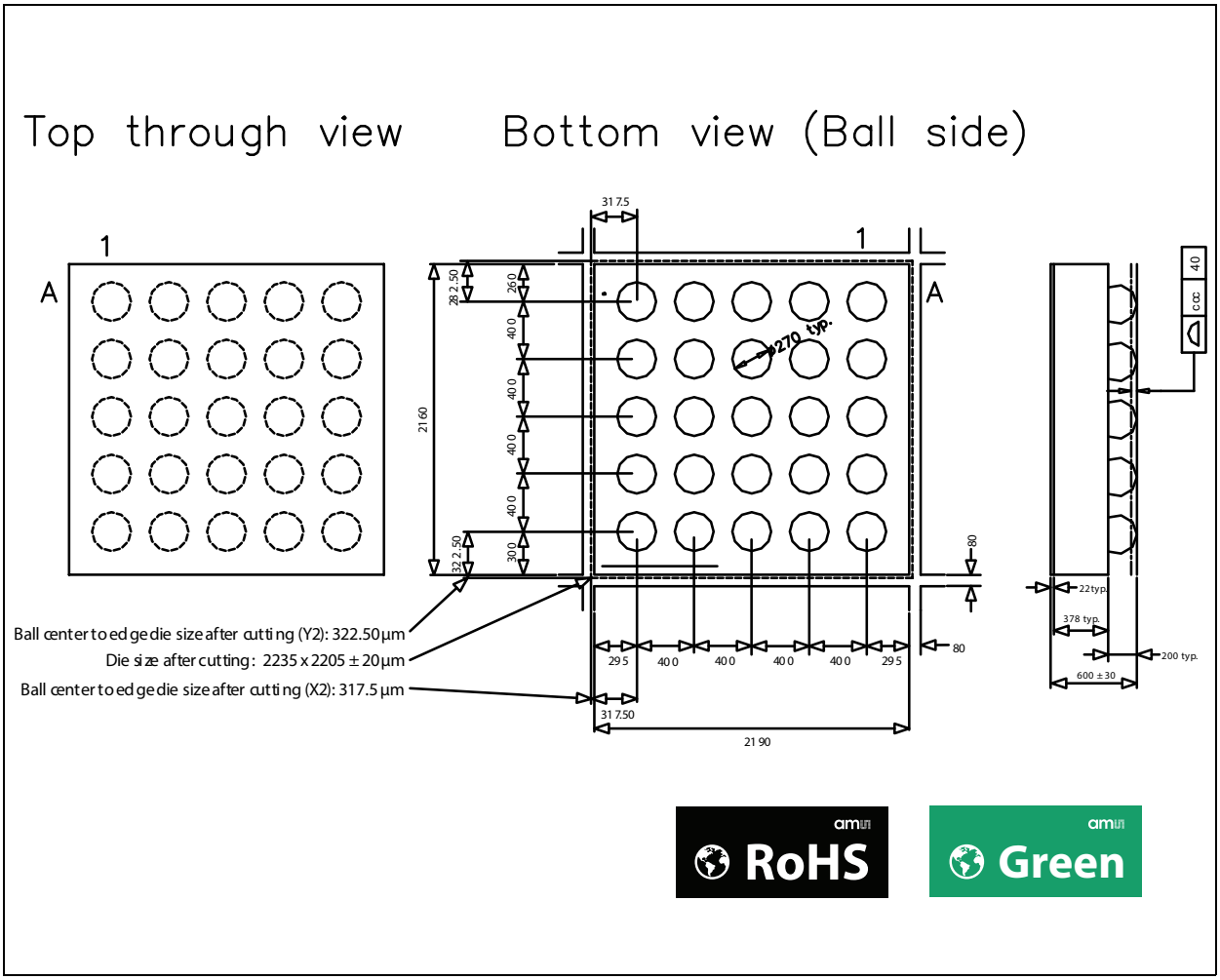
Figure 92:
External Components

Symbol	Parameter	Temp. Characteristic	Min. Rated Voltage	Max. Tolerance	Min. Nom. Capacitance
Capacitors					
C1, C_{VBAT}	Input Capacitor	Y5R; X5R	4V	±20%	4.7µF
C3, C_{FLY}	VNEG charge pump flying capacitor	Y5R; X5R	4V	±20%	1µF
C4, C10, C_{ACR}, C_{ACR}	AC coupling capacitor	Y5R; X5R	4V	±10%	10µF
C5, C_{VNEG}	Output Capacitor	Y5R; X5R	4V	±20%	10µF
C8, C9	AC coupling input capacitor	Y5R; X5R	4V	±20%	4.7µF
C6, C_{MICS}	Output Capacitor	Y5R; X5R	4V	±20%	10µF
C7	Output Capacitor (optional component)	Y5R; X5R	4V	±20%	22µF
C2, C11, C_{MICL}, C_{MICR}	AC coupling capacitor; value depends on ANC filter design	Y5R; X5R	4V	±10%	-
C_{FILTER}	ANC filter related capacitors	Y5R; X5R	4V	±10%	-
Resistors					
R1, R6	Bias current resistor for microphones	-	-	5%	2.2kΩ
R4, R5	Pull down resistors to avoid humming noise	-	-	5%	150Ω
R3, R7	Microphone input high pass filter; value depends on ANC filter design	-	-	5%	-
R2	Microphone supply filter resistor (optional component)	-	-	10%	220Ω
R_{FILTER}	ANC filter related resistors	-	-	1%	-

External Components: This table provides detailed information concerning the recommended external components to operate AS3412.

Package Drawings & Markings

Figure 93:
Package Drawings WL-CSP



Package Drawing: This figure shows the package drawing of the AS3412.

Note(s):

1. Pin 1 = A1
2. ccc Coplanarity
3. All dimensions are in µm

Figure 94:
Package Marking

Package Marking: This figure shows the package marking of the AS3412.

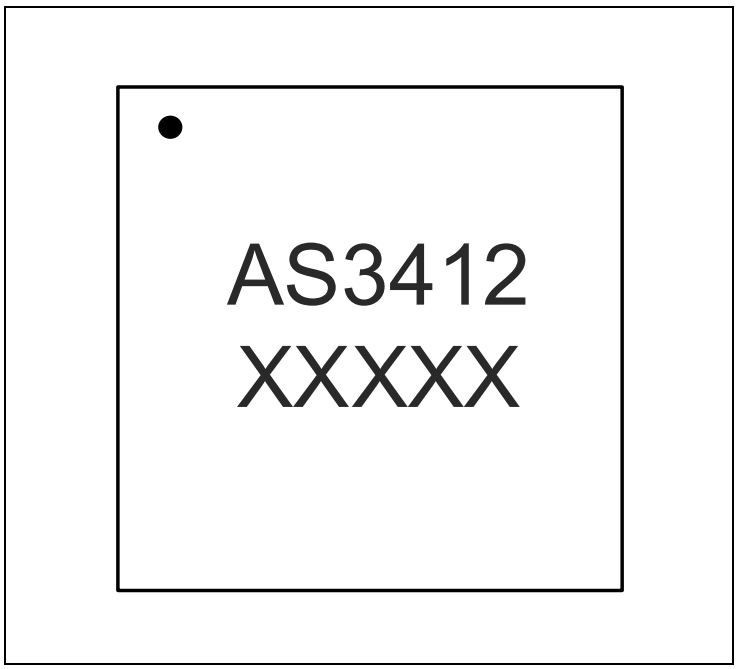


Figure 95:
Package Code

XXXXX
Tracecode

Package Code: This table shows the package code of the AS3412 WL-CSP package.

Ordering & Contact Information

Figure 96:
Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS3412-EWLT	WL-CSP	AS3412	Tape & Reel	10000 pcs/reel

Ordering Information: Shows the ordering information of the AS3412.

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 0-91 (2016-Mar-22) to current revision 1-00 (2016-Apr-06)	Page
Initial production version for release	
Updated Figure 7	8
Updated Figure 14	14
Updated Figure 19	18
Updated Figure 23	21
Updated Figure 35	29
Updated Figure 68	51

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide