8-bit I²C-bus and SMBus I/O port with interrupt

Features

- Operation power supply voltage from 2.3V to 5.5 V
- 8-bit I²C-bus GPIO with interrupt and reset
- 5V tolerant I/Os
- Polarity inversion register
- Active LOW interrupt output
- Low current consumption
- 0Hz to 400KHz clock frequency
- Noise filter on SCL/SDA inputs
- Power-on reset
- ESD protection (4KV HBM and 1KV CDM)
- Offered in four different packages: SOIC-16, TSSOP-16 and TQFN 3x3-16, TQFN 4x4-16

Description

The PI4IOE5V9554 and PI4IOE5V9554A provide 8 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C-bus/SMBus applications. It includes the features such as higher driving capability, 5V tolerance, lower power supply, individual I/O configuration, and smaller packaging. It provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PI4IOE5V9554/PI4IOE5V9554A consist of an 8-bit register to configure the I/Os as either inputs or outputs, and an 8-bit polarity register to change the polarity of the input port register data. The data for each input or output is kept in the corresponding Input port or Output port register. All registers can be read by the system master.

The PI4IOE5V9554/PI4IOE5V9554A open-drain interrupt output is activated and indicate to the system when any input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I²C-bus address and allow up to eight devices to share the same I²C-bus/SMBus. The PI4IOE5V9554A is identical to the PI4IOE5V9554 except that the fixed I²C-bus address is different allowing up to sixteen of these devices (eight of each) on the same I²C-bus/SMBus.

Pin Configuration

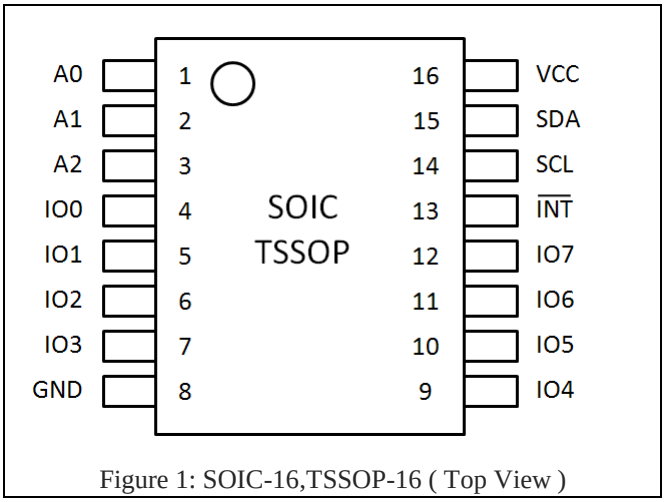

Figure 1: SOIC-16,TSSOP-16 (Top View)

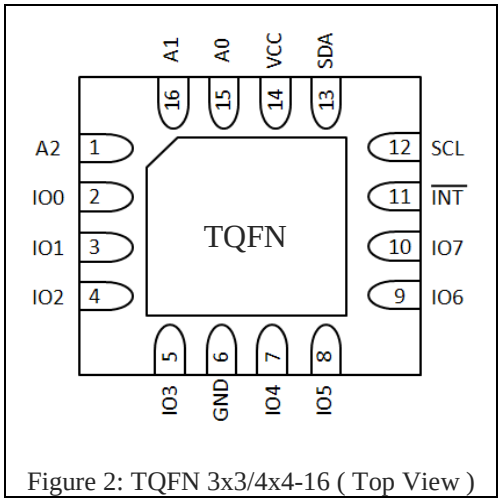

Figure 2: TQFN 3x3/4x4-16 (Top View)

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Pin Description

Table 1: Pin Description

Pin		Name	Type	Description
SOIC16 TSSOP16	TQFN16			
1	15	A0	I	Address input 0
2	16	A1	I	Address input 1
3	1	A2	I	Address input 2
4	2	IO0	I/O	input/output 0
5	3	IO1	I/O	input/output 1
6	4	IO2	I/O	input/output 2
7	5	IO3	I/O	input/output 3
8	6	GND	G	Supply ground
9	7	IO4	I/O	input/output 4
10	8	IO5	I/O	input/output 5
11	9	IO6	I/O	input/output 6
12	10	IO7	I/O	input/output 7
13	11	$\overline{INT}$	O	Interrupt output (open drain)
14	12	SCL	I	Serial clock line
15	13	SDA	I	Serial data line
16	14	VCC	P	Supply voltage

* I = Input; O = Output; P = Power; G = Ground

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Maximum Ratings

Power supply	-0.5V to +6.0V
Voltage on an I/O pin	GND-0.5V to +6.0V
Input current	±20mA
Output current on an I/O pin	±50mA
Supply current	±160mA
Ground supply current	200mA
Total power dissipation	400mW
Operation temperature	-40~85℃
Storage temperature	-65~150℃
Maximum Junction temperature ,T j(max)	125℃

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Static characteristics

VCC = 2.3 V to 5.5 V; GND = 0 V; Tamb= -40 ℃ to +85 ℃; unless otherwise specified.

Table 2: Static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
V_{CC}	Supply voltage		2.3	-	5.5	V
I_{CC}	Supply current	Operating mode; VCC = 5.5 V; no load; f_{SCL}= 400 kHz	-	40	60	μA
		Operating mode; VCC = 2.3 V; no load; f_{SCL}= 400 kHz		10	20	uA
I_{stb}	Standby current	Standby mode; VCC = 5.5 V; no load; V_I = GND; f_{SCL}= 0 kHz; I/O = inputs	-	500	700	uA
		Standby mode; VCC = 5.5 V; no load; V_I = VCC; f_{SCL}= 0 kHz; I/O = inputs	-	0.25	1	μA
V_{POR}	Power-on reset voltage[1]		-	1.16	1.41	V
Input SCL, input/output SDA						
V_{IL}	Low level input voltage		-0.5	-	+0.3VCC	V
V_{IH}	High level input voltage		0.7VCC	-	5.5	V
I_{OL}	Low level output current	V_{OL}=0.4V; VCC=2.3V	3	6	-	mA
I_L	Leakage current	V_I=VCC or GND	-1	-	1	μA
C_i	Input capacitance	V_I =GND	-	6	10	pF

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I/Os						
V_{IL}	Low level input voltage		-0.5	-	+0.81	V
V_{IH}	High level input voltage		+1.8	-	5.5	V
I_{OL}	Low level output current	VCC =2.3V; V_{OL} = 0.5V[2]	8	10	-	mA
		VCC =2.3V; V_{OL} = 0.7V[2]	10	13	-	mA
		VCC =3.0V; V_{OL} = 0.5V[2]	8	14		mA
		VCC =3.0V; V_{OL} =0.7V[2]	10	19		mA
		VCC =4.5V; V_{OL} =0.5V[2]	8	17		mA
		VCC =4.5V; V_{OL} =0.7V2]	10	24		mA
V_{OH}	High level output current	I_{OH}=-8mA; VCC=2.3V[3]	1.8	-	-	V
		I_{OH}=-10mA; VCC=2.3V[3]	1.7	-	-	V
		I_{OH}=-8mA; VCC=3.0V[3]	2.6	-	-	V
		I_{OH}=-10mA; VCC=3.0V[3]	2.5	-	-	V
		I_{OH}=-8mA; VCC=4.5V[3]	4.1	-	-	V
		I_{OH}=-10mA; VCC=4.5V[3]	4.0	-	-	V
I_{LI}	Low level input leakage current	VCC=3.6V; V_I=VCC	-1	-	1	uA
I_L	Leakage current	VCC=5.5V; V_I=GND			-100	uA
C_i	Input capacitance		-	3.7	10	pF
C_o	Output capacitance		-	3.7	10	pF
Interrupt $\overline{INT}$						
I_{OL}	Low level output current	V_{OL}=0.4V	3	-	-	mA
Select inputs A0,A1,A2						
V_{IL}	Low level input voltage		-0.5	-	+0.81	V
V_{IH}	High level input voltage		+1.8	-	5.5	V
I_L	Input leakage current		-1	-	1	μA

Note:
[1]: VCC must be lowered to 0.2 V for at least 20us in order to reset part.
[2]: Each I/O must be limited to a maximum current of 25mA and the device must be limited to a maximum current of 100mA.
[3]: The total current sourced by all I/Os must be limited to 85mA.

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Dynamic Characteristics

Table 3: Dynamic characteristics

Symbol	Parameter	Test Conditions	Standard mode I^2C		Fast mode I^2C		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{VD;ACK}$[1]	data valid acknowledge time		-	3.45	-	0.9	µs
$t_{HD;DAT}$[2]	data hold time		0	-	0	-	ns
$t_{VD;DAT}$	data valid time		-	3.45	-	0.9	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals		-	300	-	300	ns
t_r	rise time of both SDA and SCL signals		-	1000	-	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
Port timing							
$t_{v(Q)}$	Data output valid time[3]		-	200	-	200	ns
$t_{su(D)}$	Data input set-up time		100	-	100	-	ns
$t_{h(D)}$	Data input hold time		1	-	1	-	us
Interrupt timing							
$t_{v(INT)}$	Valid time on pin $\overline{INT}$		-	4	-	4	us
$t_{rec(INT)}$	Reset time on pin $\overline{INT}$		-	4	-	4	us

Note:
[1]: $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
[2]: $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
[3]: $t_{v(Q)}$measured from 0.7VCC on SCL to 50% I/O output.

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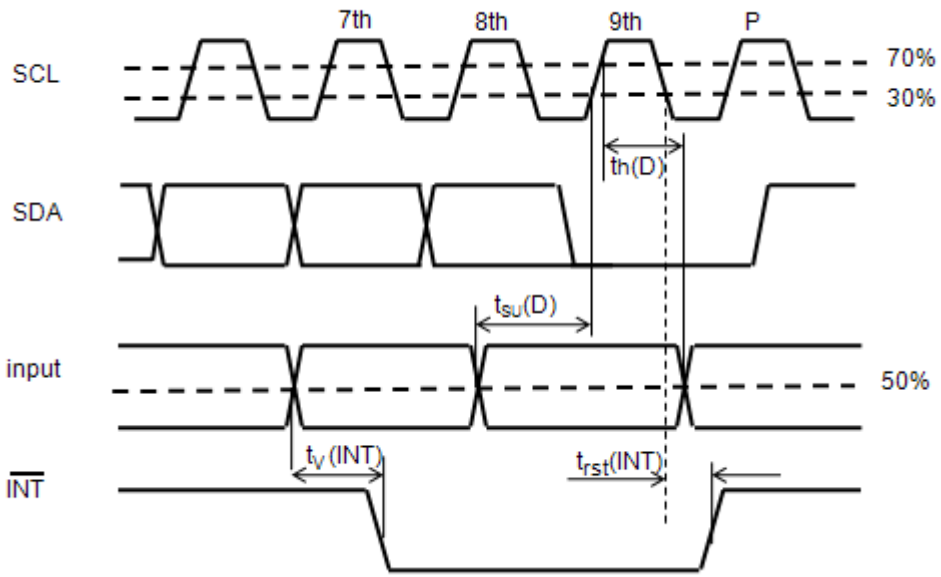
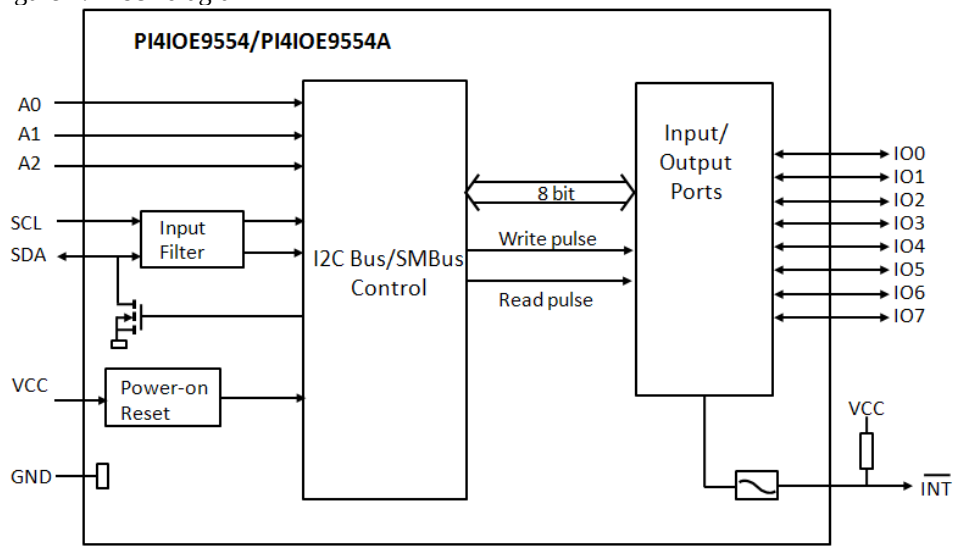


Figure 3: timing parameters for INT signal

PI4IOE5V9554/PI4IOE5V9554A Block Diagram

Figure 4: Block diagram



All I/Os are set to inputs at reset.

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Details Description

a. Device address

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PI4IOE5V9554/54A is shown below. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

Table 4: Device address Byte

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
PI4IOE5V9554	0	1	0	0	A2	A1	A0	R/W
PI4IOE5V9554A	0	1	1	1	A2	A1	A0	R/W

Note: Read "1", Write "0"

b. Register description

i. Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 5: Command byte

Command	Protocol	Function
0	Read byte	Input port register
1	Read/write byte	Output port register
2	Read/write byte	Polarity Inversion register
3	Read/write byte	Configuration register

ii. Register 0: Input port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default 'X' is determined by the externally applied logic level, normally '1' when no external signal externally applied because of the internal pull-up resistors.

Table 6: Input port register

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0

iii. Register 1: Output port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3.Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 7: Output port register

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	1	1	1	1	1	1	1	1

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iv. Register 2: Polarity inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

Table 8: Polarity inversion register

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	0	0	0	0	0	0	0	0

v. Register 3: Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, theI/Os are configured as inputs with a weak pull-up to VCC.

Table 9: Configuration register

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

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c. Power-on reset

When power is applied to VCC, an internal Power-On Reset (POR) holds thePI4IOE5V9554/PI4IOE5V9554A in a reset condition until VCC has reached VPOR. At that point, the reset condition is released and thePI4IOE5V9554/PI4IOE5V9554A registers and state machine will initialize to their default states. Thereafter, VCC must be lowered below 0.2 V to reset the device.
For a power reset cycle, VCC must be lowered below 0.2 V and then restored to the operating voltage.

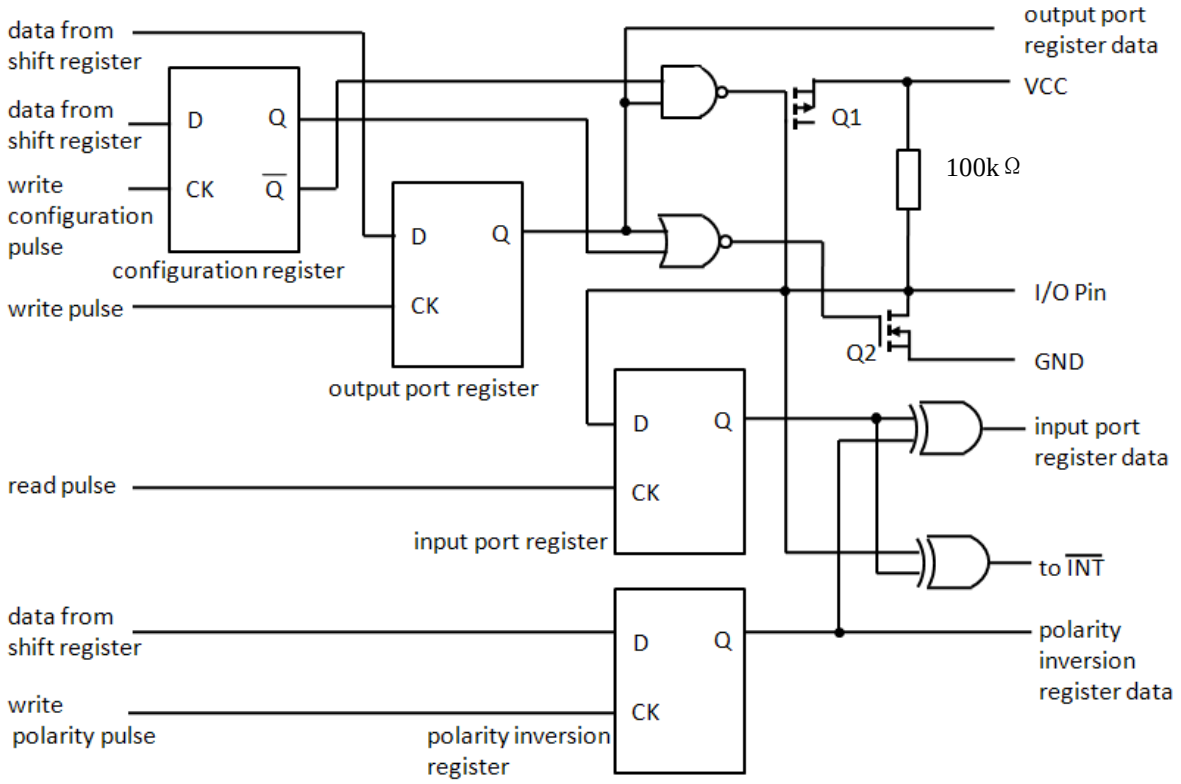
d. Interrupt output

The open-drain interrupt output is activated when one of the port pins change state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the Input Port register is read.
Note that changing an I/O from and output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

e. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up (100 kΩ typ.) to VCC. The input voltage may be raised above VCC to a maximum of 5.5V.
If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either VCC or GND.

Figure 5: Simplified schematic of IO0 to IO7



Note: At power –on reset, all registers return to default values.

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f. Bus Transaction

Data is transmitted to the PI4IOE5V9554/PI4IOE5V9554A registers using the Write mode as shown in Figure 6 and Figure 7. These devices do not implement an auto-increment function, so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

Figure 6: write to output register

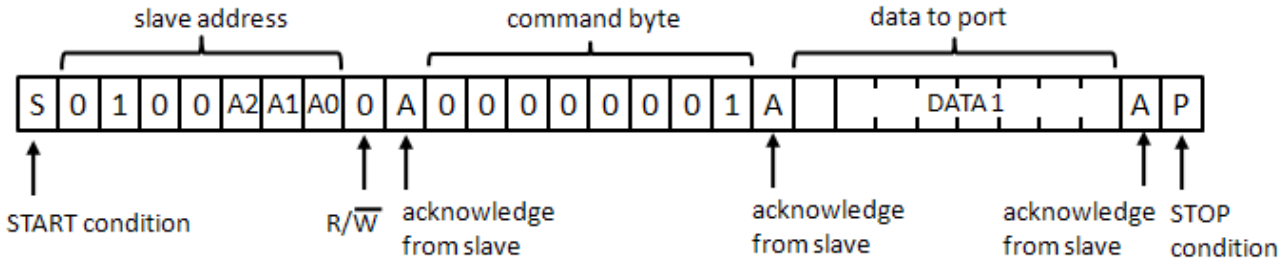
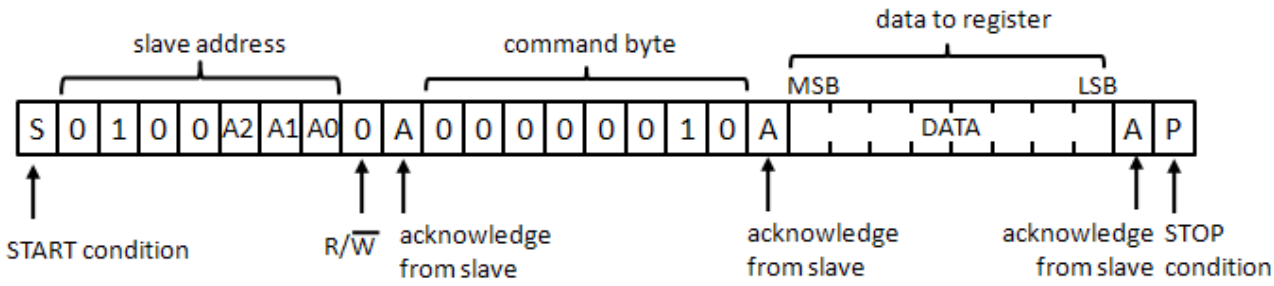


Figure 7: Write to configuration register or polarity inversion register



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Data is read from the PI4IOE5V9554/PI4IOE5V9554A registers using the Read mode as shown in Figure 8 and Figure 9.

Figure 8: Read from register

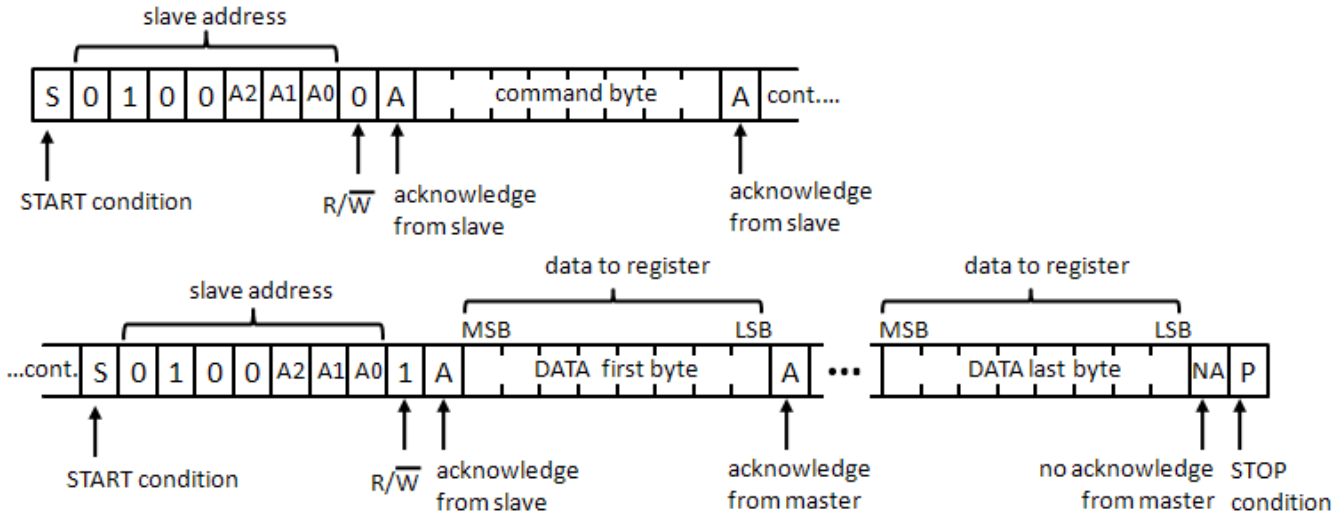
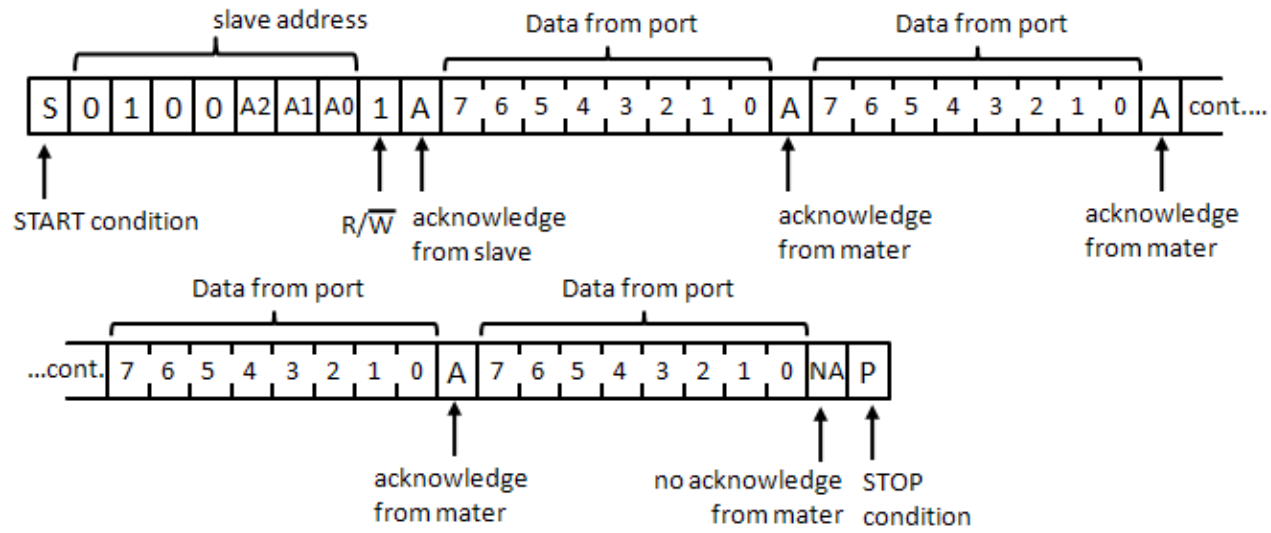


Figure 9: Read input port register



This figure assumes the command byte has previously been programmed with 00h.
Transfer of data can be stopped at any moment by a STOP condition.

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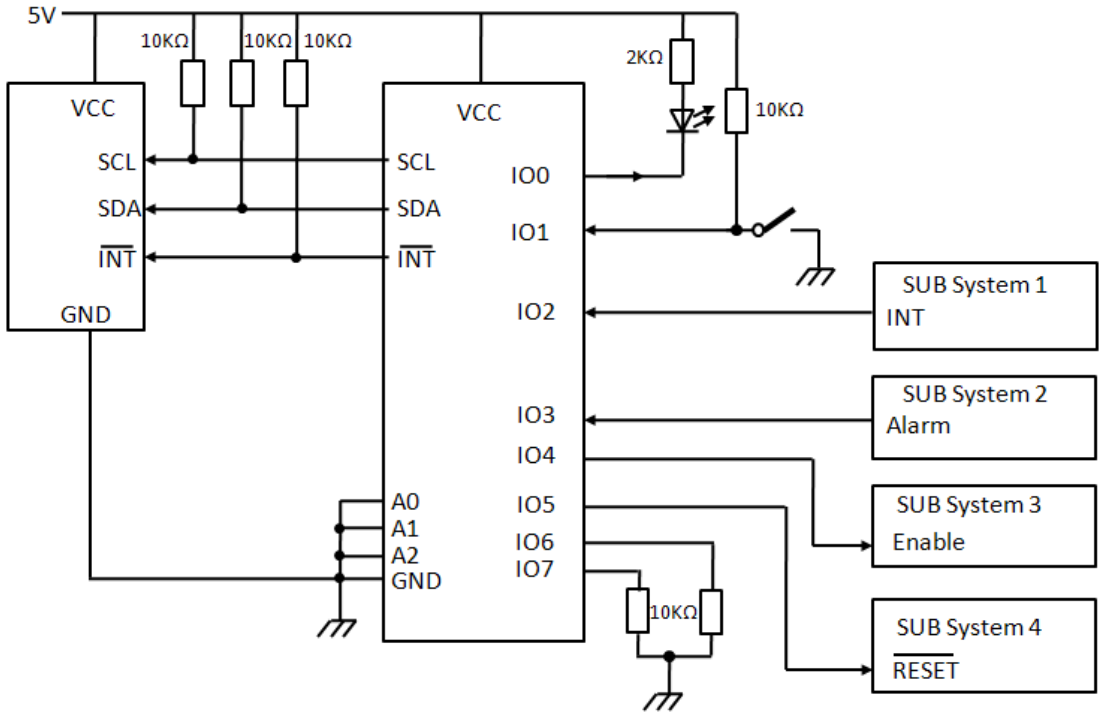
Application Design-In Information

Figure 10: Typical application



Device address configured as 0100100x for this example.
IO0, IO4, IO5 configured as outputs.
IO1, IO2, IO3 configured as inputs.
IO6, IO07 are not used and must be configured as outputs.

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Part Marking

PI4IOE5V9554

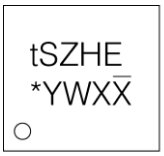
L Package

Z: Die Rev
Y: Year
W: Workweek
1st X: Assembly Site Code
2nd X: Fab Site Code

W Package

Z: Die Rev
Y: Year
W: Workweek
K: Assembly Site Code
G: Wafer Fab Site Code

ZH Package



*: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code

ZY Package

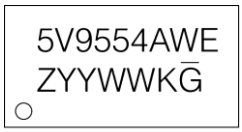
Z: Die Rev
Y: Year
W: Workweek
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code

PI4IOE5V9554A

L Package

Z: Die Rev
Y: Year
W: Workweek
1st X: Assembly Site Code
2nd X: Fab Site Code

W Package



Z: Die Rev
YY: Year
WW: Workweek
K: Assembly Site Code
G: Wafer Fab Site Code

ZH Package

Z: Die Rev
Y: Year
W: Workweek
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code

ZY Package

Z: Die Rev
Y: Year
W: Workweek
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code

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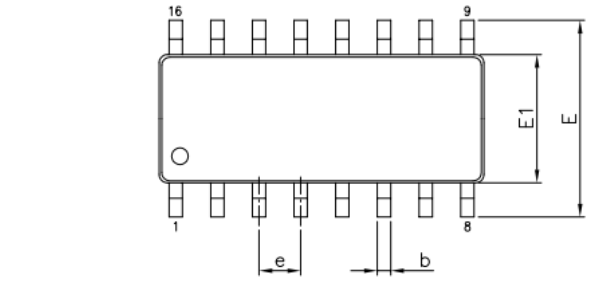
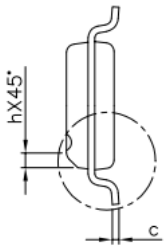
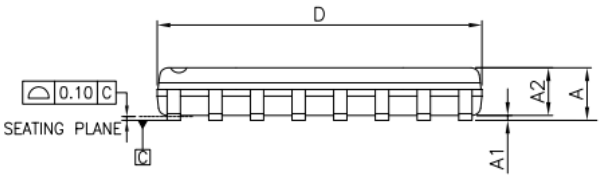
Packaging Mechanical

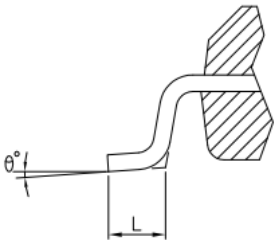
SOIC-16(W)





SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.00	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	9.80	9.90	10.0
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
L	0.40	–	1.27
h	0.15	–	0.50
θ°	0	–	8





NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC OUTLINE : MS-012 AC
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE MIN. DIMENSION OF A2 AND h ARE OUT OF JEDEC SPEC.

DATE: 06/30/16

DESCRIPTION: 16-Pin, 150mil Wide SOIC

PACKAGE CODE: W

DOCUMENT CONTROL #: PD-1004 REVISION: G

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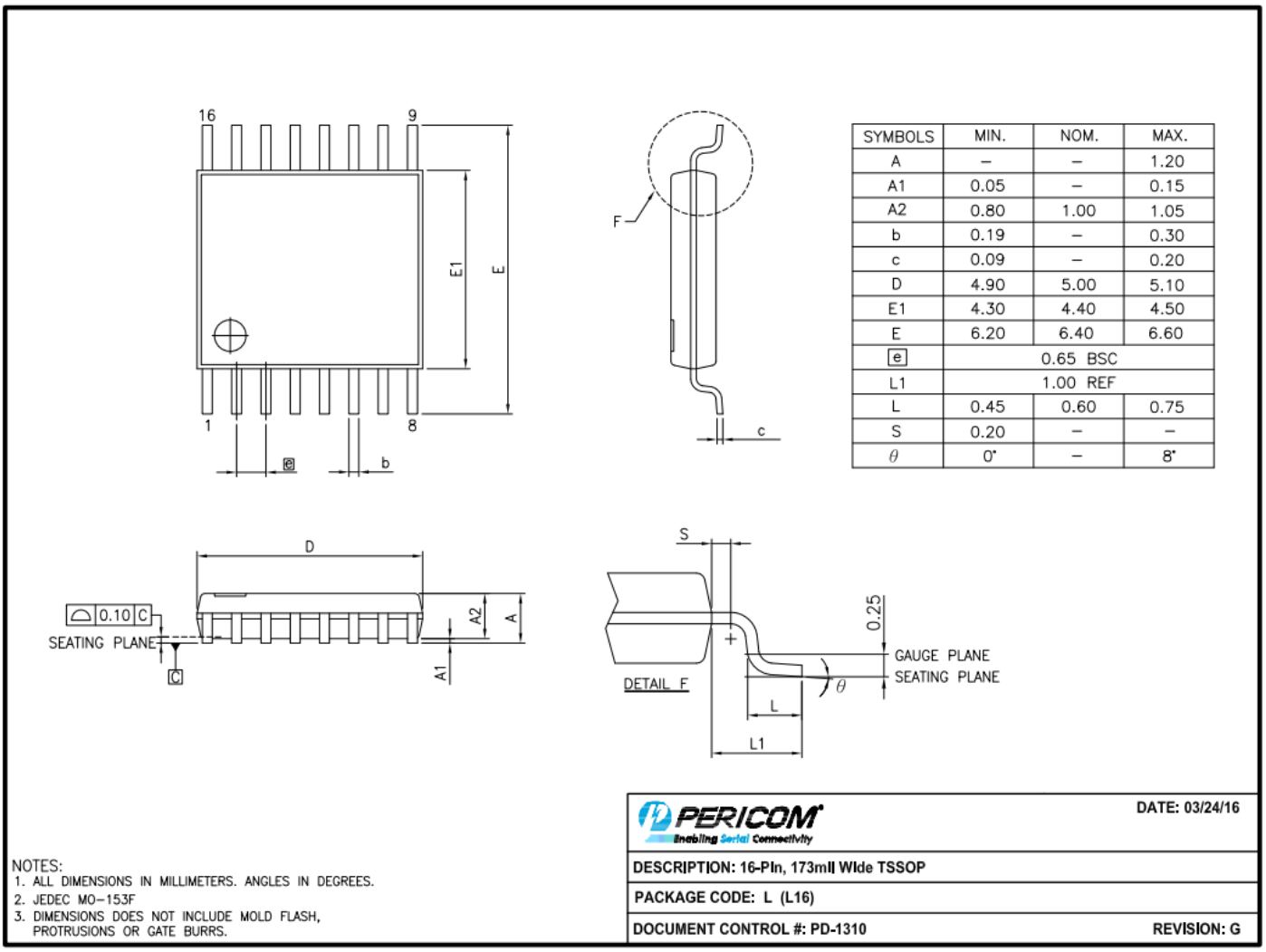
TSSOP-16(L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO–153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity — DATE: 03/24/16

DESCRIPTION: 16-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L16)

DOCUMENT CONTROL #: PD-1310 — REVISION: G

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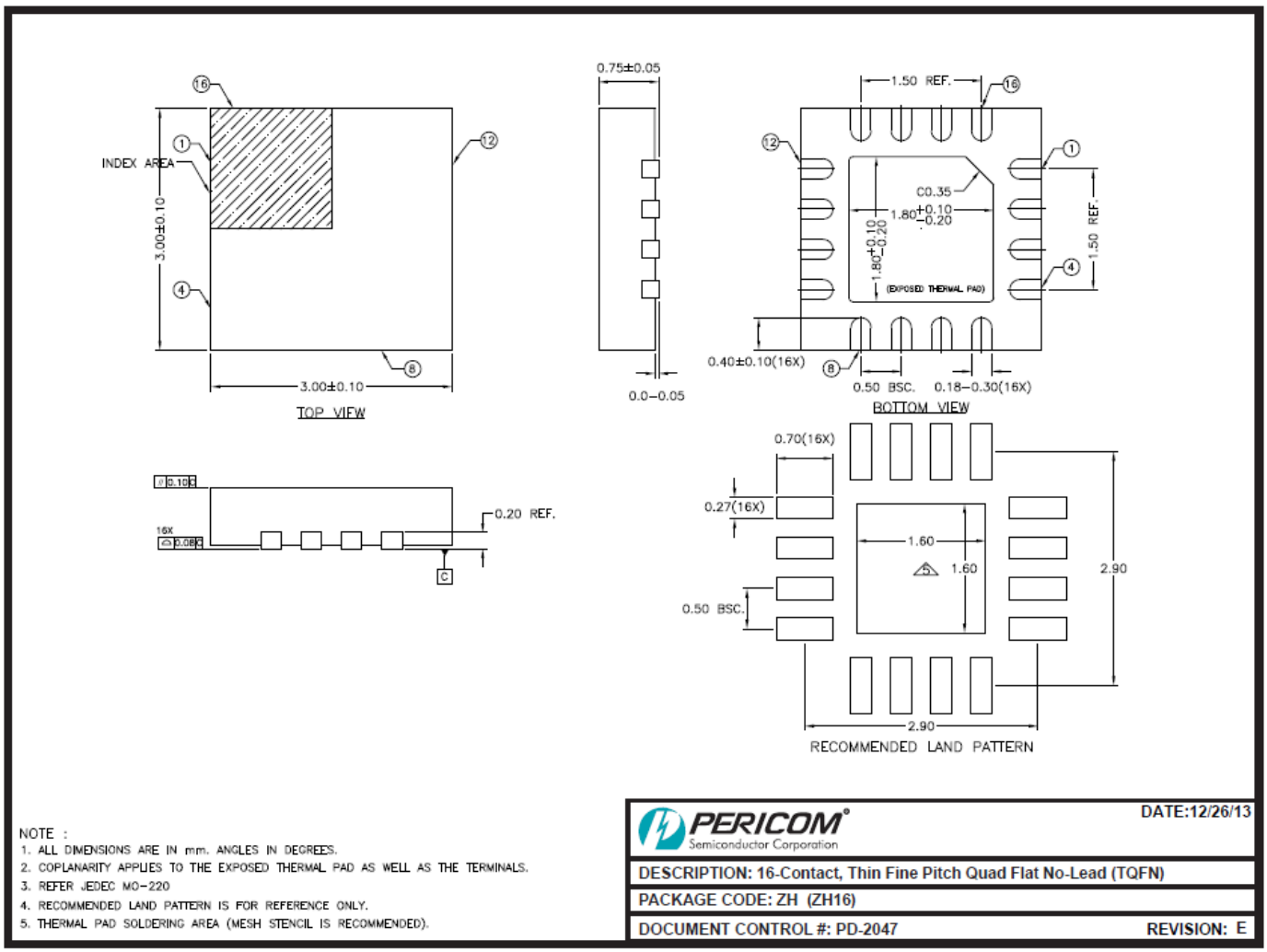
TQFN 3x3-16(ZH)



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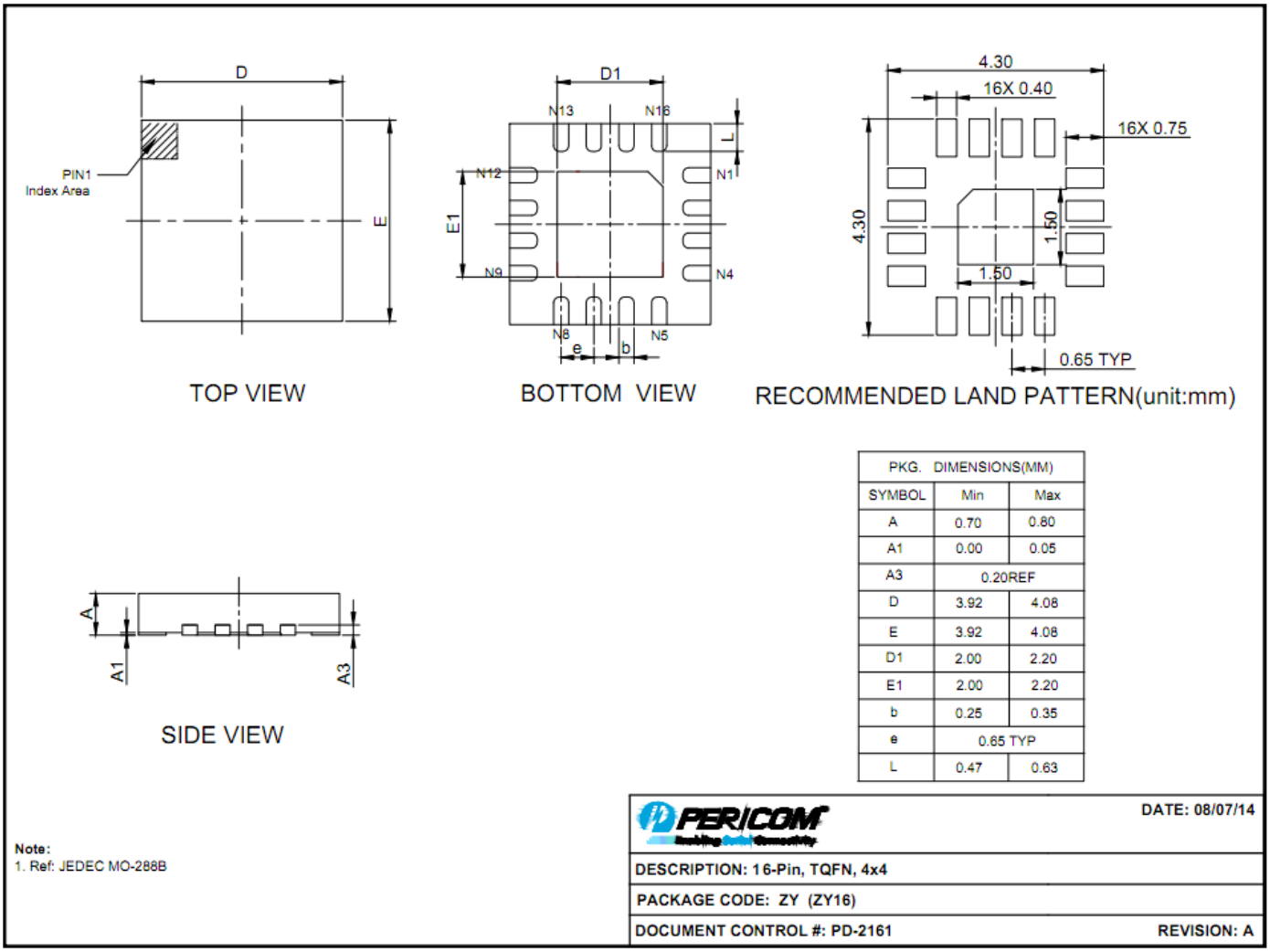
TQFN 4x4-16(ZY)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20REF	
D	3.92	4.08
E	3.92	4.08
D1	2.00	2.20
E1	2.00	2.20
b	0.25	0.35
e	0.65 TYP	
L	0.47	0.63

Note:
1. Ref: JEDEC MO-288B

PERICOM Semiconductor Corporation — DATE: 08/07/14

DESCRIPTION: 16-Pin, TQFN, 4x4

PACKAGE CODE: ZY (ZY16)

DOCUMENT CONTROL #: PD-2161 — REVISION: A

For latest package info.
please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Numbers	Package Code	Package
PI4IOE5V9554WEX, PI4IOE5V9554AWEX	W	16-Pin,150 mil Wide SOIC
PI4IOE5V9554LEX, PI4IOE5V9554ALEX	L	16-pin TSSOP16(173mil wide)
PI4IOE5V9554ZHEX, PI4IOE5V9554AZHEX	ZH	16-pin TQFN3.0x3.0
PI4IOE5V9554ZYEX, PI4IOE5V9554AZYEX	ZY	16-pin TQFN4.0x4.0

Notes:

- EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
- See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

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