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FDPF680N10T

N-Channel PowerTrench® MOSFET

100 V, 12 A, 68 mΩ



Features

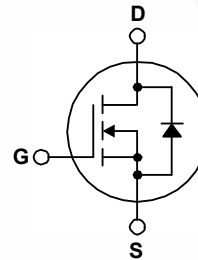
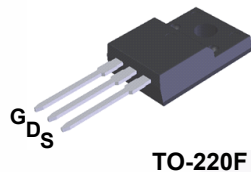
- $R_{DS(on)} = 54 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 6 \text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Consumer Appliances
- LCD/LED/PDP TV
- Synchronous Rectification
- Uninterruptible Power Supply
- Micro Solar Inverter



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDPF680N10T	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	12
		- Continuous ($T_C = 100^\circ\text{C}$)	7.6
I_{DM}	Drain Current	- Pulsed (Note 1)	48
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	50.4
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	13.0
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	24
		- Derate Above 25°C	0.19
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDPF680N10T	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	5.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDPF680N10T	FDPF680N10T	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$, $T_C = 25^\circ\text{C}$	100	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.1	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_C = 150^\circ\text{C}$	-	-	500	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 6 \text{ A}$	-	54	68	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}$, $I_D = 12 \text{ A}$	-	26	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	750	1000	pF
C_{oss}	Output Capacitance		-	60	80	pF
C_{rss}	Reverse Transfer Capacitance		-	25	40	pF
$Q_{g(tot)}$	Total Gate Charge	$V_{DS} = 80 \text{ V}$, $I_D = 12 \text{ A}$, $V_{GS} = 10 \text{ V}$	-	13	17	nC
Q_{gs}	Gate to Source Gate Charge		-	4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	4	-

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}$, $I_D = 12 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_G = 10 \Omega$	-	13	36	ns
t_r	Turn-On Rise Time		-	19	48	ns
$t_{d(off)}$	Turn-Off Delay Time		-	18	46	ns
t_f	Turn-Off Fall Time		(Note 4)	-	6	22

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	12	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	48	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 12 \text{ A}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$, $I_{SD} = 12 \text{ A}$, $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	29	-	ns
Q_{rr}	Reverse Recovery Charge		-	35	-	nC

Notes:

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. $L = 0.7 \text{ mH}$, $I_{AS} = 12 \text{ A}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 12 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

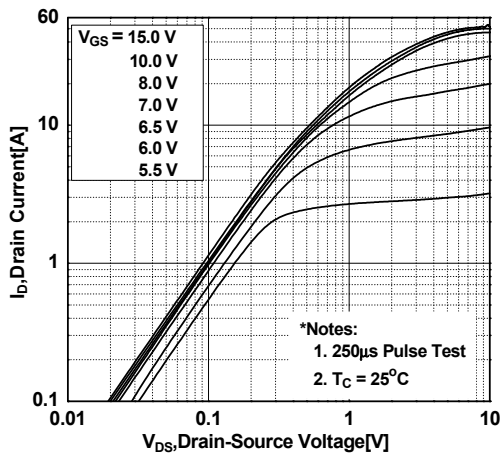


Figure 2. Transfer Characteristics

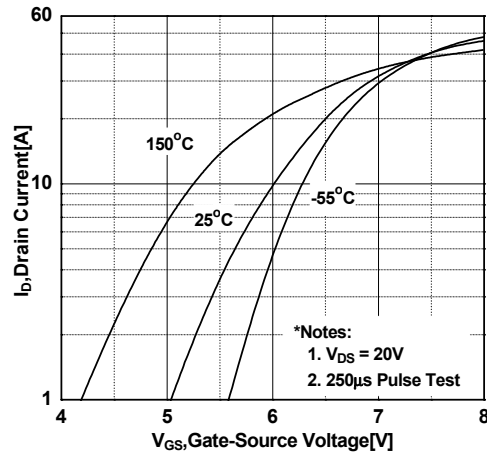


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

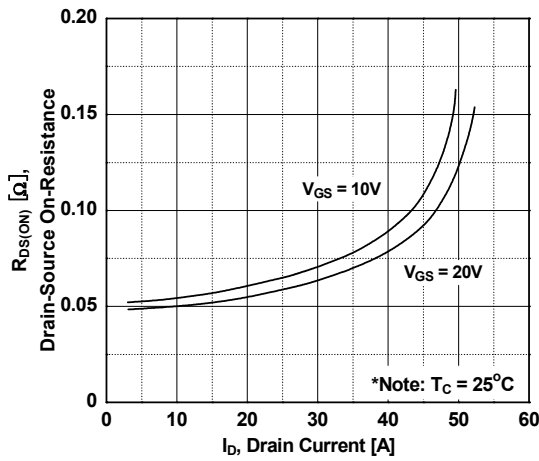


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

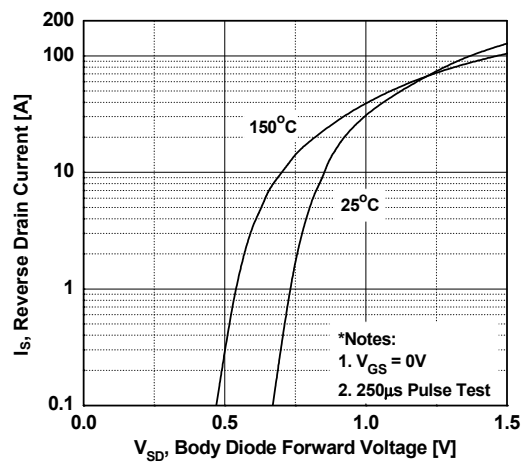


Figure 5. Capacitance Characteristics

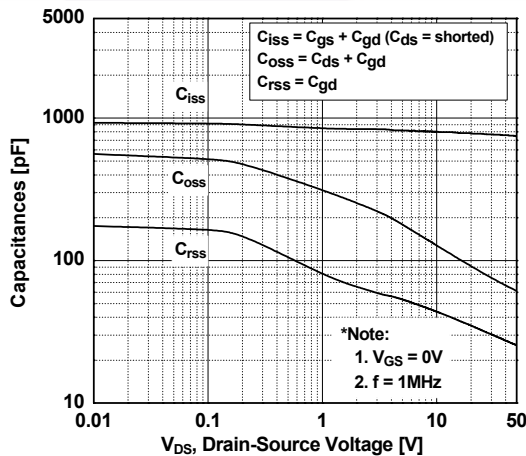
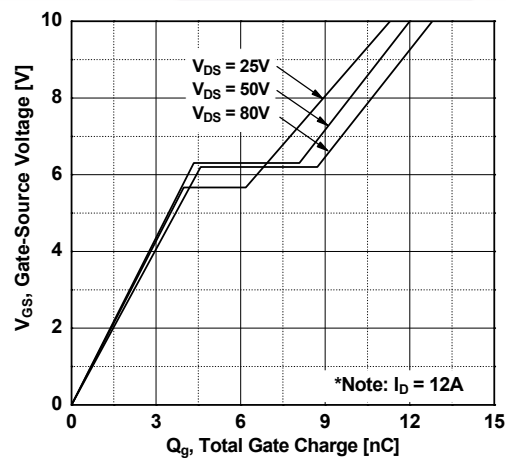


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

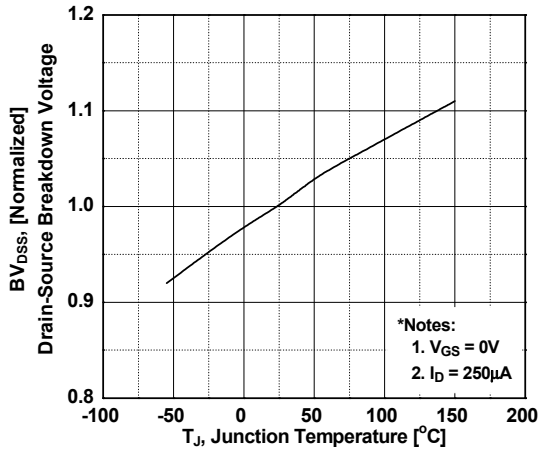


Figure 8. On-Resistance Variation vs. Temperature

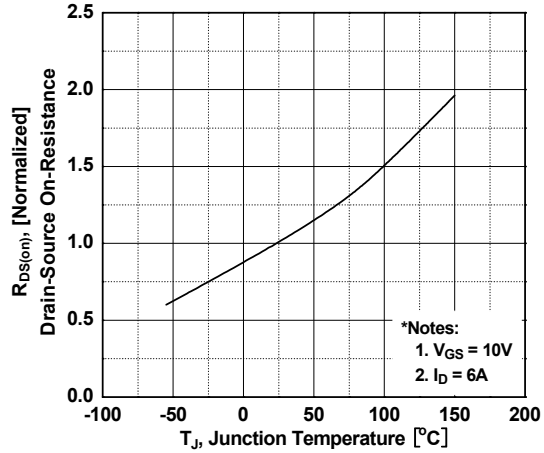


Figure 9. Maximum Safe Operating Area

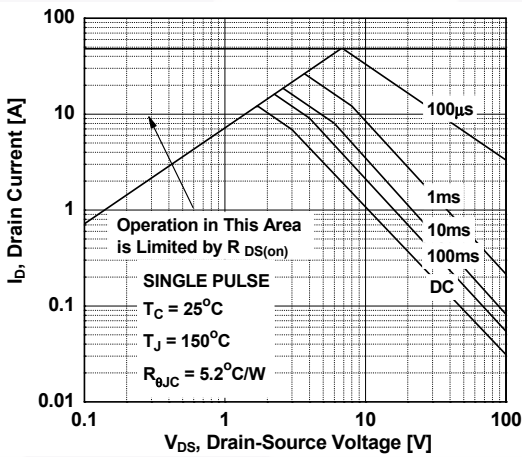


Figure 10. Maximum Drain Current vs. Case Temperature

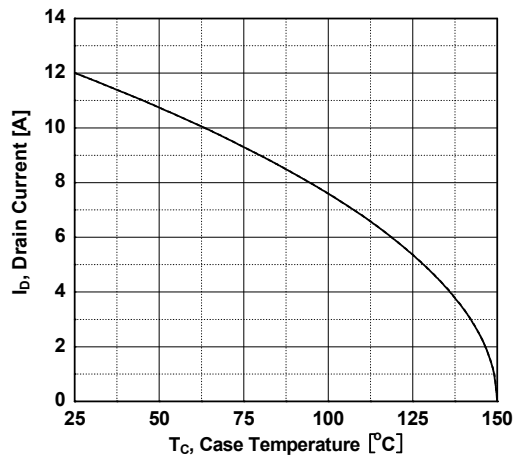


Figure 11. Transient Thermal Response Curve

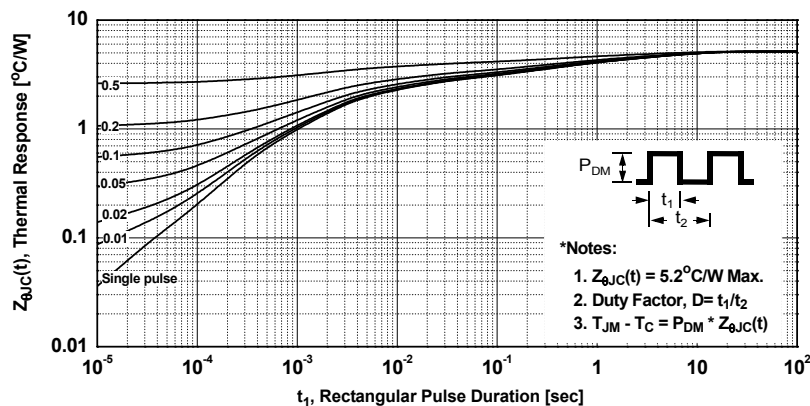




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms



Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

Figure 16. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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