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# FDS89141

## Dual N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET 100 V, 3.5 A, 62 mΩ

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 62 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 3.5\text{ A}$
- Max  $r_{DS(on)}$  = 100 mΩ at  $V_{GS} = 6\text{ V}$ ,  $I_D = 2.8\text{ A}$
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- 100% UIL Tested
- RoHS Compliant

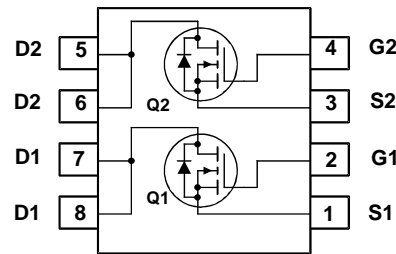
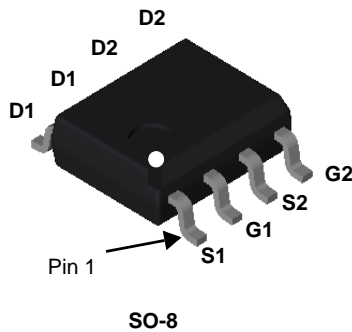


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that incorporates Shielded Gate technology. This process has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

### Applications

- Synchronous Rectifier
- Primary Switch For Bridge Topology



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

| Symbol         | Parameter                                        | Ratings     | Units |
|----------------|--------------------------------------------------|-------------|-------|
| $V_{DS}$       | Drain to Source Voltage                          | 100         | V     |
| $V_{GS}$       | Gate to Source Voltage                           | ±20         | V     |
| $I_D$          | Drain Current -Continuous                        | 3.5         | A     |
|                | -Pulsed                                          | 18          |       |
| $E_{AS}$       | Single Pulse Avalanche Energy (Note 3)           | 37          | mJ    |
| $P_D$          | Power Dissipation $T_A = 25\text{ °C}$ (Note 1a) | 31          | W     |
|                | Power Dissipation $T_A = 25\text{ °C}$ (Note 1b) | 1.6         |       |
| $T_J, T_{STG}$ | Operating and Storage Junction Temperature Range | -55 to +150 | °C    |

### Thermal Characteristics

|                 |                                                   |    |      |
|-----------------|---------------------------------------------------|----|------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case (Note 1)     | 40 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 78 |      |

### Package Marking and Ordering Information

| Device Marking | Device   | Package | Reel Size | Tape Width | Quantity   |
|----------------|----------|---------|-----------|------------|------------|
| FDS89141       | FDS89141 | SO-8    | 13 "      | 12 mm      | 2500 units |

FDS89141 Dual N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

### Off Characteristics

|                                      |                                           |                                                            |     |    |           |                      |
|--------------------------------------|-------------------------------------------|------------------------------------------------------------|-----|----|-----------|----------------------|
| $BV_{DSS}$                           | Drain to Source Breakdown Voltage         | $I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$              | 100 |    |           | V                    |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$ |     | 69 |           | mV/ $^\circ\text{C}$ |
| $I_{DSS}$                            | Zero Gate Voltage Drain Current           | $V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$              |     |    | 1         | $\mu\text{A}$        |
| $I_{GSS}$                            | Gate to Source Leakage Current            | $V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$          |     |    | $\pm 100$ | nA                   |

### On Characteristics

|                                        |                                                          |                                                                       |   |      |     |                      |
|----------------------------------------|----------------------------------------------------------|-----------------------------------------------------------------------|---|------|-----|----------------------|
| $V_{GS(th)}$                           | Gate to Source Threshold Voltage                         | $V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$                              | 2 | 3.1  | 4   | V                    |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$            |   | -9   |     | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$                           | Static Drain to Source On Resistance                     | $V_{GS} = 10 \text{ V}, I_D = 3.5 \text{ A}$                          |   | 47   | 62  | m $\Omega$           |
|                                        |                                                          | $V_{GS} = 6 \text{ V}, I_D = 2.8 \text{ A}$                           |   | 63   | 100 |                      |
|                                        |                                                          | $V_{GS} = 10 \text{ V}, I_D = 3.5 \text{ A}, T_J = 125^\circ\text{C}$ |   | 81   | 107 |                      |
| $g_{FS}$                               | Forward Transconductance                                 | $V_{DS} = 10 \text{ V}, I_D = 3.5 \text{ A}$                          |   | 14.7 |     | S                    |

### Dynamic Characteristics

|            |                              |                                                                  |  |     |     |          |
|------------|------------------------------|------------------------------------------------------------------|--|-----|-----|----------|
| $C_{iss}$  | Input Capacitance            | $V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ |  | 299 | 398 | pF       |
| $C_{oss}$  | Output Capacitance           |                                                                  |  | 70  | 93  | pF       |
| $C_{riss}$ | Reverse Transfer Capacitance |                                                                  |  | 4.7 | 7   | pF       |
| $R_g$      | Gate Resistance              |                                                                  |  | 1.0 |     | $\Omega$ |

### Switching Characteristics

|              |                               |                                                                                         |                                         |                                              |     |     |
|--------------|-------------------------------|-----------------------------------------------------------------------------------------|-----------------------------------------|----------------------------------------------|-----|-----|
| $t_{d(on)}$  | Turn-On Delay Time            | $V_{DD} = 50 \text{ V}, I_D = 3.5 \text{ A}, V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$ |                                         | 5                                            | 10  | ns  |
| $t_r$        | Rise Time                     |                                                                                         |                                         | 1.4                                          | 10  | ns  |
| $t_{d(off)}$ | Turn-Off Delay Time           |                                                                                         |                                         | 9.8                                          | 20  | ns  |
| $t_f$        | Fall Time                     |                                                                                         |                                         | 2.2                                          | 10  | ns  |
| $Q_{g(TOT)}$ | Total Gate Charge             |                                                                                         | $V_{GS} = 0 \text{ V to } 10 \text{ V}$ | $V_{DD} = 50 \text{ V}, I_D = 3.5 \text{ A}$ | 5.1 | 7.1 |
| $Q_{g(TOT)}$ | Total Gate Charge             | $V_{GS} = 0 \text{ V to } 5 \text{ V}$                                                  | 2.9                                     |                                              | 4.1 | nC  |
| $Q_{gs}$     | Gate to Source Charge         |                                                                                         | 1.4                                     |                                              |     | nC  |
| $Q_{gd}$     | Gate to Drain "Miller" Charge |                                                                                         | 1.3                                     |                                              |     | nC  |

### Drain-Source Diode Characteristics

|          |                                       |                                                          |  |     |     |    |
|----------|---------------------------------------|----------------------------------------------------------|--|-----|-----|----|
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS} = 0 \text{ V}, I_S = 3.5 \text{ A}$ (Note 2)     |  | 0.8 | 1.3 | V  |
|          |                                       | $V_{GS} = 0 \text{ V}, I_S = 2 \text{ A}$ (Note 2)       |  | 0.8 | 1.2 |    |
| $t_{rr}$ | Reverse Recovery Time                 | $I_F = 3.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ |  | 33  | 53  | ns |
| $Q_{rr}$ | Reverse Recovery Charge               |                                                          |  | 23  | 37  | nC |

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a  $1 \text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5 \text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $78^\circ\text{C/W}$  when mounted on a  $1 \text{ in}^2$  pad of 2 oz copper



b)  $135^\circ\text{C/W}$  when mounted on a minimum pad

- Pulse Test: Pulse Width  $< 300 \mu\text{s}$ , Duty cycle  $< 2.0\%$ .
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3.0 \text{ mH}$ ,  $I_{AS} = 5.0 \text{ A}$ ,  $V_{DD} = 100 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ .

**Typical Characteristics ( N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

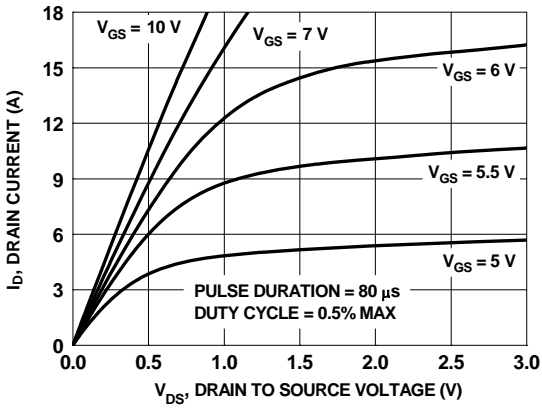


Figure 1. On-Region Characteristics

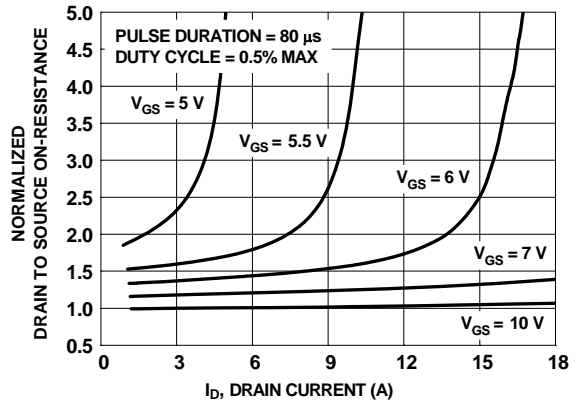


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

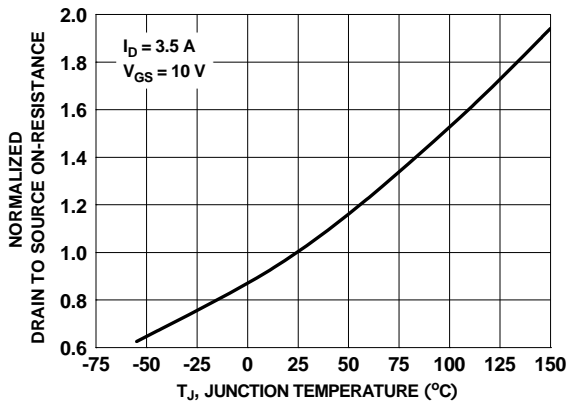


Figure 3. Normalized On-Resistance vs Junction Temperature

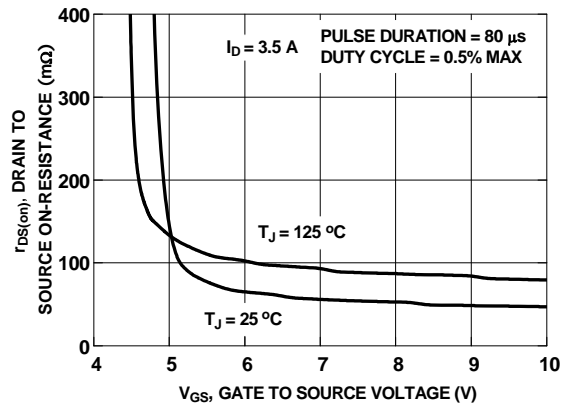


Figure 4. On-Resistance vs Gate to Source Voltage

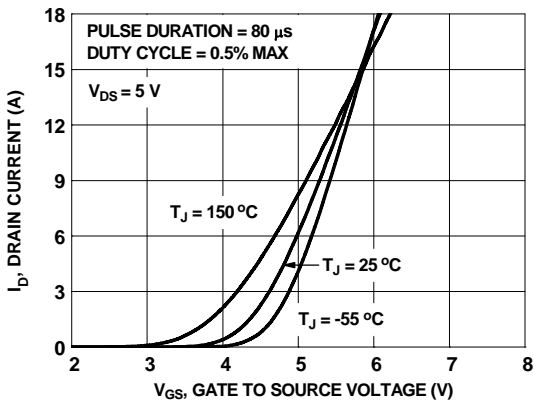


Figure 5. Transfer Characteristics

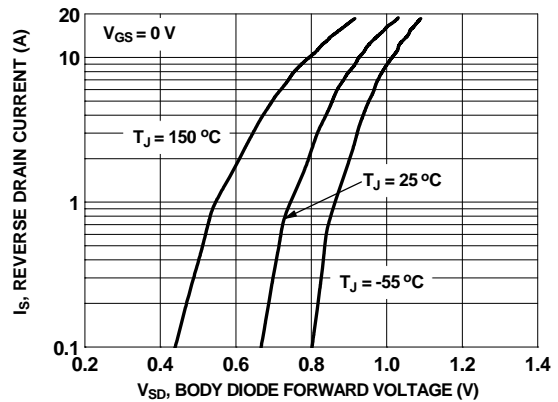
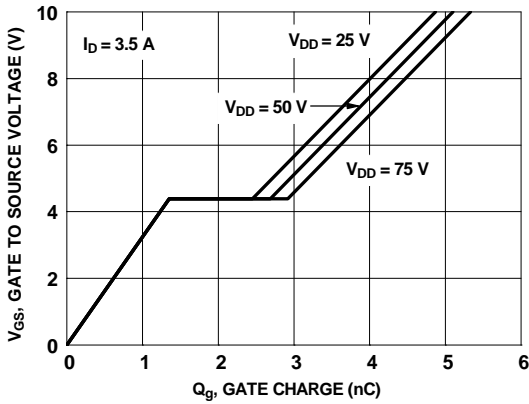
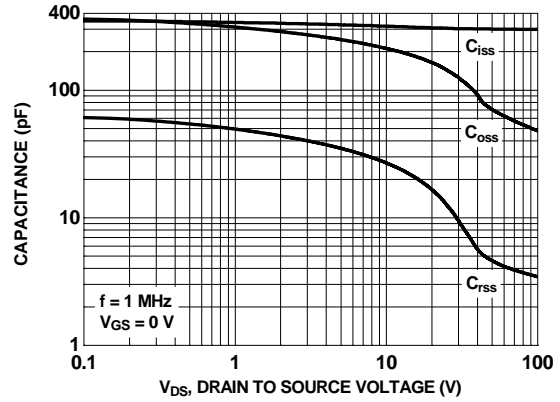


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

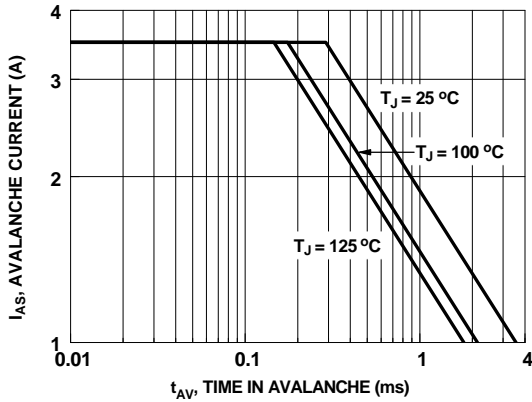
**Typical Characteristics ( N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



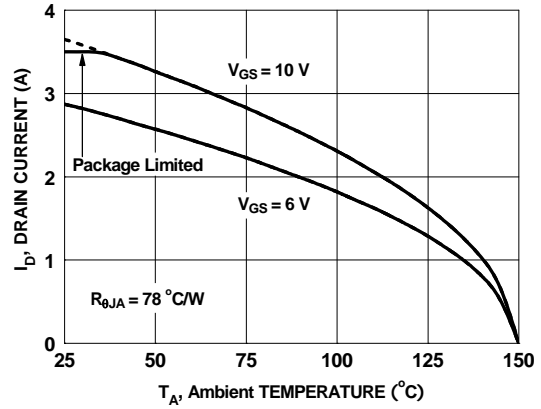
**Figure 7. Gate Charge Characteristics**



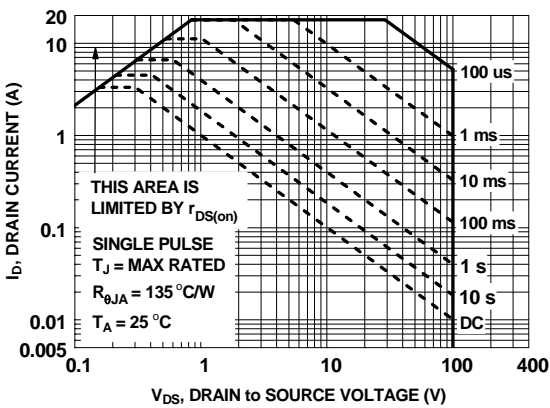
**Figure 8. Capacitance vs Drain to Source Voltage**



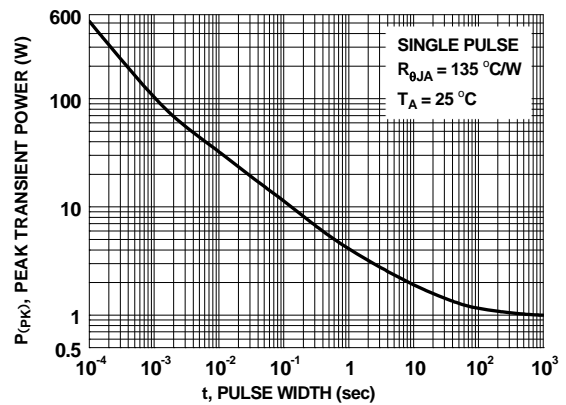
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

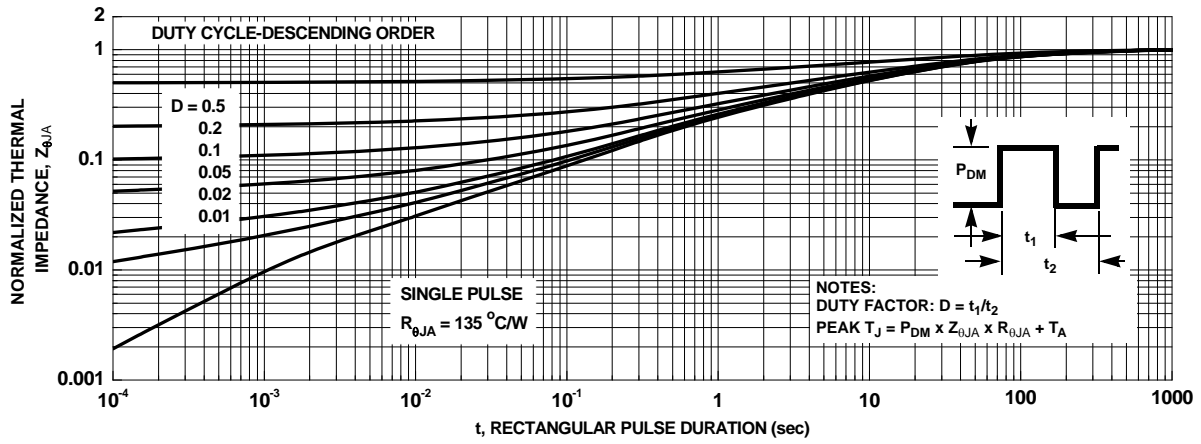


**Figure 11. Forward Bias Safe Operating Area**

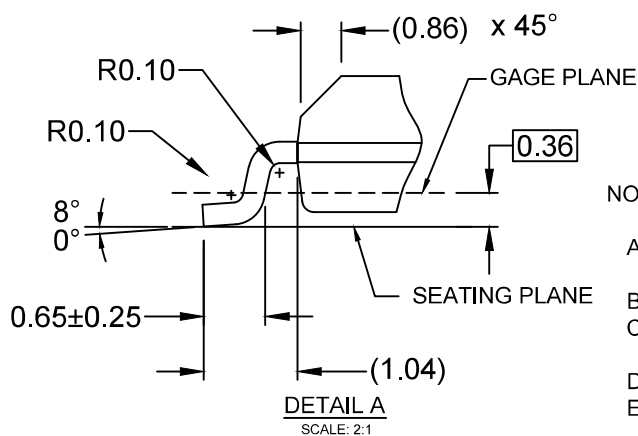
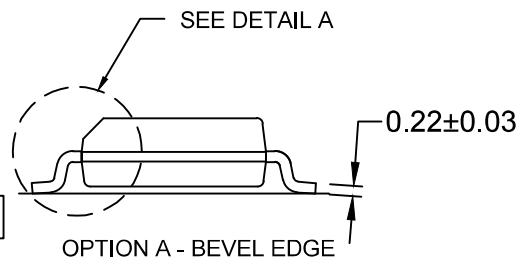
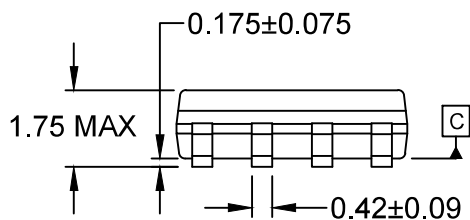
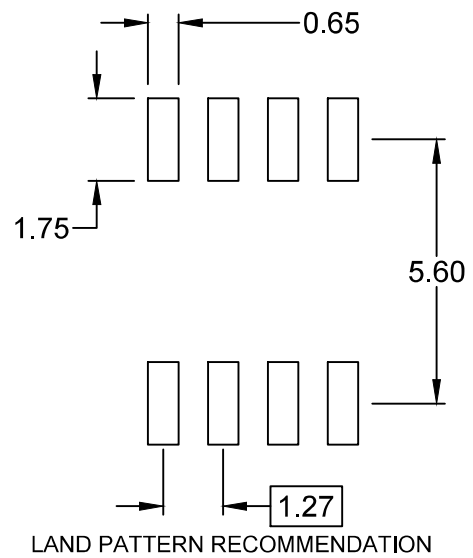
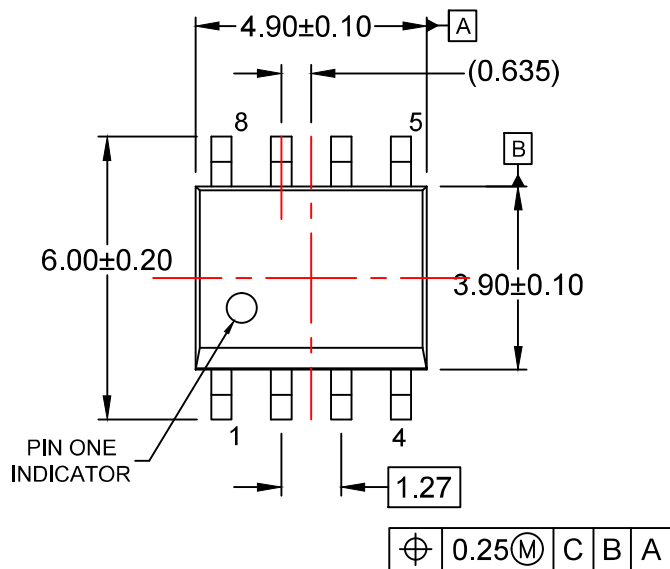


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics ( N-Channel )**  $T_J = 25^{\circ}\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16



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