PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/14/8508
Dated 16 Jul 2014

M24C64, 64-Kbit I2C Bus EEPROM Industrial grade / SO8N, TSSOP8 & UFDFPN8 packages Redesign and upgrade to the CMOSF8H+ process technology

Table 1. Change Implementation Schedule

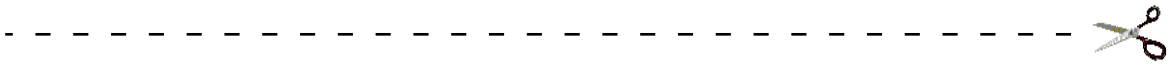
Forecasted implementation date for change	09-Jul-2014
Forecasted availability date of samples for customer	10-Oct-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	10-Oct-2014
Estimated date of changed product first shipment	15-Oct-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M24C64 products family in SO8N, TSSOP8 & UFDFPN8
Type of change	Waferfab process change
Reason for change	Line up to state-of-the-art of process
Description of the change	Redesign and upgrade to the new CMOSF8H+ Process technology.
Change Product Identification	Process Technology identifier "T"
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MMY/14/8508**
Please sign and return to STMicroelectronics Sales Office	**Dated 16 Jul 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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PRODUCT / PROCESS CHANGE NOTIFICATION

M24C64, 64-Kbit I2C Bus EEPROM
Industrial grade / SO8N, TSSOP8 & UFDFPN8 packages
Redesign and upgrade to the CMOSF8H+ process technology

What is the change?

The **M24C64**, 64-Kbit serial I²C bus EEPROM product family for Industrial grade, assembled in SO8N TSSOP8 & UFDFPN8 packages, currently produced using the CMOSF8H process technology at ST Rousset (France) 8" wafer diffusion plant, has been **redesigned** and will be **upgraded** to the **CMOSF8H+** process technology at the same wafer diffusion plant.

The CMOSF8H+ is closely derived from CMOSF8H (already used for production of densities ranging from 64 Kb to 2 Mb), with a more compact layout, in order to achieve competitive die size.

This upgraded version in CMOSF8H+ allows offering UFDFPN5 (1.4 mm x 1.7 mm while UFDFPN8 is 2 mm x 3 mm).

The new M24C64 in CMOSF8H+ version is functionally compatible with the current CMOSF8H version as per datasheet rev. 28 – November 2013, attached.

Following parameters will be updated in revised datasheet rev. 29:

- AC characteristics:
  - $t_{CLQX\ (min)}$ & $t_{NS\ (max)}$ at 50 ns
- Absolute maximum rating: V_{ESD} electrostatic pulse Human Body model:
  - Max 3000 V

Concurrent to this change, the M24C64 in CMOSF8H+ in SO8N, TSSOP8 & UFDFPN8 will be assembled with 0.8 mil Copper wire.

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M24C64 in the new CMOSF8H+ process technology will increase the production capacity throughput and consequently improve the service to our customers.

When?

The production of the upgraded M24C64 with the new CMOSF8H+ will ramp up from August 2014 and shipments can start from October 2014 onward (or earlier upon customer approval).

How will the change be qualified?

The new version of the M24C64 in CMOSF8H+ will be qualified using the standard ST Microelectronics Corporate Procedures for Quality & Reliability.

The **Qualification Plan QPMMY1311** is included inside this document.

What is the impact of the change?

- Form: Marking change (see **Device marking** paragraph)

- Fit: No change

- Function:

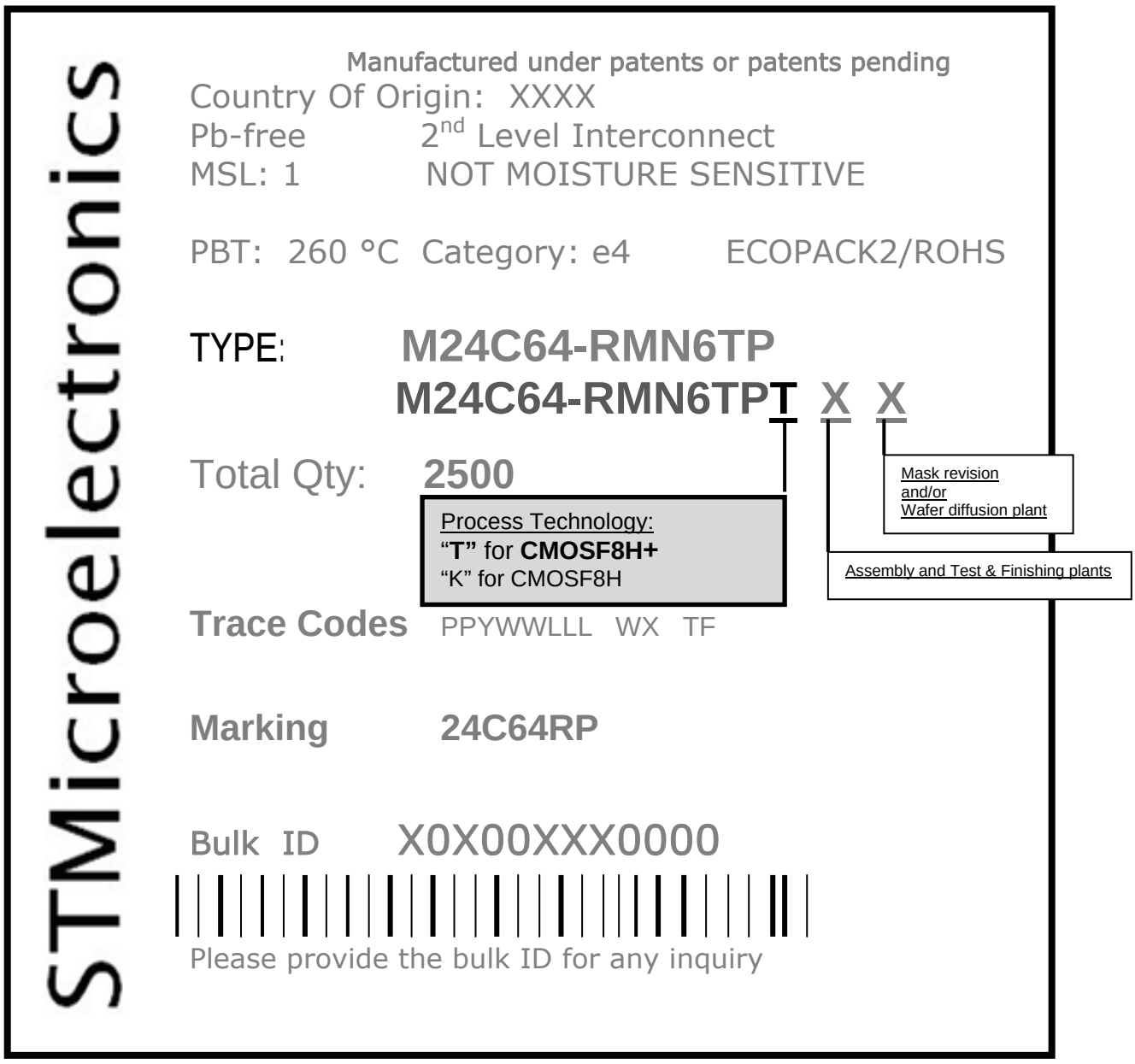
- Change on Absolute maximum rating $\mathbf{V_{ESD}}$ **HBM** from 4000 V to **3000 V**
- Change on $\mathbf{t_{CLQX\ (min)}}$ & $\mathbf{t_{NS\ (max)}}$ respectively from 100 ns & 80 ns to **50 ns** for both

How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **process technology** identifier is "**T**" for the **upgraded version** in **CMOSF8H+**, this identifier being "K" for the current version in CMOSF8H.

➔ *Example for M24C64-RMN6TP*



How can the change be seen?

- DEVICE MARKING

For the **SO8N**, the difference is visible inside the **trace code** PYWWT where the last digit T for Process Technology is "**T**" for the **upgraded version** in **CMOSF8H+**, this digit being "K" for current CMOSF8H version.

	Upgraded CMOSF8H+	Current CMOSF8H
Example: M24C64-RMN6TP	24C64RP *PYWW***T**	24C64RP *PYWW***K**

	Upgraded CMOSF8H+	Current CMOSF8H
TSSOP8 Example: M24C64-RDW6TP	O 464R**T** *PYWW*	O 464R**K** *PYWW*

For the **UFDFPN8** package, the difference is visible inside the product name.
Example for M24C64-FMC6TG: **upgraded version** in **CMOSF8H+** is **4FFT**, current version being 464F.

	Upgraded CMOSF8H+	Current CMOSF8H
UFDFPN8 Example: M24C64-FMC6TG	O 4**FFT** *PYWW*	O 464F *PYWW*

Appendix A- Product Change Information

Product family / Commercial products:	M24C64 products family assembled in SO8N, TSSOP8 & UFDFPN8 packages / Industrial grade
Customer(s):	All
Type of change:	Wafer fab process technology change
Reason for the change:	Line up to state-of-the-art of process
Description of the change:	Redesign and upgrade to the new CMOSF8H+ Process technology.
Forecast date of the change: (Notification to customer)	Week 28 / 2014
Forecast date of Qualification samples availability for customer(s):	See APPENDIX B
Forecast date for the internal STMicroelectronics change, Qualification Report availability:	The **Qualification Plan QPMM1311** is included inside this document. **Qualification Report QRMM1311** will be available - Week 37 / 2014 for UFDFPN8 - Week 41 / 2014 for SO8 / TSSOP8
Marking to identify the changed product:	Process Technology identifier "**T"** for CMOSF8H+
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See APPENDIX B
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	Week 42 / 2014

Appendix B: Concerned Commercial Part Numbers:

Commercial Part Numbers	Package	Samples availability
M24C64-FDW6TP	TSSOP8	Week 41 / 2014
M24C64-FMC6TG	UFDFPN8	Week 37 / 2014
M24C64-FMN6TP	SO8	Week 41 / 2014
M24C64-RDW6TP	TSSOP8	Week 41 / 2014
M24C64-RMN6P	SO8	No samples in tube
M24C64-RMN6TP	SO8	Week 41 / 2014
M24C64-WDW6TP (1)	TSSOP8	Week 41 / 2014
M24C64-WMN6P (1)	SO8	No samples in tube
M24C64-WMN6TP (1)	SO8	Week 41 / 2014

Note (1): Following product line rationalization, we recommend customer to use "**–R**" version (1.8 V – 5.5 V) when "–W" (2.5 V – 5.5 V) is used.
For instance, **M24C64-RDW6TP should be preferred** to *M24C64-WDW6TP*.

Appendix C: Qualification Plan:

See following pages

M24C64 Redesign and Upgrade to the CMOSF8H+ process technology Qualification Plan QPMMY1311 (1/5)

- The new version of the M24C64 in CMOSF8H+ will be qualified using the standard STMicroelectronics corporate procedures for quality and reliability.
- The CMOSF8H+ process technology has been qualified on 3 lots using the driver product M24C16 (refer to qualification report QRMMY1126).
- The new M24C64 is designed with the same architecture and technology as the driver product M24C16. Qualification of the new M24C64 benefits of the family approach (1 lot).

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M24C64 Redesign and Upgrade to the CMOSF8H+ process technology Qualification Plan QPMMY1311 (2/5)

- The product vehicles used for the die qualification are presented in *Table 1*.

Table 1. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24C16	CMOSF8H+	ST Rousset 8"	CDIP8	Engineering assy (1)
M24C64 (2)	CMOSF8H+	ST Rousset 8"	CDIP8	Engineering assy (1)

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.
2. Qualification on 3 lots using the driver product M24C16 - Qualification of M24C64 benefits of the family approach (1 lot).

- The product vehicles used for package qualification are presented in *Table 2*.

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24C64 (1)	CMOSF8H+	ST Rousset 8"	SO8N	ST Shenzhen / Subcon Amkor
			TSSOP8	ST Shenzhen / Subcon Amkor
			UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba / Subcon Amkor
			UFDFPN5 (MLP5) 1.7 x 1.4 mm	ST Calamba

1. Qualification on 3 lots using the driver product M24C16 - Qualification of M24C64 benefits from the family approach (1 lot).

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M24C64 Redesign and Upgrade to the CMOSF8H+ process technology
Qualification Plan QPMMY1311 (3/5)

- The reliability test plan related to the new M24C64 is presented as follows :

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Acceptance Criteria
EDR	**High temperature operating life after endurance**					
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTOL 150 °C, 6v	80	1	1008 hrs	0/80
	Data retention after endurance					
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTSL 150 °C	80	1	1008 hrs	0/80
LTOL	**Low temperature operating life**					
	JESD22-A108	-40 °C, 6v	80	1	1008 hrs	0/80
HTSL	**High temperature storage life**					
	JESD22-A103	Retention bake at 200 °C	80	1	1008 hrs	0/80
WEB	**Program/erase endurance cycling + bake**					
	Internal spec.	5 million cycles at 25 °C then: retention bake at 200 °C / 48 hrs	80	1	5 million cycles / 48hrs	0/80

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M24C64 Redesign and Upgrade to the CMOSF8H+ process technology
Qualification Plan QPMMY1311 (4/5)

Test	Test short description					
	Method	**Conditions**	**Sample size / lots**	**No. of lots**	**Duration**	**Acceptance Criteria**
ESD HBM	**Electrostatic discharge (human body model)**					
	AEC-Q100-002 ANSI/ESDA/JEDEC JS-001-2012	C = 100 pF, R = 1500 Ohms	27	1	N/A	PASS 3000 V
ESD MM	**Electrostatic discharge (machine model)**					
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ohms	12	1	N/A	PASS 200 V
LU	**Latch-up (current injection and over-voltage stress)**					
	AEC-Q100-004 JESD78B	At 150 °C	6	1	N/A	Class II – Level A

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M24C64 Redesign and Upgrade to the CMOSF8H+ process technology
Qualification Plan QPMMY1311 (5/5)

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Acceptance Criteria
PC	**Preconditioning: moisture sensitivity level 1**					
	JESD22-A113 / J-STD-020D	MSL1, peak temperature at 260°C, 3 Ireflows	345	1	N/A	0/345
THB (1)	**Temperature humidity bias**					
	AEC-Q100 / JESD22-A101	85 °C, 85% RH, bias 5.6V	80	1	1008 hrs	0/80
TC (1)	**Temperature cycling**					
	AEC-Q100 / JESD22-A104	-65 °C / +150 °C	80	1	1000 cy	0/80
TMSK (1)	**Thermal shocks**					
	JESD22-A106	-55 °C / +125 °C	25	1	200 shocks	0/25
AC (1)	**Autoclave (pressure pot)**					
	AEC-Q100 / JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	96 hrs	0/80
HTSL (1)	**High temperature storage life**					
	AEC-Q100 / JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ESD CDM	**Electrostatic discharge (charge device model)**					
	AEC-Q100–011 ANSI-ESDSTM5 3 1-1999	Field induced charging method	18	1	N/A	PASS 1500V

1. THB-, TC-, TMSK-, AC-, and HTSL- dedicated parts are first subject to preconditioning flow.

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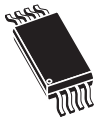
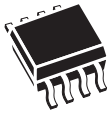
M24C64-W M24C64-R M24C64-F M24C64-DF

64-Kbit serial I²C bus EEPROM

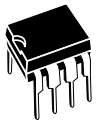
Datasheet - production data



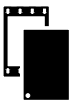
TSSOP8 (DW)
169 mil width



SO8 (MN)
150 mil width



PDIP8 (BN)



UFDFPN8
(MC)

WLCSP (CS)

Thin WLCSP (CT)

Features

- Compatible with all I²C bus modes:
  - 1 MHz
  - 400 kHz
  - 100 kHz
- Memory array:
  - 64 Kbit (8 Kbytes) of EEPROM
  - Page size: 32 bytes
  - Additional Write lockable page (M24C64-D order codes)
- Single supply voltage:
  - 1.7 V to 5.5 V over –40 °C / +85 °C
- Write:
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Random and sequential Read modes
- Write protect of the whole memory array
- Enhanced ESD/Latch-Up protection
- More than 4 million Write cycles
- More than 200-year data retention
- Packages:
  - RoHS compliant and halogen-free (ECOPACK®)

This is information on a product in full production. www.st.com

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Figure 21. Thin WLCSP 8-bump wafer-length chip-scale package outline (M24C64-DFCT6TP/K) . . . 38

1 Description

The M24C64 is a 64-Kbit I^2C-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 8 K × 8 bits.

The M24C64-W can operate with a supply voltage from 2.5 V to 5.5 V, the M24C64-R can operate with a supply voltage from 1.8 V to 5.5 V, and the M24C64-F and M24C64-DF can operate with a supply voltage from 1.7 V to 5.5 V, over an ambient temperature range of -40 °C / +85 °C.

The M24C64-D offers an additional page, named the Identification Page (32 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

Figure 1. Logic diagram

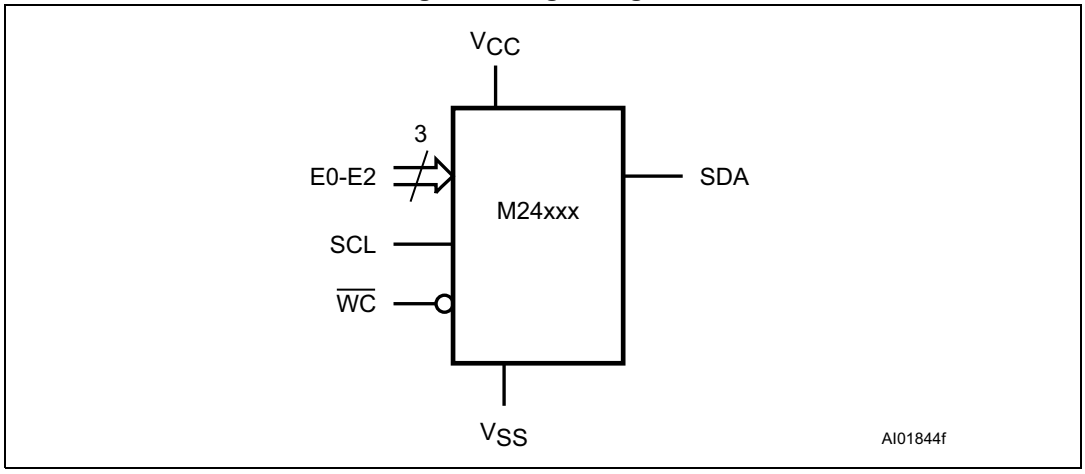
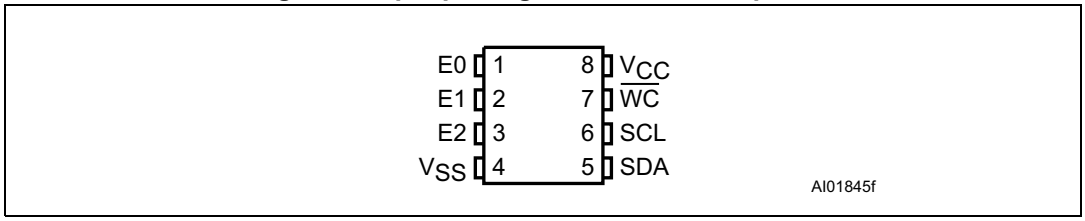


Table 1. Signal names

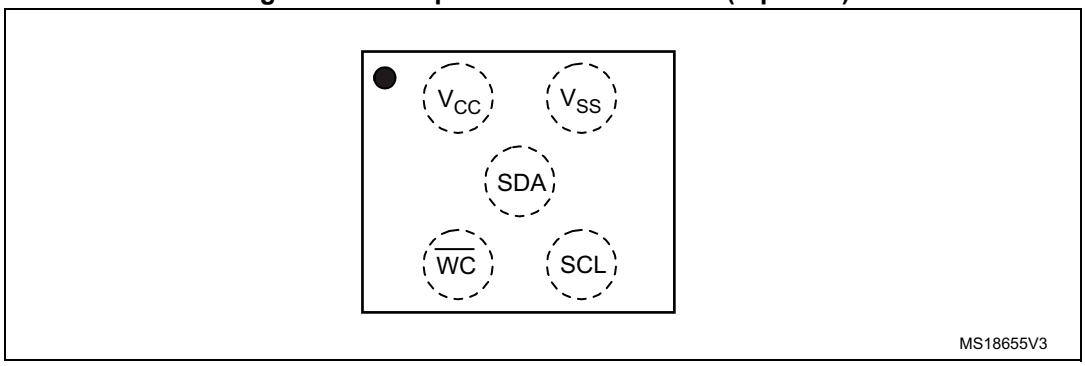
Signal name	Function	Direction
E2, E1, E0	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
$\overline{WC}$	Write Control	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. 8-pin package connections, top view



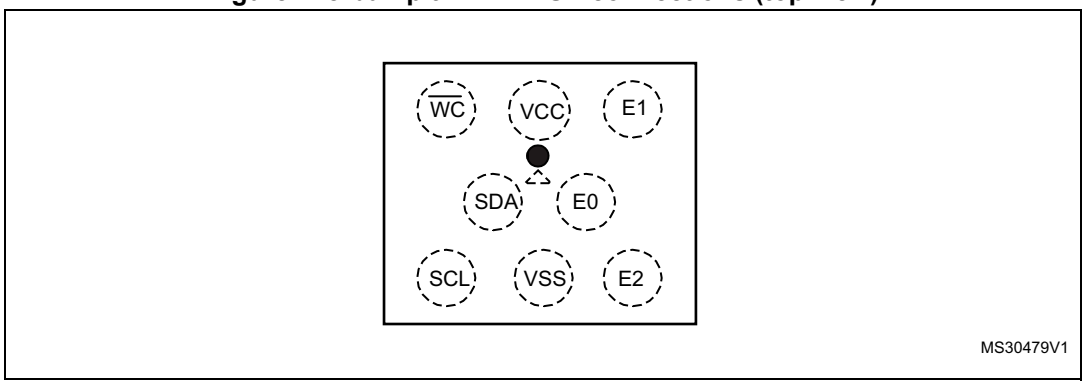
1. See *Section 9: Package mechanical data* for package dimensions, and how to identify pin 1.

Figure 3. 5-bump WLCSP connections (top view)



Note: Inputs E2, E1, E0 are internally connected to (001). Please refer to Section 2.3 for further explanations.

Figure 4. 8-bump thin WLCSP connections (top view)



Caution: As EEPROM cells lose their charge (and so their binary value) when exposed to ultra violet (UV) light, EEPROM dice delivered in wafer form or in WLCSP package by STMicroelectronics must never be exposed to UV light.

2 Signal description

2.1 Serial Clock (SCL)

The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

2.2 Serial Data (SDA)

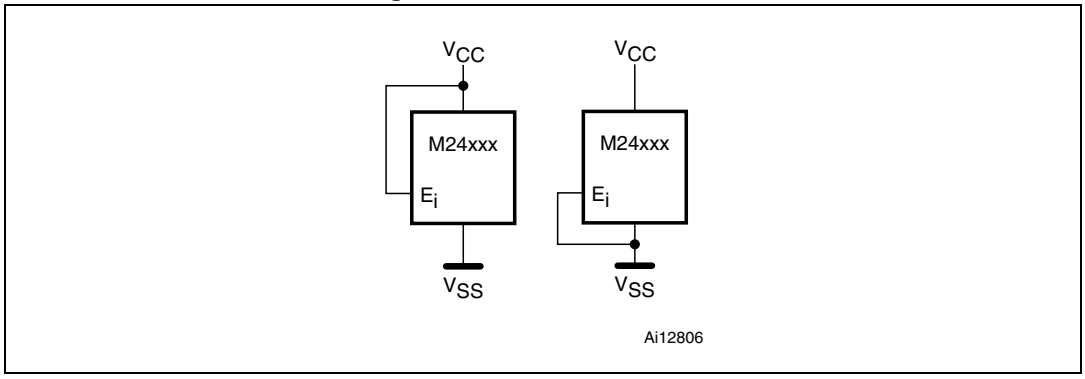
SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to V_{CC} (*Figure 13* indicates how to calculate the value of the pull-up resistor).

2.3 Chip Enable (E2, E1, E0)

(E2,E1,E0) input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code. These inputs must be tied to V_{CC} or V_{SS}, as shown in *Table 2: Device select code*. When not connected (left floating), these inputs are read as low (0).

For the 5-balls WLCSP package, the (E2,E1,E0) inputs are internally connected to (0,0,1).

Figure 5. Device select code



2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven high. Write operations are enabled when Write Control ($\overline{WC}$) is either driven low or left floating.

When Write Control ($\overline{WC}$) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in *Section 8: DC and AC parameters)*. In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters)* and the rise time must not vary faster than 1 V/µs.

2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see Operating conditions in *Section 8: DC and AC parameters*).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

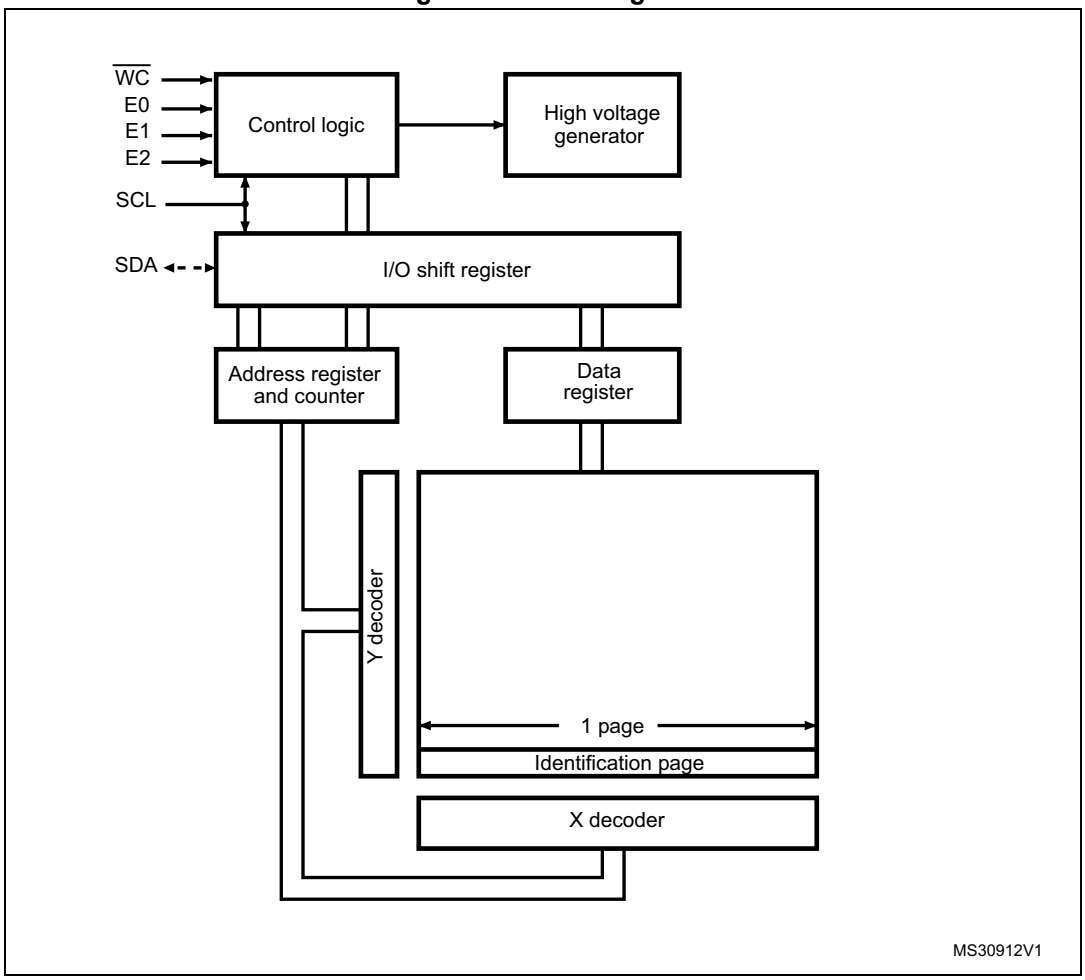
2.6.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

3 Memory organization

The memory is organized as shown below.

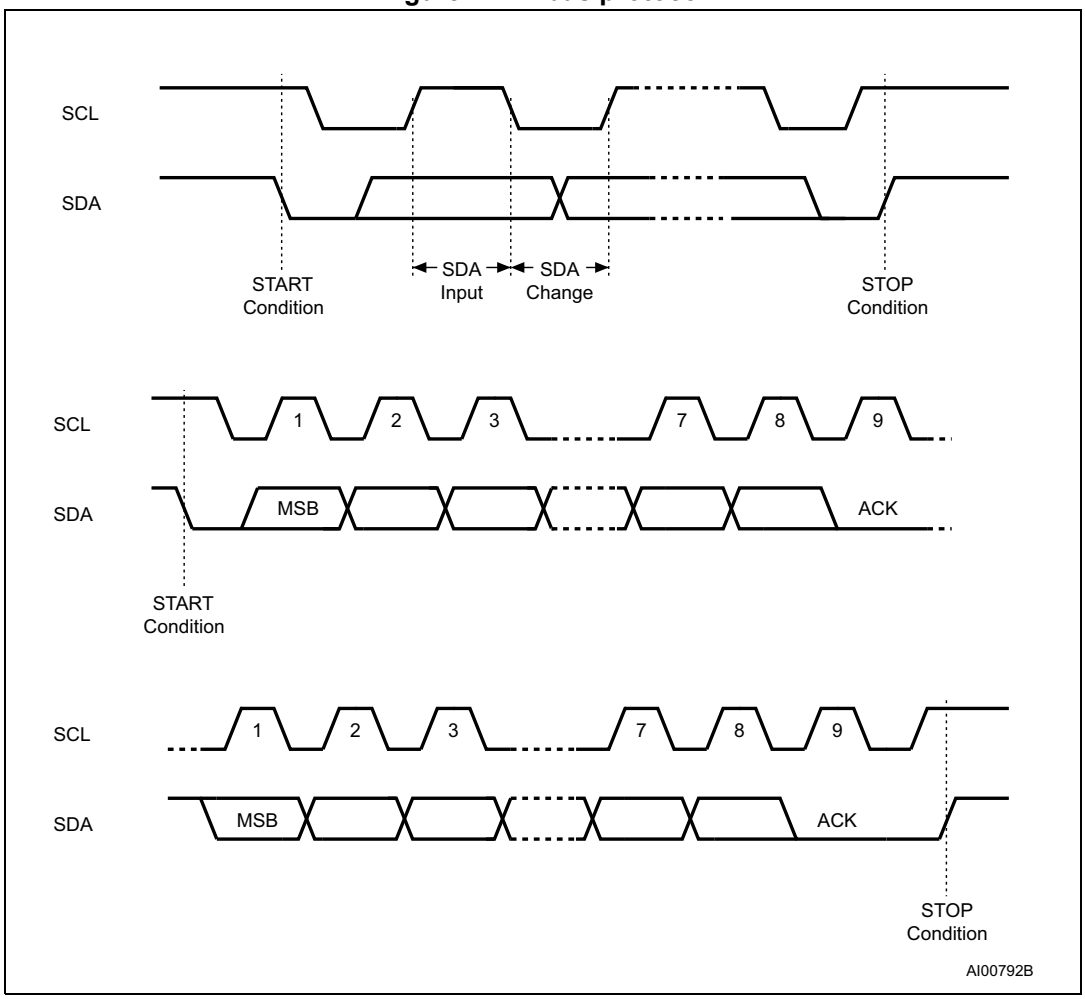
Figure 6. Block diagram



4 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 7*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 7. I^2C bus protocol



4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

4.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on Serial Data (SDA), most significant bit first).

Table 2. Device select code

	Device type identifier(1)				Chip Enable address(2)			$\overline{RW}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code when addressing the memory array	1	0	1	0	E2	E1	E0	$R\overline{W}$
Device select code when accessing the Identification page	1	0	1	1	E2	E1	E0	$R\overline{W}$

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared with the value read on input pins E0, E1,and E2.

When the device select code is received, the device only responds if the Chip Enable address is the same as the value on its Chip Enable E2,E1,E0 inputs.

The 8th bit is the Read/$\overline{\text{Write}}$ bit ($R\overline{W}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, the device deselects itself from the bus, and goes into Standby mode.

5 Instructions

5.1 Write operations

Following a Start condition the bus master sends a device select code with the R/$\overline{W}$ bit (R$\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 8*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Table 3. Most significant address byte

A15	A14	A13	A12	A11	A10	A9	A8

Table 4. Least significant address byte

A7	A6	A5	A4	A3	A2	A1	A0

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle t_W is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition and the successful completion of an internal Write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

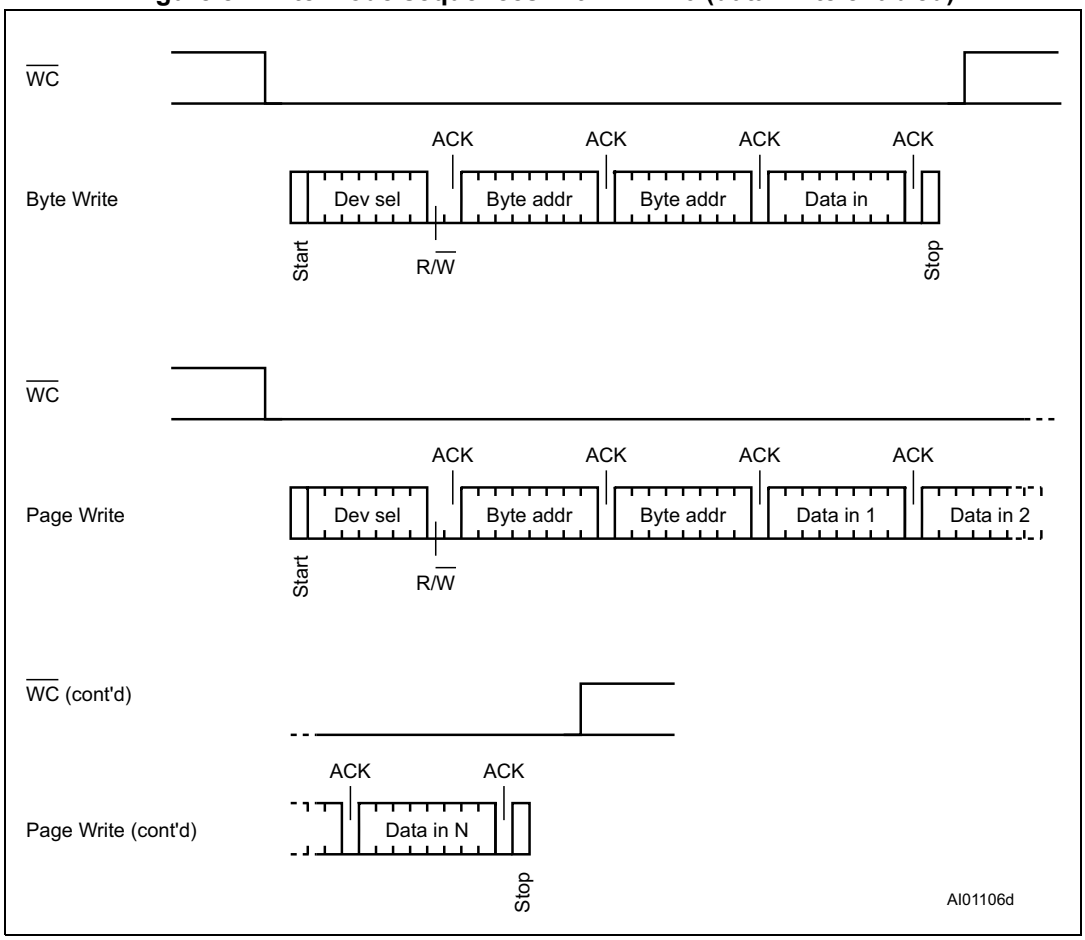
During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

If the Write Control input (WC) is driven High, the Write instruction is not executed and the accompanying data bytes are *not* acknowledged, as shown in *Figure 9*.

5.1.1 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 8*.

Figure 8. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)



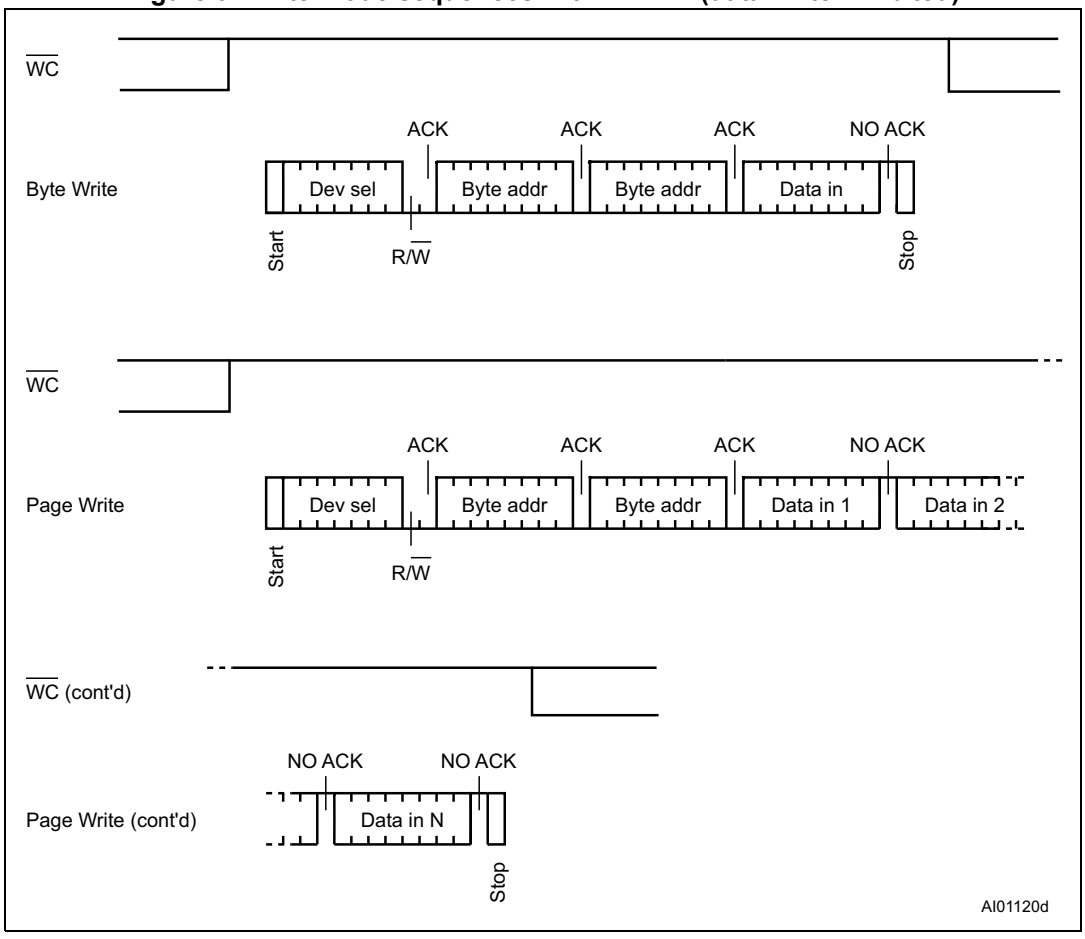
5.1.2 Page Write

The Page Write mode allows up to 32 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A15/A5, are the same. If more bytes are sent than will fit up to the end of the page, a “roll-over” occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 32 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is low. If Write Control ($\overline{WC}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck, as shown in *Figure 9*. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a Stop condition.

Figure 9. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



5.1.3 Write Identification Page (M24C64-D only)

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits A15/A5 are don't care except for address bit A10 which must be ‘0’. LSB address bits A4/A0 define the byte address inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

5.1.4 Lock Identification Page (M24C64-D only)

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be ‘1’; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

5.1.5 ECC (Error Correction Code) and Write cycling

The Error Correction Code (ECC) is an internal logic function which is transparent for the I^2C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes[(a)]. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group[(a)]. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined *Table 11: Cycling performance by groups of four bytes*.

a. A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.

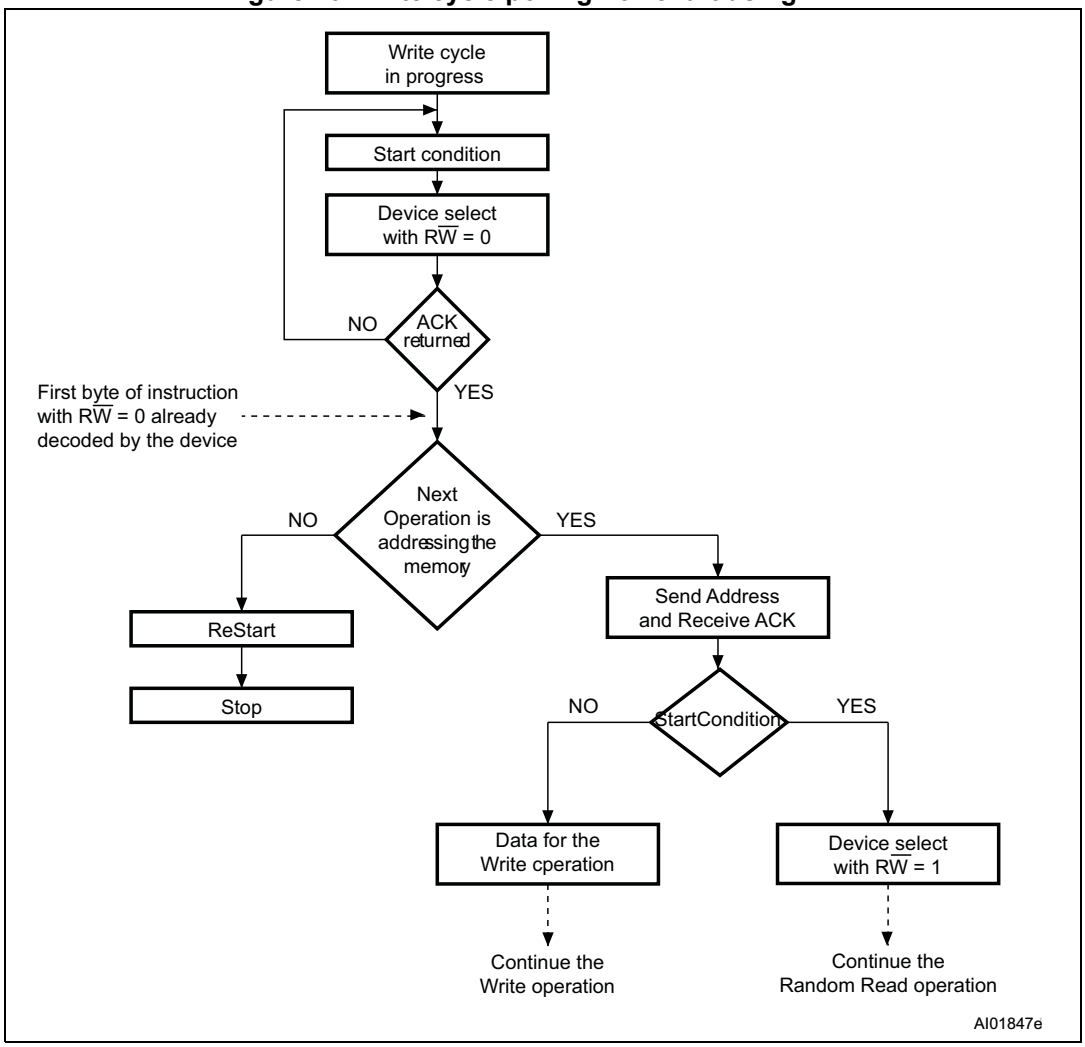
5.1.6 Minimizing Write delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in AC characteristics tables in *Section 8: DC and AC parameters*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 10*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 10. Write cycle polling flowchart using ACK



1. The seven most significant bits of the Device Select code of a Random Read (bottom right box in the figure) must be identical to the seven most significant bits of the Device Select code of the Write (polling instruction in the figure).

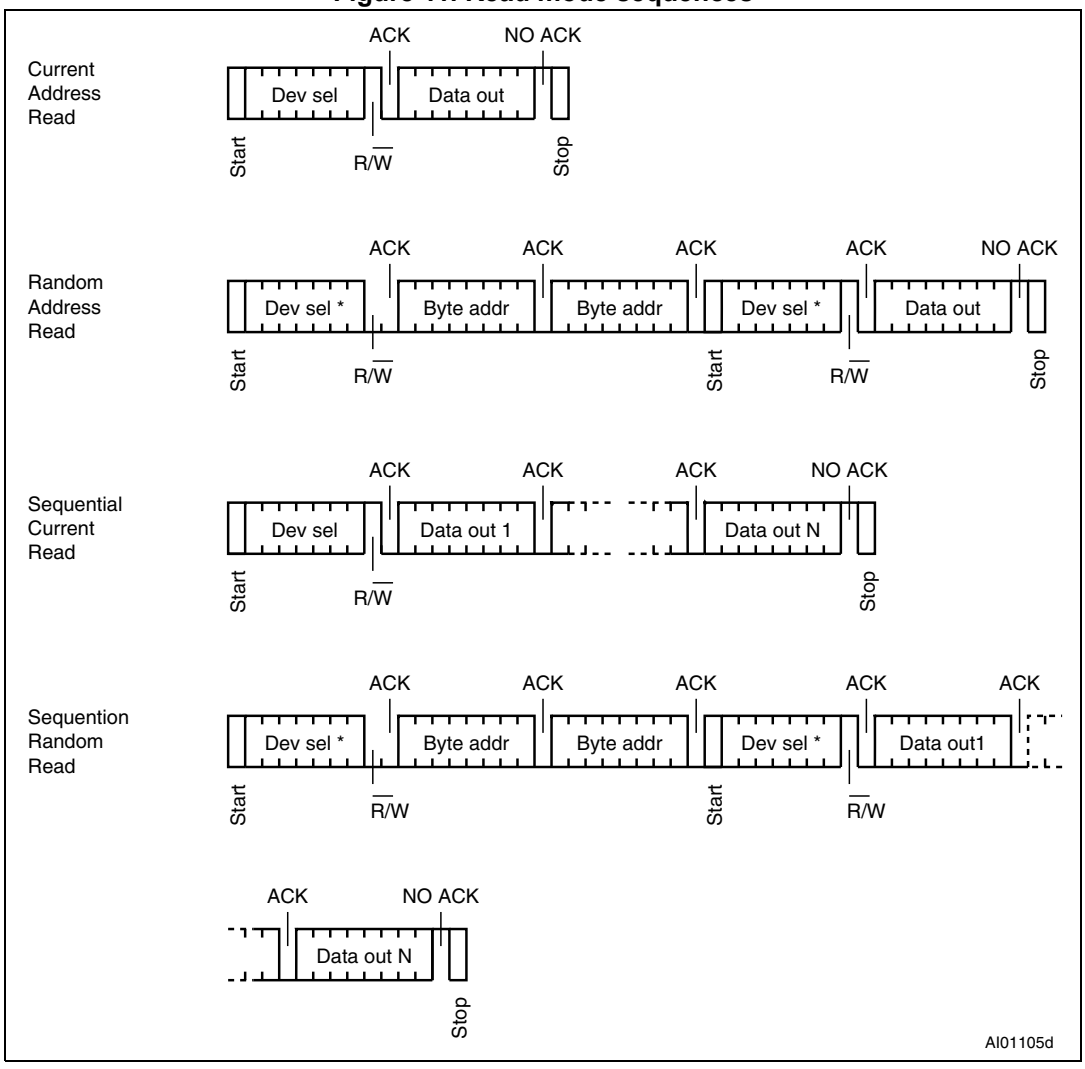
5.2 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the Read instructions, after each byte read (data out), the device waits for an acknowledgment (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

Figure 11. Read mode sequences



5.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 11*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the R/W bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 11*, *without* acknowledging the byte.

Note that the address counter value is defined by instructions accessing either the memory or the Identification page. When accessing the Identification page, the address counter value is loaded with the byte location in the Identification page, therefore the next Current Address Read in the memory uses this new address counter value. When accessing the memory, it is safer to always use the Random Address Read instruction (this instruction loads the address counter with the byte location to read in the memory, see *Section 5.2.1*) instead of the Current Address Read instruction.

5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 11*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

5.3 Read Identification Page (M24C64-D only)

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing an Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits A15/A5 are don't care, the LSB address bits A4/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 bytes).

5.4 Read the lock status (M24C64-D only)

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoAck bit if the Identification page is locked.

Right after this, it is recommended to transmit to the device a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic,
- Stop: the device is then set back into Standby mode by the Stop condition.

6 Initial delivery state

The device is delivered with all the memory array bits and Identification page bits set to 1 (each byte contains FFh).

7 Maximum rating

Stressing the device outside the ratings listed in *Table 5* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note(1)		°C
	PDIP-specific lead temperature during soldering	-	260(2)	°C
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{IO}	Input or output range	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body model)(3)	-	4000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb-free assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions of Hazardous Substances (RoHS) 2011/65/EU.
2. T_{LEAD} max must not be applied for more than 10 s.
3. Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω).

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 6. Operating conditions (voltage range W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	1(1)	MHz

1. f_{Cmax} is 1 MHz devices identified by process letter K.

Table 7. Operating conditions (voltage range R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	1(1)	MHz

1. f_{Cmax} is 1 MHz devices identified by process letter K.

Table 8. Operating conditions (voltage range F)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	1(1)	MHz

1. f_{Cmax} is 1 MHz devices identified by process letter K.

Table 9. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	100		pF
	SCL input rise/fall time, SDA input fall time	-	50	ns
	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 12. AC measurement I/O waveform

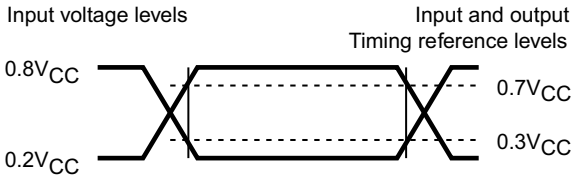


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Table 10. Input parameters

Symbol	Parameter(1)	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)	-	-	8	pF
C_{IN}	Input capacitance (other pins)	-	-	6	pF
Z_L	Input impedance (E2, E1, E0, $\overline{WC}$)(2)	V_{IN} < 0.3 V_{CC}	30	-	kΩ
Z_H		V_{IN} > 0.7 V_{CC}	500	-	kΩ

1. Characterized only, not tested in production.
2. E2, E1, E0 input impedance when the memory is selected (after a Start condition).

Table 11. Cycling performance by groups of four bytes

Symbol	Parameter	Test condition(1)	Max.	Unit
Ncycle	Write cycle endurance(2)	$T_A \leq$ 25 °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	4,000,000	Write cycle(3)
		T_A = 85 °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	1,200,000	

1. Cycling performance for products identified by process letter K.
2. The Write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer. The Write cycle endurance is defined by characterization and qualification.
3. A Write cycle is executed when either a Page Write, a Byte Write, a Write Identification Page or a Lock Identification Page instruction is decoded. When using the Byte Write, the Page Write or the Write Identification Page, refer also to *Section 5.1.5: ECC (Error Correction Code) and Write cycling*.

Table 12. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention(1)	T_A = 55 °C	200	Year

1. For products identified by process letter K. The data retention behavior is checked in production, while the 200-year limit is defined from characterization and qualification results.

Table 13. DC characteristics (M24C64-W, device grade 6)

Symbol	Parameter	Test conditions (in addition to those in *Table 6*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	2.5 V < V_{CC} < 5.5 V, f_c = 400 kHz (rise/fall time < 50 ns)	-	2	mA
		2.5 V < V_{CC} < 5.5 V, f_c = 1 MHz(1) (rise/fall time < 50 ns)	-	2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 2.5 V ≤ V_{CC} ≤ 5.5 V	-	5(2)	mA
I_{CC1}	Standby supply current	Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V	-	2	µA
		Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V	-	3(4)	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	-	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	-	0.7 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$, E2, E1, E0)	-	0.7 V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	V

1. Only for devices identified with process letter K.
2. Characterized value, not tested in production.
3. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).
4. Only for new products identified with process letter K, previous products offer $I_{CC1(max)}$ = 5 µA

Table 14. DC characteristics (M24C64-R, device grade 6)

Symbol	Parameter	Test conditions[1] (in addition to those in *Table 7*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, f_c= 400 kHz	-	0.8	mA
		f_c= 1 MHz[2]	-	2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 1.8 V ≤ V_{CC} < 2.5 V	-	3[3]	mA
I_{CC1}	Standby supply current	Device not selected[4], $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V	-	1	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	1.8 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	6.5	V
	Input high voltage ($\overline{WC}$)	1.8 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+ 0.6	V
V_{OL}	Output low voltage	I_{OL} = 1 mA[5], V_{CC} = 1.8 V	-	0.2	V

1. If the application uses the voltage range R device with 2.5 V < V_{cc} < 5.5 V and -40 °C < T_A < +85 °C, please refer to *Table 13* instead of this table.
2. Only for devices identified with process letter K.
3. Characterized value, not tested in production.
4. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).
5. I_{OL} = 0.7 mA for previous devices (identified by process letters G or S).

Table 15. DC characteristics (M24C64-F, M24C64-DF, device grade 6)

Symbol	Parameter	Test conditions[1] (in addition to those in *Table 8*)	Min.	Max.	Unit
I_{LI}	Input leakage current (E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.7 V, f_c= 400 kHz	-	0.8	mA
		f_c= 1 MHz[2]	-	2.5	mA
I_{CC}	Supply current (Read)	V_{CC} = 1.7 V, f_c= 400 kHz	-	0.8	mA
I_{CC0}	Supply current (Write)	During t_W 1.7 V < V_{CC} < 2.5 V	-	3[3]	mA
I_{CC1}	Standby supply current	Device not selected[4], $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.7 V	-	1	µA
V_{IL}	Input low voltage (SCL, SDA, WC)	1.7 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	1.7 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	6.5	V
	Input high voltage (WC, E2, E1, E0)	1.7 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.7 V	-	0.2	V

1. If the application uses the voltage range F device with 2.5 V < V_{CC} < 5.5 V and -40 °C < T_A < +85 °C, please refer to *Table 13* instead of this table.
2. Only for devices identified by process letter K (see *Table 17*).
3. Characterized value, not tested in production.
4. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 16. 400 kHz AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2}(1)	t_F	SDA (out) fall time	20(2)	300	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}(4)	t_{DH}	Data out hold time	100(5)	-	ns
t_{CLQV}(6)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_{WLDL}(7)(1)	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	µs
t_{DHWH}(8)(1)	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	µs
t_W	t_{WR}	Internal Write cycle duration	-	5	ms
t_{NS}(1)		Pulse width ignored (input filter on SCL and SDA) - single glitch	-	80(9)	ns

1. Characterized only, not tested in production.
2. With C_L = 10 pF.
3. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.
4. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
5. The previous product identified by process letter P was specified with t_{CLQX} = 200 ns (min). Both values offer a safe margin compared to the I^2C specification recommendations.
6. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3V_{CC}$ or $0.7V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in *Figure 13.*
7. $\overline{WC}$=0 set up time condition to enable the execution of a WRITE command.
8. $\overline{WC}$=0 hold time condition to enable the execution of a WRITE command.
9. The previous M24C64 device (identified by process letter P) offers t_{NS} = 100 ns (max), while the current M24C64 device offers t_{NS} = 80 ns (max). Both products offer a safe margin compared to the 50 ns minimum value recommended by the I^2C specification.

Table 17. 1 MHz AC characteristics

Symbol	Alt.	Parameter[1]	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	500	-	ns
t_{XH1XH2}	t_R	Input signal rise time	(2)	(2)	ns
t_{XL1XL2}	t_F	Input signal fall time	(2)	(2)	ns
t_{QL1QL2}[3]	t_F	SDA (out) fall time	20[4]	120	ns
t_{DXCX}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}[5]	t_{DH}	Data out hold time	100	-	ns
t_{CLQV}[6]	t_{AA}	Clock low to next data valid (access time)	-	450	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_{WLDL}[7][3]	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	µs
t_{DHWH}[8][3]	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	µs
t_W	t_{WR}	Write time	-	5	ms
t_{NS}[3]		Pulse width ignored (input filter on SCL and SDA)	-	80	ns

1. Only for M24C64 devices identified by the process letter K.
2. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be less than 120 ns when f_C < 1 MHz.
3. Characterized only, not tested in production.
4. With C_L = 10 pF.
5. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
6. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that the Rbus × Cbus time constant is within the values specified in *Figure 14*.
7. $\overline{WC}$=0 set up time condition to enable the execution of a WRITE command.
8. $\overline{WC}$=0 hold time condition to enable the execution of a WRITE command.

Figure 13. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 400 kHz

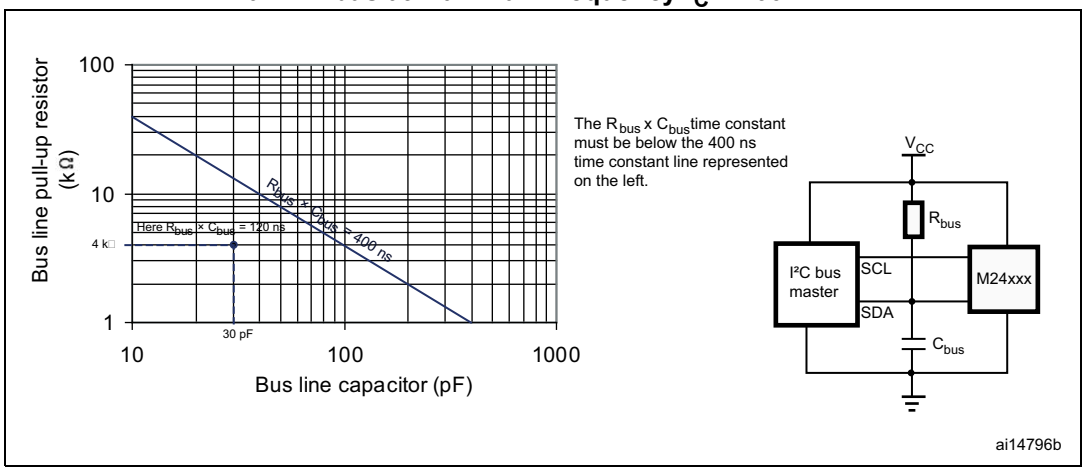


Figure 14. Maximum R_{bus} value versus bus parasitic capacitance C_{bus}) for an I^2C bus at maximum frequency f_C = 1MHz

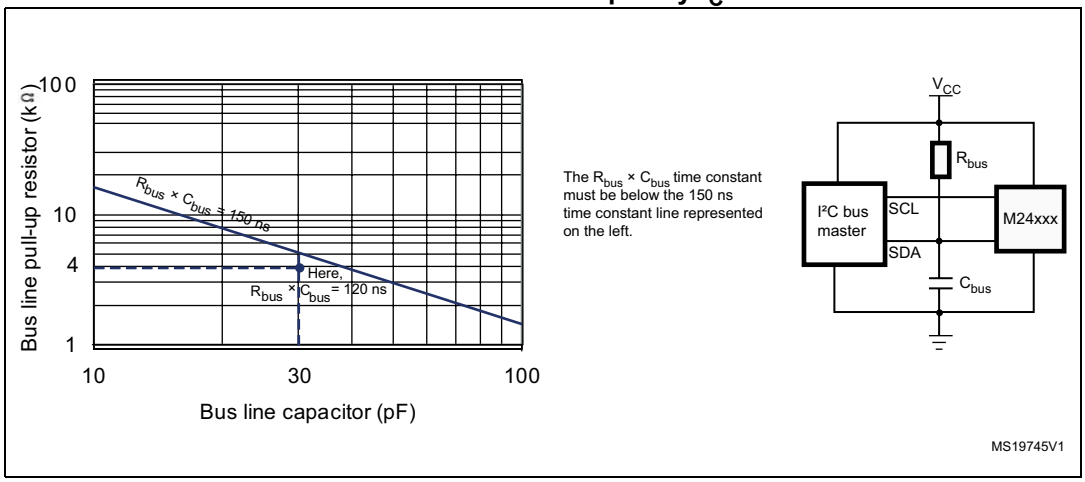
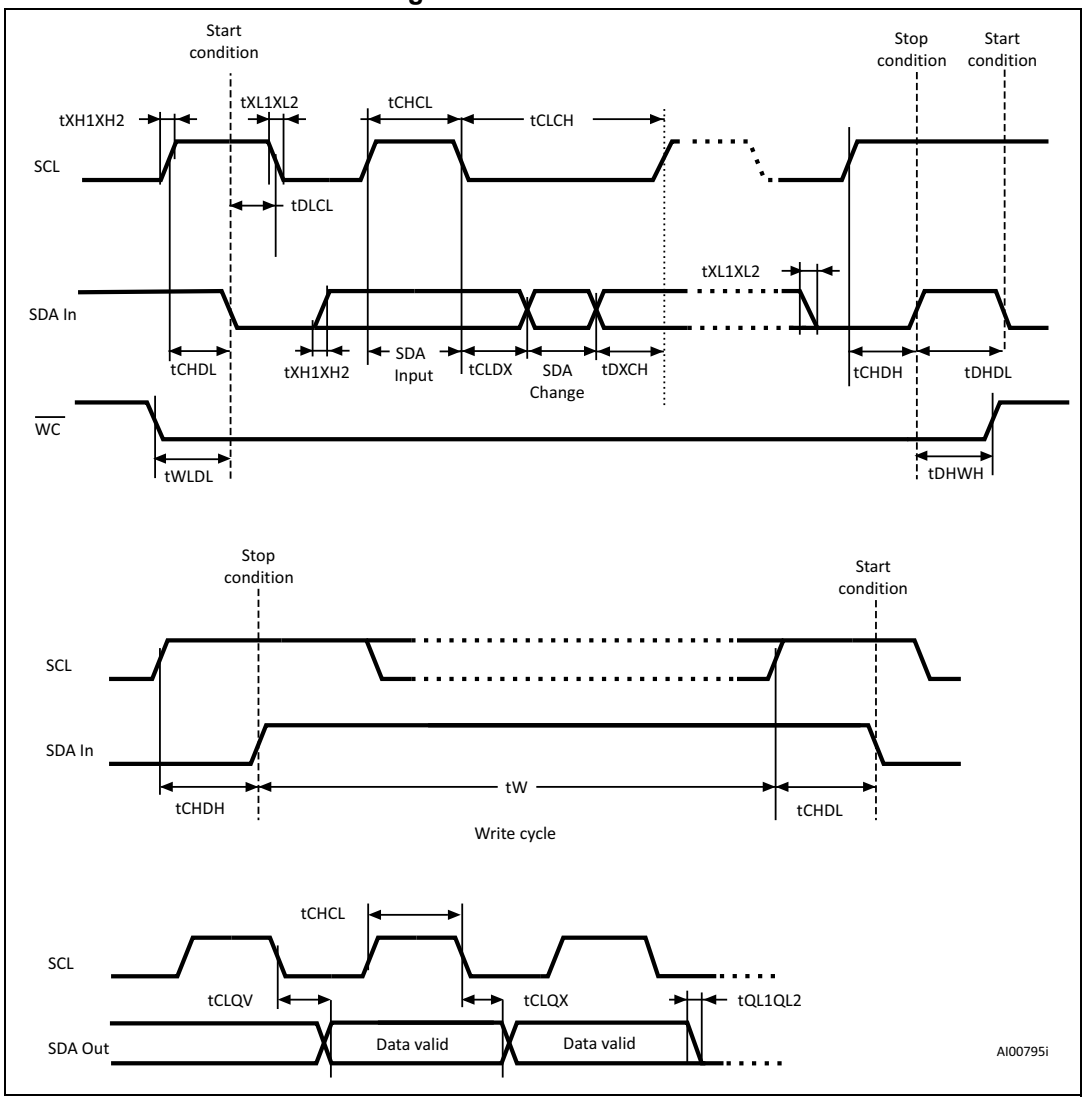


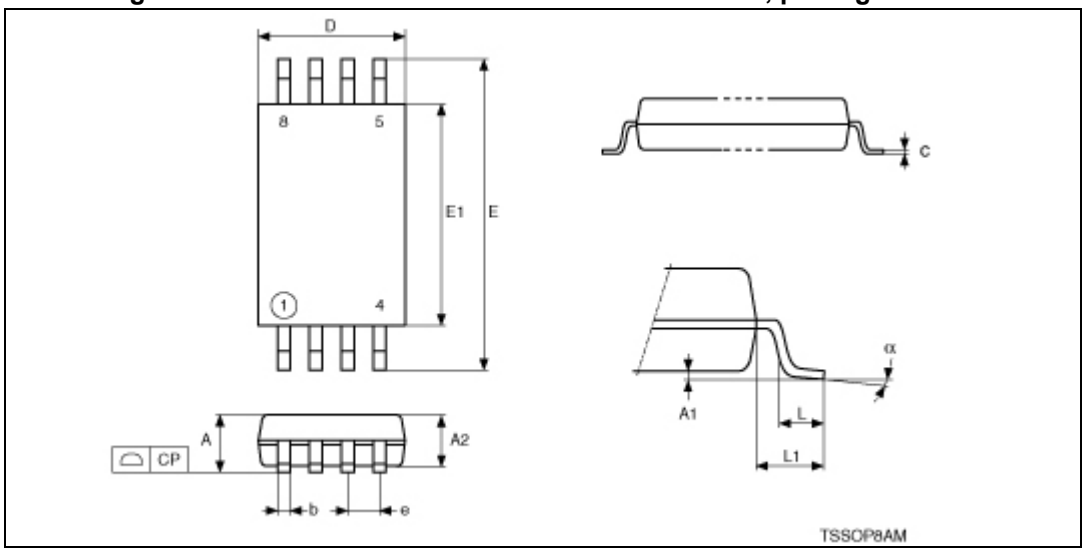
Figure 15. AC waveforms



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 16. TSSOP8 – 8-lead thin shrink small outline, package outline



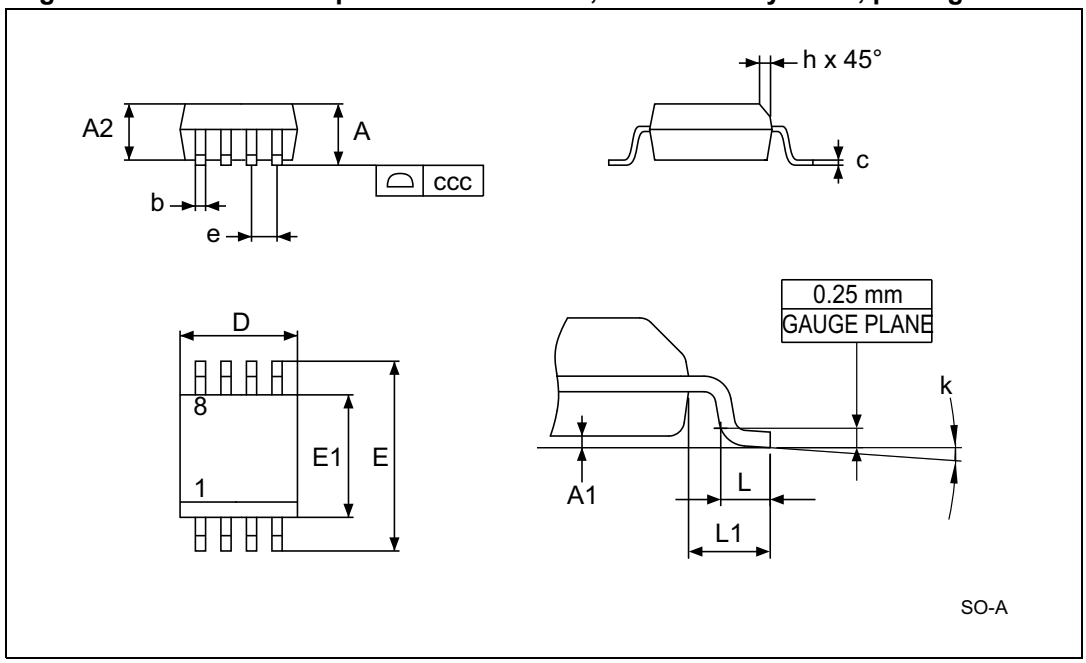
1. Drawing is not to scale.

Table 18. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	–	–	1.200	–	–	0.0472
A1	–	0.050	0.150	–	0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b	–	0.190	0.300	–	0.0075	0.0118
c	–	0.090	0.200	–	0.0035	0.0079
CP	–	–	0.100	–	–	0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000	–	–	0.0394	–	–
α	–	0°	8°	–	0°	8°

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 17. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



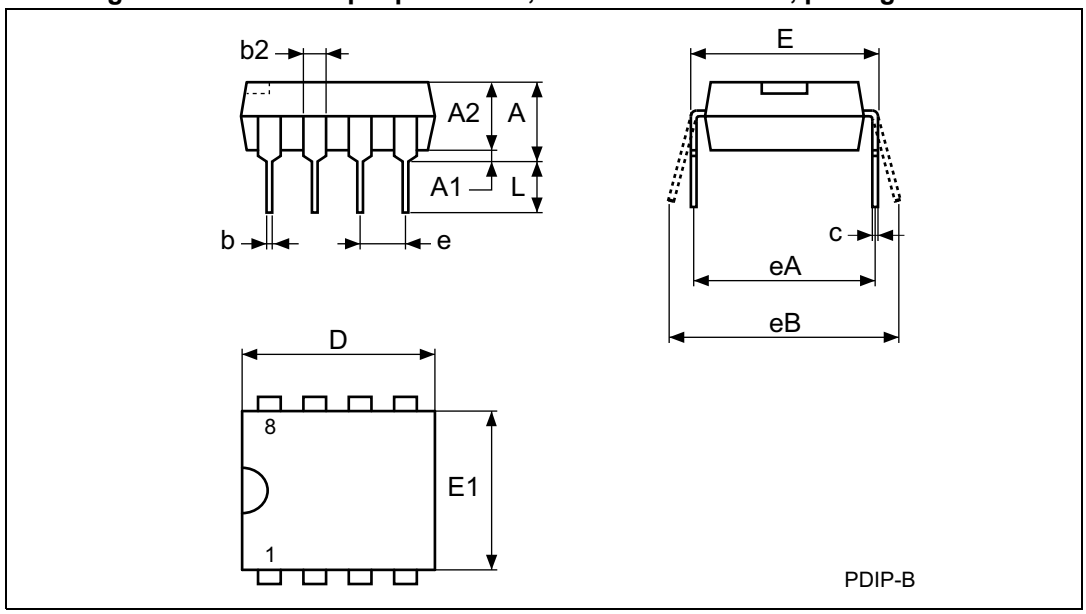
1. Drawing is not to scale.

Table 19. SO8N – 8-lead plastic small outline, 150 mils body width, package data

Symbol	millimeters			inches [1]		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.750	–	–	0.0689
A1	–	0.100	0.250	–	0.0039	0.0098
A2	–	1.250	–	–	0.0492	–
b	–	0.280	0.480	–	0.0110	0.0189
c	–	0.170	0.230	–	0.0067	0.0091
ccc	–	–	0.100	–	–	0.0039
D	4.900	4.800	5.000	0.1929	0.1890	0.1969
E	6.000	5.800	6.200	0.2362	0.2283	0.2441
E1	3.900	3.800	4.000	0.1535	0.1496	0.1575
e	1.270	–	–	0.0500	–	–
h	–	0.250	0.500	–	0.0098	0.0197
k	–	0°	8°	–	0°	8°
L	–	0.400	1.270	–	0.0157	0.0500
L1	1.040	–	–	0.0409	–	–

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 18. PDIP8 – 8-pin plastic DIP, 0.25 mm lead frame, package outline



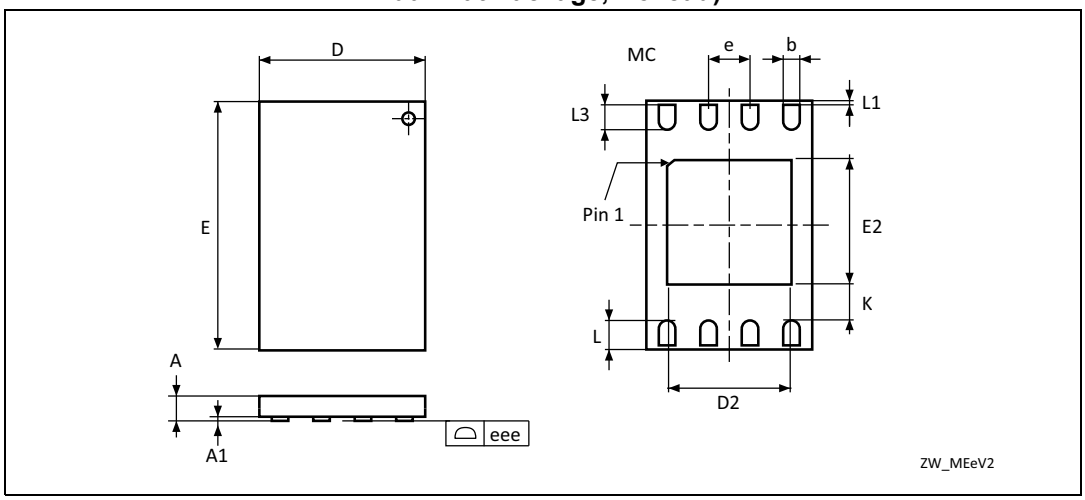
1. Drawing is not to scale.

Table 20. PDIP8 – 8-pin plastic DIP, 0.25 mm lead frame, package mechanical data

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	–	–	5.33	–	–	0.2098
A1	–	0.38	–	–	0.0150	–
A2	3.30	2.92	4.95	0.1299	0.1150	0.1949
b	0.46	0.36	0.56	0.0181	0.0142	0.0220
b2	1.52	1.14	1.78	0.0598	0.0449	0.0701
c	0.25	0.20	0.36	0.0098	0.0079	0.0142
D	9.27	9.02	10.16	0.3650	0.3551	0.4000
E	7.87	7.62	8.26	0.3098	0.3000	0.3252
E1	6.35	6.10	7.11	0.2500	0.2402	0.2799
e	2.54	–	–	0.1000	–	–
eA	7.62	–	–	0.3000	–	–
eB	–	–	10.92	–	–	0.4299
L	3.30	2.92	3.81	0.1299	0.1150	0.1500

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 19. UFDFPN8 (MLP8) – package outline (UFDFPN: Ultra thin Fine pitch Dual Flat Package, No lead)



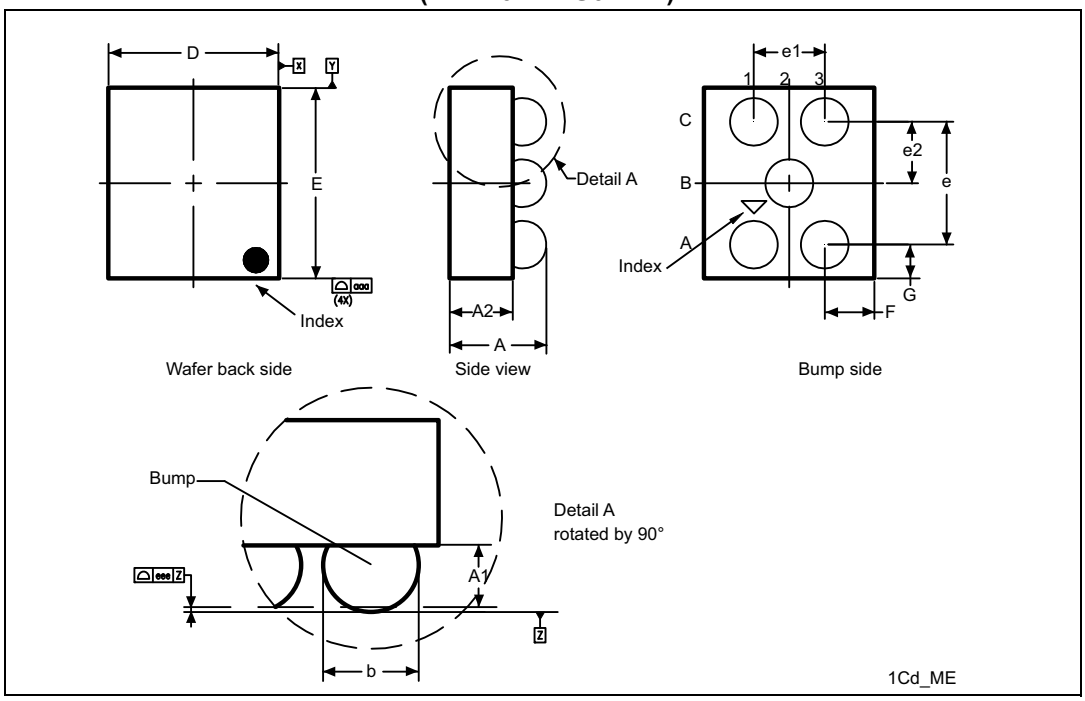
1. Drawing is not to scale.
2. The central pad (area E2 by D2 in the above illustration) is internally pulled to V_{SS}. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 21. UFDFPN8 (MLP8) – package dimensions (UFDFPN: Ultra thin Fine pitch Dual Flat Package, No lead)

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MC)	–	1.200	1.600	–	0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MC)	–	1.200	1.600	–	0.0472	0.0630
e	0.500	–	–	0.0197	–	–
K (rev MC)	–	0.300	–	–	0.0118	–
L	–	0.300	0.500	–	0.0118	0.0197
L1	–	–	0.150	–	–	0.0059
L3	–	0.300	–	–	0.0118	–
eee[2]	–	0.080	–	–	0.0031	–

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

Figure 20. WLCSP 5-bump wafer-length chip-scale package outline (M24C64-FCS6TP/K)



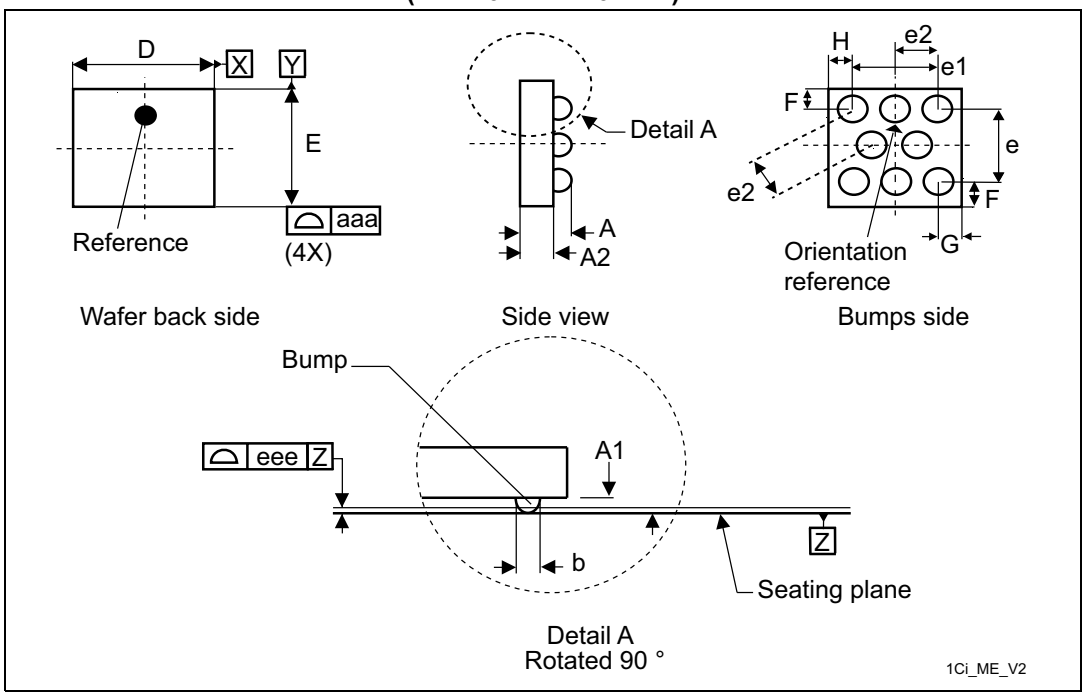
1. Drawing is not to scale.
2. The index on the wafer back side (circle) is above the index of the bump side (triangle/arrow).

Table 22. WLCSP 5-bump wafer-length chip-scale package mechanical data (M24C64-FCS6TP/K)

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.545	0.490	0.600	0.0215	0.0193	0.0236
A1	0.190			0.0075		
A2	0.355			0.0140		
b[2]	0.270			0.0106		
D	0.959		1.074	0.0378		0.0423
E	1.073		1.168	0.0422		0.0460
e	0.693			0.0273		
e1	0.400			0.0157		
e2	0.3465			0.0136		
F	0.280			0.0110		
G	0.190			0.0075		
aaa	0.110					0.0043
eee	0.060					0.0024

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension measured at the maximum bump diameter parallel to primary datum Z.

Figure 21. Thin WLCSP 8-bump wafer-length chip-scale package outline (M24C64-DFCT6TP/K)



1. Drawing is not to scale.
2. The index on the wafer back side (circle) is above the index of the bump side (triangle/arrow).

Table 23. Thin WLCSP 8-bump wafer-length chip-scale package mechanical data (M24C64-DFCT6TP/K)

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.315	0.300	0.330	0.0124	0.0118	0.0130
A1	0.115			0.0045		
A2	0.200			0.0079		
b[2]	0.160			0.0063		
D	1.073		1.093	0.0422		0.0430
E	0.959		0.979	0.0378		0.0385
e	0.693			0.0273		
e1	0.800			0.0315		
e2	0.400			0.0157		
F	0.133			0.0052		
G	0.137			0.00524		
aaa	0.110			0.0043		
eee	0.060			0.0043		

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension measured at the maximum bump diameter parallel to primary datum Z.

10 Part numbering

Table 24. Ordering information scheme

Example: M24C64 - D W MN 6 T P /P

Device type

M24 = I^2C serial access EEPROM

Device function

C64 = 64 Kbit (8192 x 8)

Device family

Blank = Without Identification page

D = With additional Identification page

Operating voltage

W = V_{CC} = 2.5 V to 5.5 V

R = V_{CC} = 1.8 V to 5.5 V

F = V_{CC} = 1.7 V to 5.5 V

Package

BN = PDIP8(1)

MN = SO8 (150 mil width)(2)

DW = TSSOP8 (169 mil width)

MC = UFDFPN8 (MLP8)(2)

CS = 5-bump WLCSP(2)

CT = 8-bump WLCSP(2)

Device grade

6 = Industrial: device tested with standard test flow over –40 to 85 °C

Option

blank = standard packing

T = Tape and reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

Process(3)

/P or /K = Manufacturing technology code

1. RoHS-compliant (ECOPACK1®)
2. RoHS-compliant and halogen-free (ECOPACK2®)
3. The process letters appear on the device package (marking) and on the shipment box. Please contact your nearest ST Sales Office for further information.

11 Revision history

Table 25. Document revision history

Date	Revision	Changes
14-Mar-2011	22	Updated information concerning E2, E1, E0 for the WLCSP package: – note under *Figure 3: 5-bump WLCSP connections (top view)* – comment under *Figure 5: Device select code* – note 3 under *Table 2: Device select code*
07-Apr-2011	23	Updated MLP8 package data and *Section Figure 56.: WLCSP 5 bumps package outline*. Added footnote (a) in *Section 4.5: Memory addressing*.
18-May-2011	24	Updated: – *Figure 3: 5-bump WLCSP connections (top view)* – *Table 5: Absolute maximum ratings* – *Small text changes* Added: – *Figure 12: Memory cell characteristics*
08-Sep-2011	25	Updated: – *Table 21: UFDFPN8 (MLP8) – package dimensions (UFDFPN: Ultra thin Fine pitch Dual Flat Package, No lead)* – *Figure 14: Maximum R_{bus} value versus bus parasitic capacitance C_{bus}) for an I^2C bus at maximum frequency f_C = 1MHz* – *Figure 6: I2C Fast mode Plus (fC = 1 MHz): maximum Rbus value versus bus parasitic capacitance (Cbus)*. Added t_{WLDL} and t_{DHWH} in: – *Table 16: 400 kHz AC characteristics* – *Table 17: 1 MHz AC characteristics* – *Figure :* Minor text changes.
16-Dec-2011	26	Updated A dimension in *Table 22: WLCSP 5-bump wafer-length chip-scale package mechanical data (M24C64-FCS6TP/K)*.

Table 25. Document revision history (continued)

Date	Revision	Changes
28-Aug-2012	27	Datasheet split into: – M24C64-DF, M24C64-W, M24C64-R,M24C64-F (this datasheet) for standard products (range 6), – M24C64-125 datasheet for automotive products (range 3). Added 8-bump thin WLCSP. Updated single supply voltage and number of Write cycles on cover page. Updated *Section 2.1: Serial Clock (SCL)* and *Section 2.2: Serial Data (SDA)*. Updated *Figure 6: Block diagram*. Added *Section 4.5: Device addressing*. *Section 5.1: Write operations* move to *Section 5: Instructions* and updated. Moved *Figure 8: Write mode sequences with WC = 0 (data write enabled)* to *Section 5.1.1: Byte Write*. *Section 5.1.2: Page Write*: changed address bits to A15/A5 and updated *Figure 9*. Case of locked Write identification Page removed from *Section 5.1.4: Lock Identification Page (M24C64-D only)*. Updated *Section 5.1.5: ECC (Error Correction Code) and Write cycling* and move *Figure 10: Write cycle polling flowchart using ACK* to *Section 5.1.6: Minimizing Write delays by polling on ACK*. Added note 1 in *Table 6: Operating conditions (voltage range W)* and *Table 7: Operating conditions (voltage range R)*. Added *Table 11: Cycling performance by groups of four bytes* and updated *Table 12: Memory cell data retention*. Removed note 2 in *Table 16: 400 kHz AC characteristics* for t_{QL1QL2}, t_{WLDL}, t_{DHWH}, and t_{NS}. *Table 24: Ordering information scheme*: removed ambient operating temperature for device grade 5 and added Note *2.* to MLP8 and WLCSP packages.
18-Nov-2013	28	Added text in *Chapter 5.2.2: Current Address Read* Updated note (1) under *Table 5: Absolute maximum ratings*. Removed note (3) in *Table 2: Device select code*. Updated notes below *Table 13: DC characteristics (M24C64-W, device grade 6)* and *Table 14: DC characteristics (M24C64-R, device grade 6)* Renamed *Figure 19* and *Table 21*. Updated captions above *Figure 20* and *Figure 21*.

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Document Revision History

Date	Rev.	Description of the Revision
July 02, 2014	1.00	First draft creation

Source Documents & Reference Documents

Source document Title	**Rev.:**	**Date:**

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