ESD103-B1-02ELS

Bi-directional ESD protection device, 15 V, 0.09 pF, 0201

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Product description

ESD protection device with a bi-directional symmetric I/V characteristic and excellent clamping performance, extremely low capacitance and high linearity for mobile device antenna.

Feature list

- ESD/transient protection according to:
  - IEC61000-4-2 (ESD): ±14 kV (air) / ±10 kV (contact)
- Bi-directional maximum working voltage: V_{WM} = ±15 V
- Line capacitance: C_L = 0.09 pF at f = 1 GHz
- Clamping voltage: V_{cl} = 48 V at I_{TLP} = 16 A with R_{dyn} = 1.8 Ω
- Very low leakage current: I_L = 0.1 nA
- Small form factor SMD size, low profile (0.62 x 0.32 x 0.31 mm^3)

Potential applications

- RF antennas and interfaces (LTE, WLAN)

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Device information

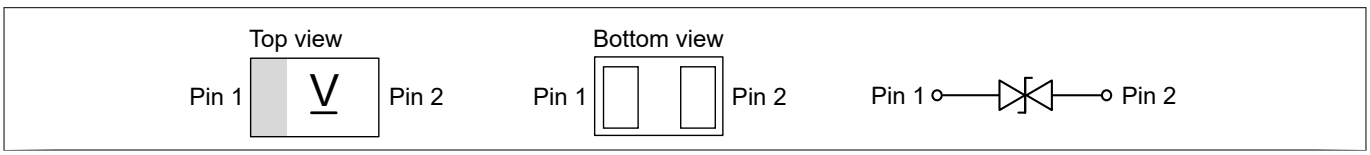

Figure 1 **Pin configuration and schematic diagram**

Table 1 **Part information**

Product name / Ordering code	Package	Pin configuration	Marking	Pieces / Reel
ESD103-B1-02ELS/ESD103B102ELSE6327XTSA1	TSSLP-2-4	1 line, bi-directional	V	15 k

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1 Absolute maximum ratings

Table 2 Absolute maximum ratings at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
Working voltage	V_{WM}	-15	+15	V	
ESD discharge voltage	V_{ESD} (contact)	-10	+10	kV	Discharge network: R = 330 Ω, C = 150 pF [1)]
	V_{ESD} (air)	-14	+14		
Operating temperature	T_{op}	-55	+125	°C	
Storage temperature	T_{stg}	-65	+150		

Attention**: **Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.

1 Based on IEC61000-4-2.

2 Electrical characteristics

Note: *T_A = 25°C, unless otherwise specified. Device is electrically symmetrical.*

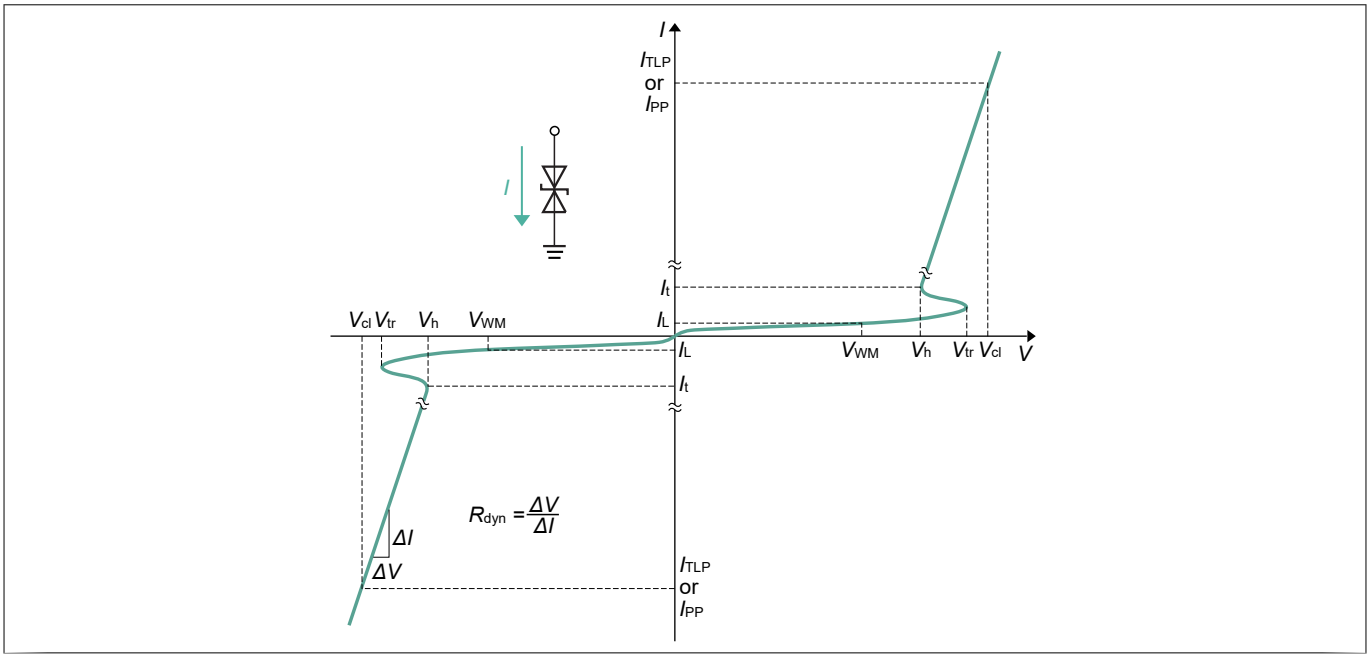

Figure 2 ***I/V* characteristic curve**

Table 3 ***I/V* characteristic parameters**

Symbol	Parameter
I_h	Holding current
I_L	Leakage current
I_{PP}	Peak pulse current, based on IEC61000-4-5
I_t	Test current
I_{TLP}	TLP current
R_{dyn}	Dynamic resistance
V_{cl}	Clamping voltage
V_h	Holding voltage
V_t	Test voltage
V_{tr}	Trigger voltage
V_{WM}	Maximum working voltage

2 Electrical characteristics

Table 4 DC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Trigger voltage [2]	V_{tr}	-	21	-	V	
eakage current	I_L	-	0.1	50	nA	V_{WM} = 15 V

Table 5 AC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line capacitance	C_L	-	0.13	0.2	pF	V = 0 V, f = 1 MHz
		-	0.09	-		V = 0 V, f = 1 GHz
Series inductance	L_S	-	0.2	-	nH	Extracted from S-parameters

Table 6 Protection characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Clamping voltage (TLP) [3] [4]	V_{cl}	-	20	-	V	I_{TLP} = 1 A
		-	36	-		I_{TLP} = 8 A
		-	48	-		I_{TLP} = 16 A
Dynamic resistance [3]	R_{dyn}	-	1.8	-	Ω	

2 Verified by design.
3 TLP parameters: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns, averaging window 30-60 ns.
4 Refer to application note AN210 [2]

3 Typical characteristic diagrams

Note: $T_A = 25°C$, *unless otherwise specified.*

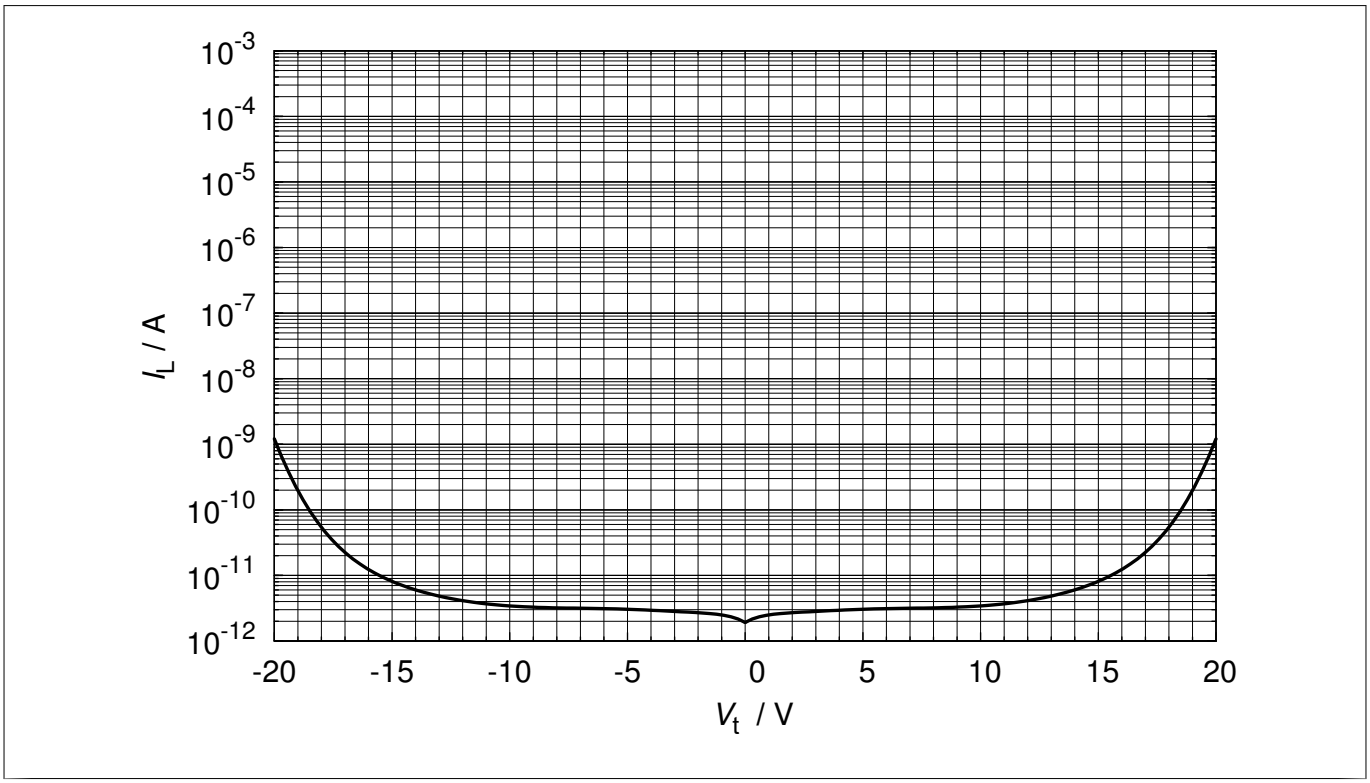

Figure 3 Leakage current $I_L = f(V_t)$

3 Typical characteristic diagrams

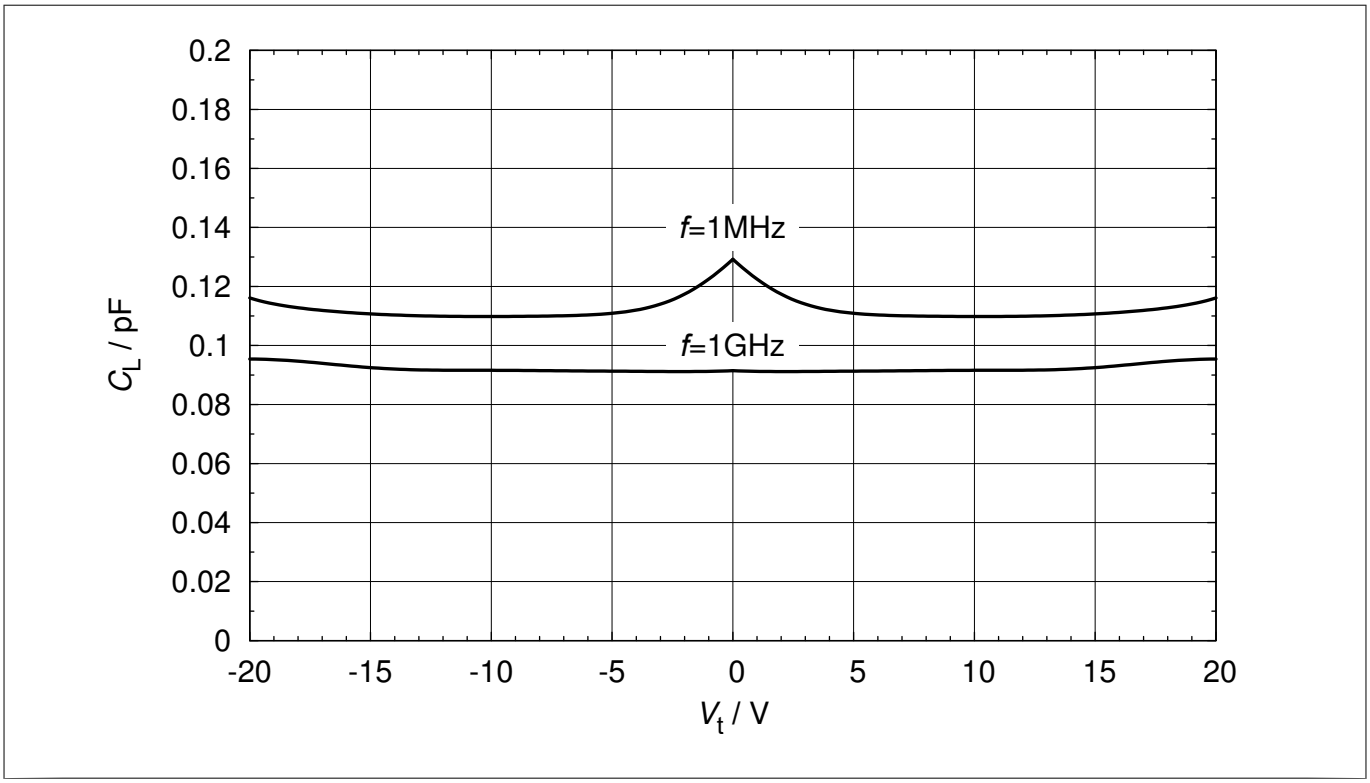

Figure 4 **Line capacitance $C_L = f(V_t)$, $f = 1$ MHz, 1 GHz**

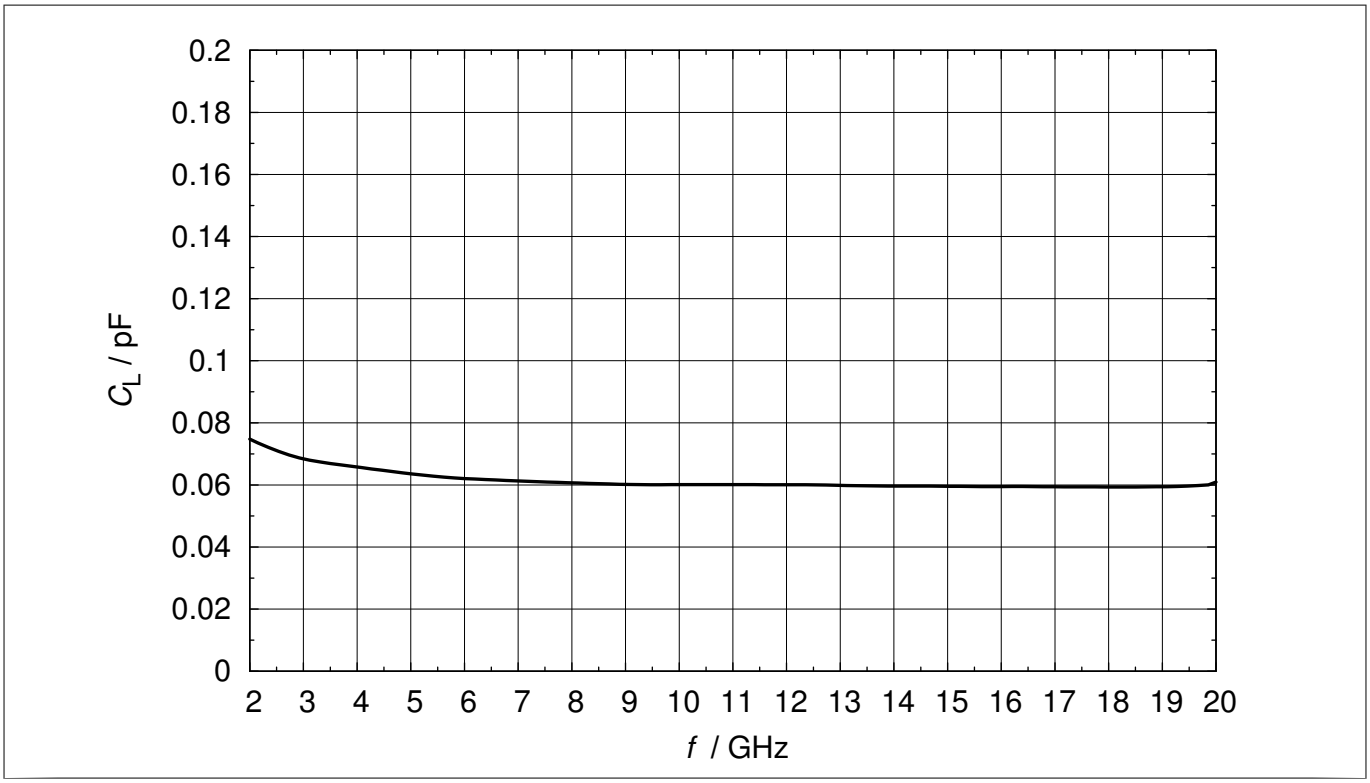

Figure 5 **Line capacitance: $C_L = f(f)$, $V_t = 0$ V**

3 Typical characteristic diagrams

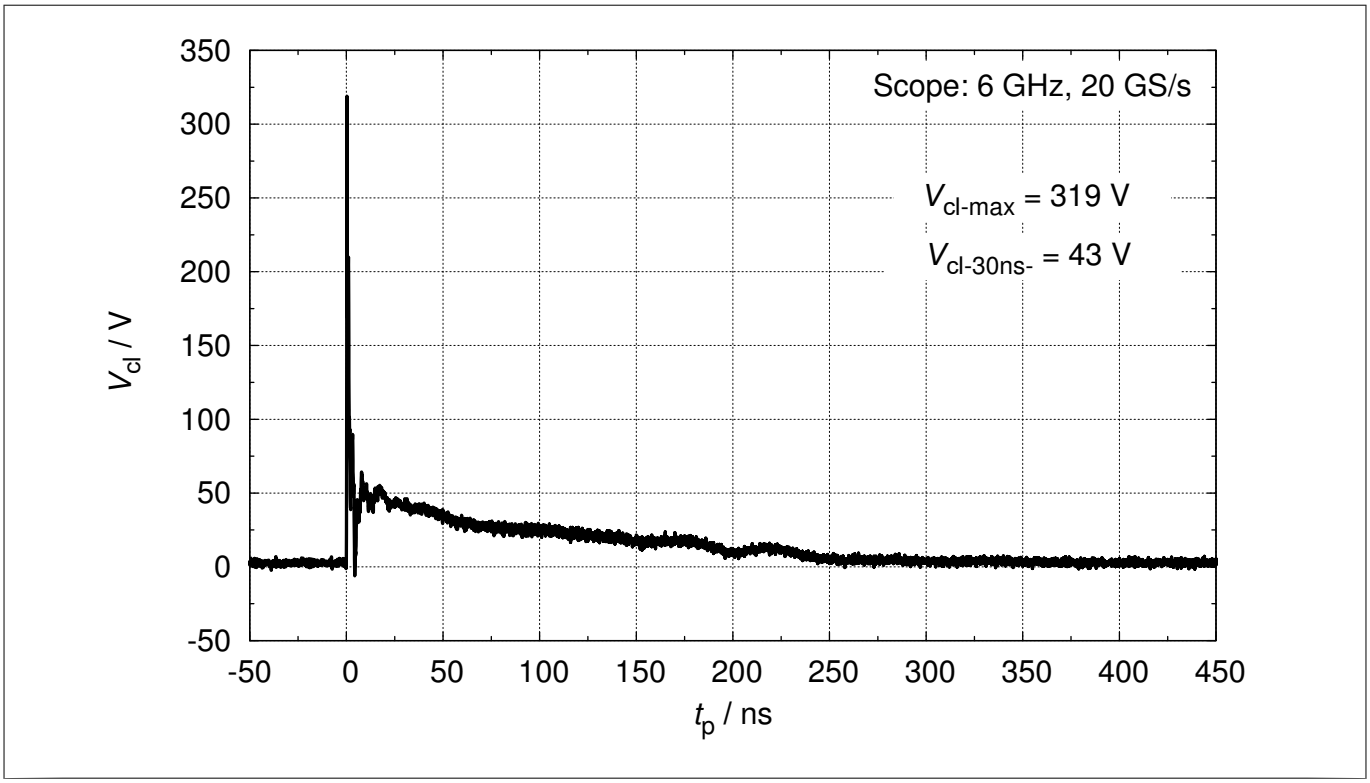

Figure 6 **Clamping voltage (ESD): V_{cl} = f(t_p), 8 kV positive pulse based on IEC61000-4-2**

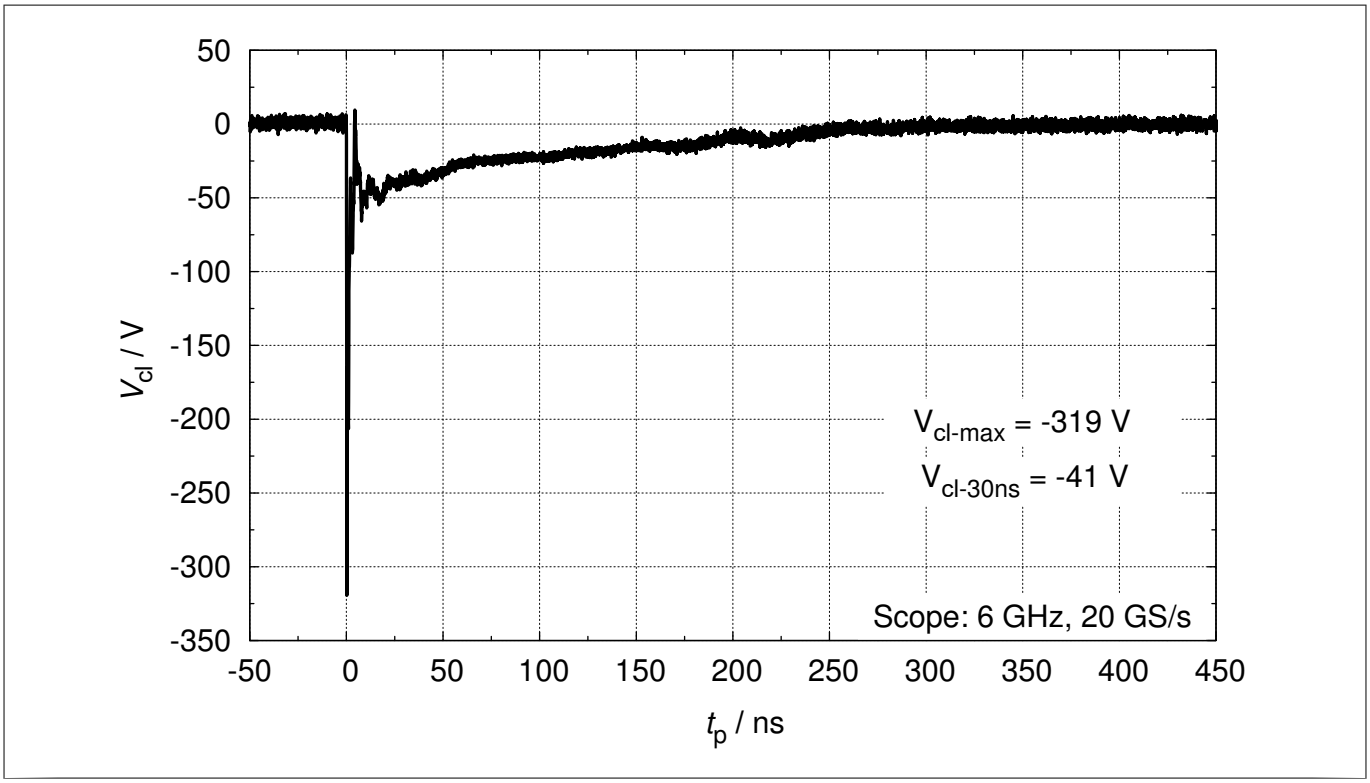

Figure 7 **Clamping voltage (ESD): V_{cl} = f(t_p), 8 kV negative pulse based on IEC61000-4-2**

3 Typical characteristic diagrams

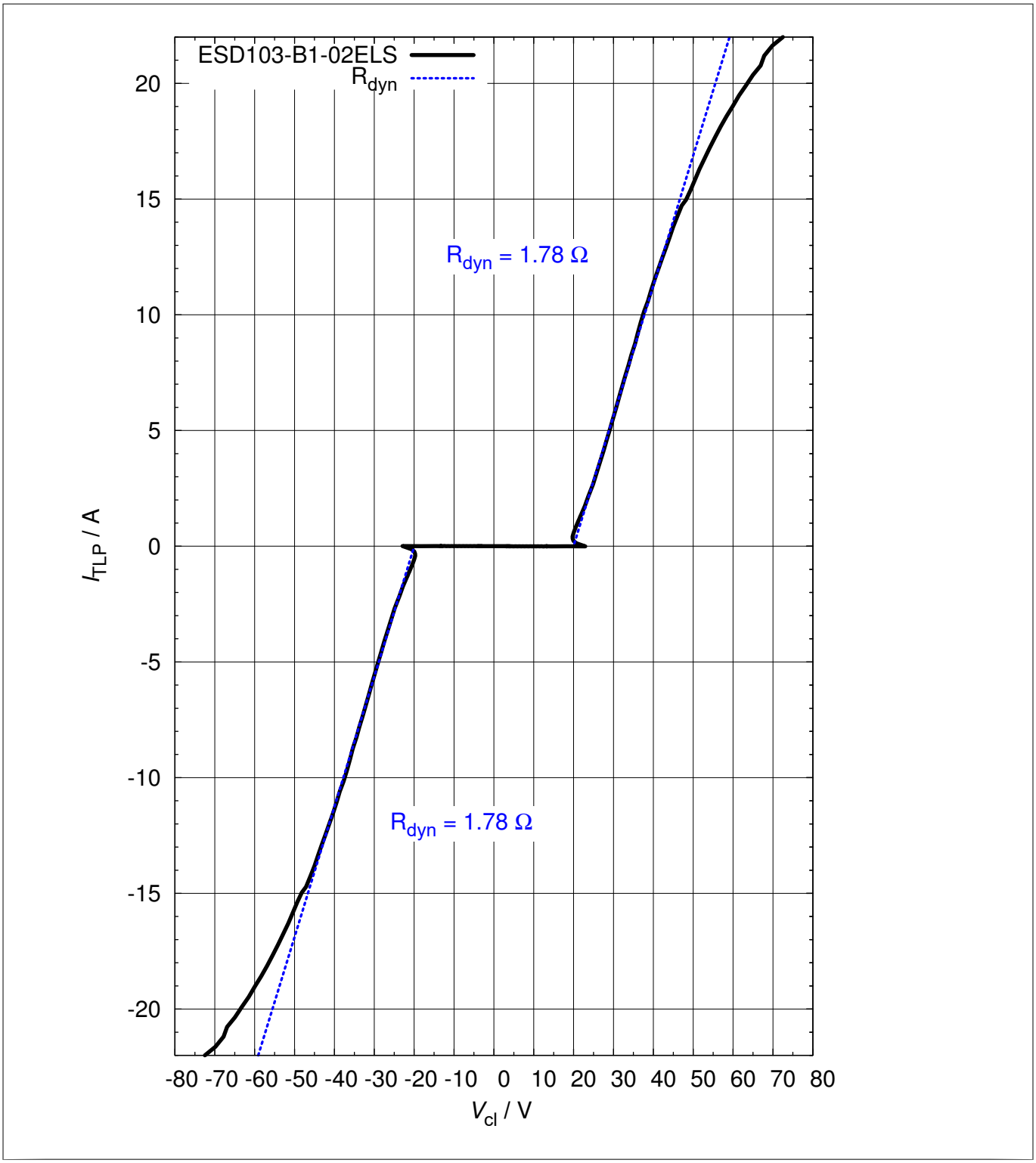

Figure 8 **Clamping voltage (TLP): I_{TLP} = f(V_{cl})**

4 Package information TSSLP-2-4

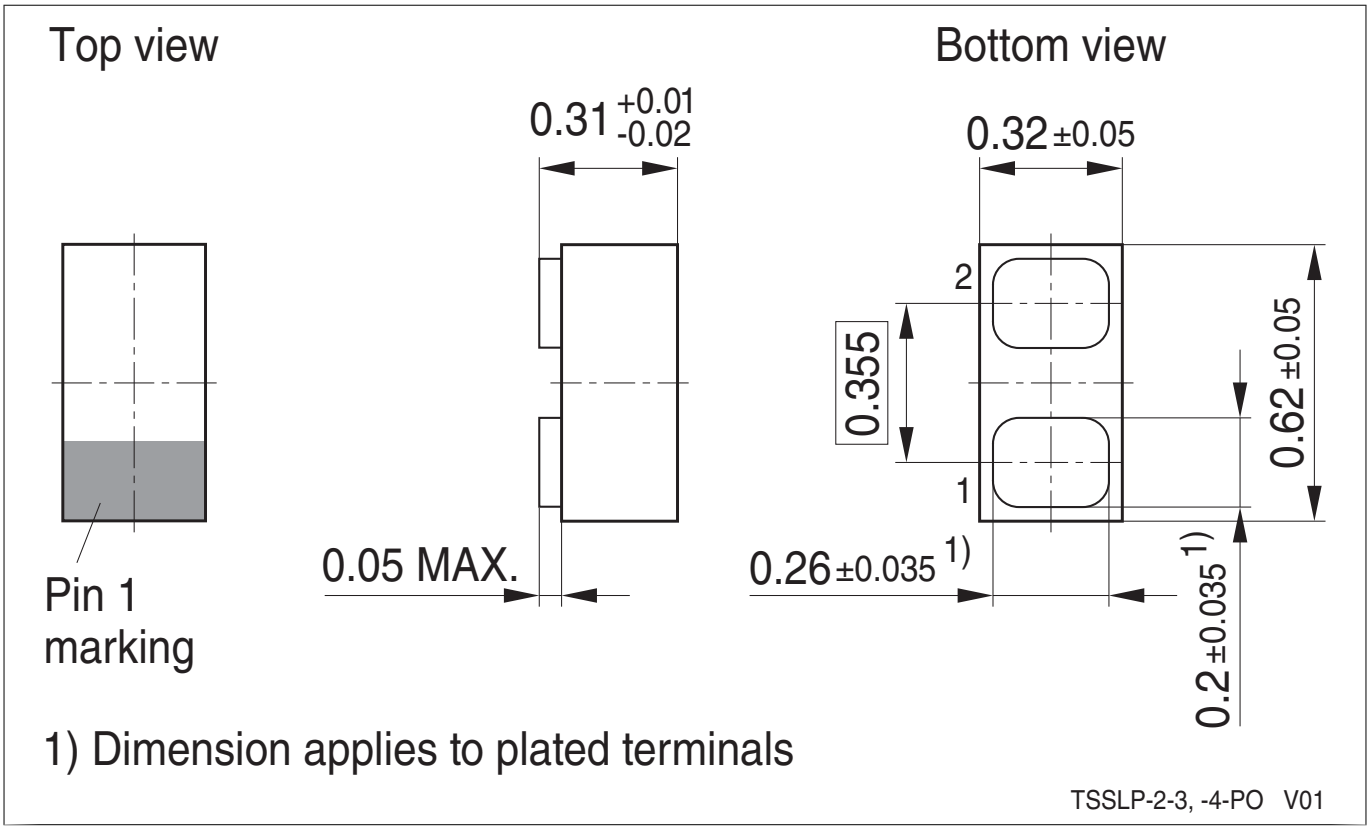

Figure 9 TSSLP-2-4 package

Note: For package information including footprint, packing and assembly recommendation refer to:

https://www.infineon.com/cms/en/product/packages/PG-TSSLP/PG-TSSLP-2-4/

5 References

[1]	Infineon AG - Understanding ESD protection device characteristics
[2]	Infineon AG - **Application note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

6 Revision history

Document version	Date of release	Description of changes
v1.3	2014-06-12	• Table 5 updated
v2.0	2023-02-02	• New datasheet layout

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