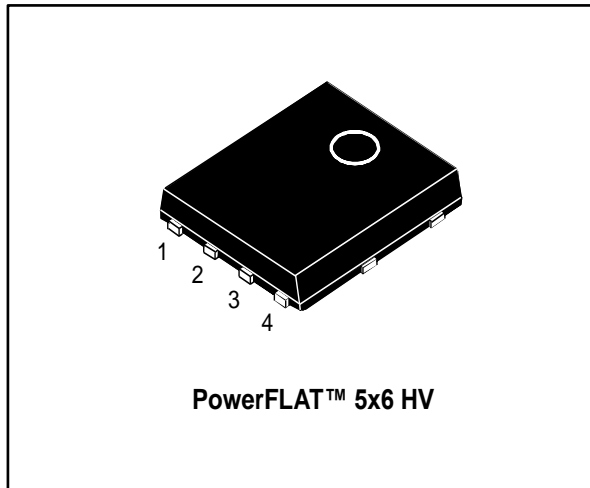
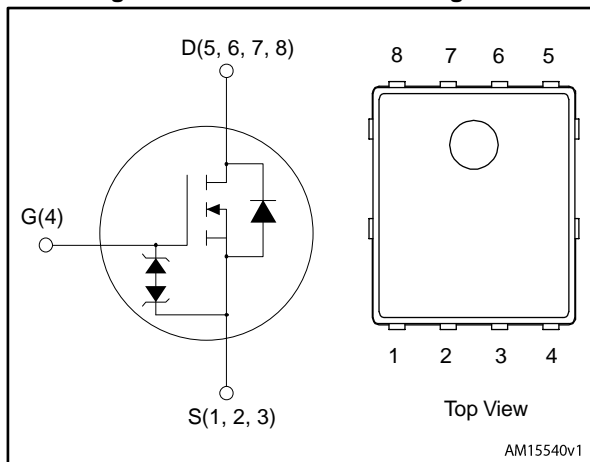


## N-channel 600 V, 0.278 $\Omega$ typ., 9 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data



**Figure 1: Internal schematic diagram**



**Table 1: Device summary**

Order code	Marking	Package	Packing
STL18N60M2	18N60M2	PowerFLAT™ 5x6 HV	Tape and reel

### Features

Order code	V <sub>DS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL18N60M2	650 V	0.308 $\Omega$	9 A

- Extremely low gate charge
- Excellent output capacitance (C<sub>oss</sub>) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>GS</sub>	Gate-source voltage	± 25	V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25 °C	9	A
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 100 °C	5.5	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	36	A
P <sub>TOT</sub> <sup>(2)</sup>	Total dissipation at T <sub>C</sub> = 25 °C	57	W
I <sub>AR</sub>	Avalanche current, repetitive or nonrepetitive (pulse width limited by T <sub>j</sub> max)	2	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	135	mJ
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15	V/ns
dv/dt <sup>(4)</sup>	MOSFET dv/dt ruggedness	50	V/ns
T <sub>stg</sub>	Storage temperature range	- 55 to 150	°C
T <sub>j</sub>	Operating junction temperature range		

**Notes:**

(1)The value is limited by package.

(2)Pulse width limited by safe operating area.

(3) $I_{SD} \leq 9$  A,  $di/dt \leq 400$  A/ $\mu$ s;  $V_{DS(peak)} \leq V_{(BR)DSS}$ ,  $V_{DD} = 400$  V.

(4) $V_{DS} \leq 480$  V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	2.2	°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb	59	°C/W

**Notes:**

(1)When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			10	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4.5\text{ A}$		0.278	0.308	$\Omega$

**Notes:**

<sup>(1)</sup> Defined by design, not subject to production test.

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	791	-	pF
$C_{oss}$	Output capacitance		-	40	-	pF
$C_{rSS}$	Reverse transfer capacitance				1.3	-
$C_{oss\text{ eq.}}^{(1)}$	Output equivalent capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	164.5	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	5.6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 13\text{ A}$ , $V_{GS} = 0\text{ to } 10\text{ V}$ (see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> )	-	21.5	-	nC
$Q_{gs}$	Gate-source charge		-	3.2	-	nC
$Q_{gd}$	Gate-drain charge		-	11.3	-	nC

**Notes:**

<sup>(1)</sup> $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80 %  $V_{DS}$ .

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 6.5\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> )	-	12	-	ns
$t_r$	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off-delay time		-	47	-	ns
$t_f$	Fall time		-	10.6	-	ns

Table 7: Source drain diode

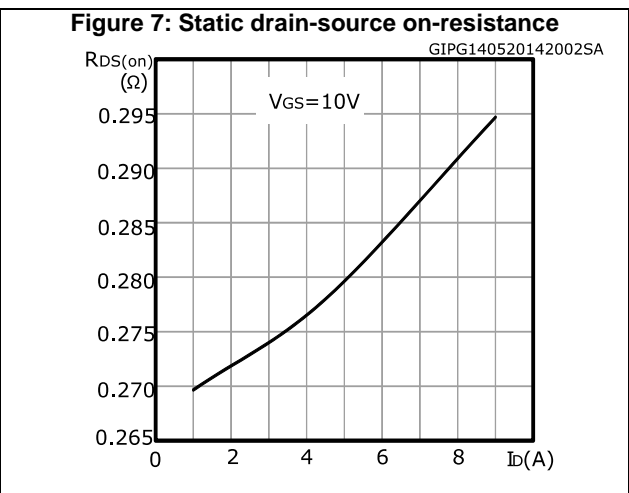
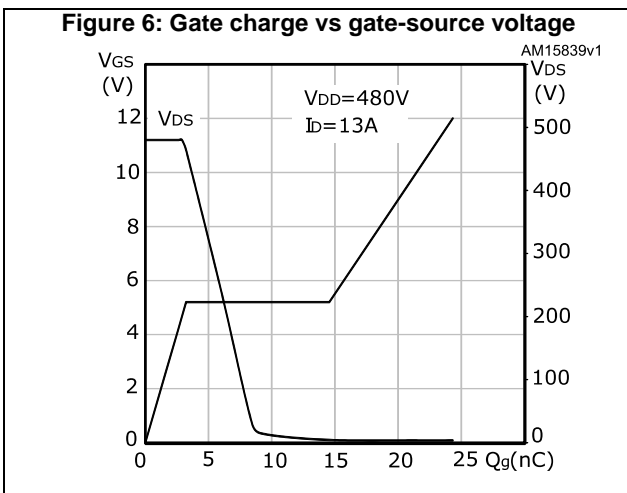
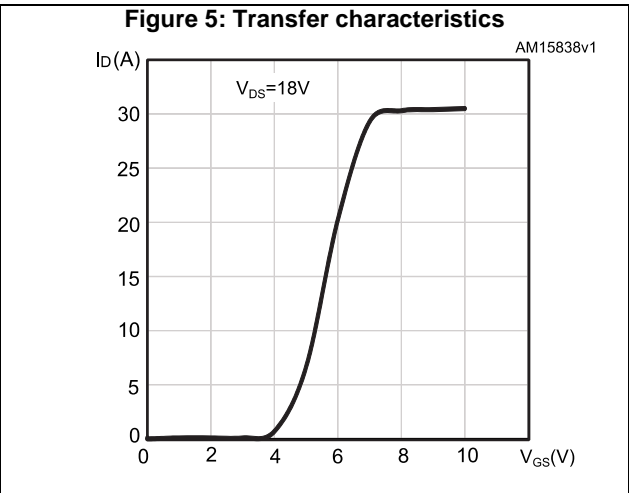
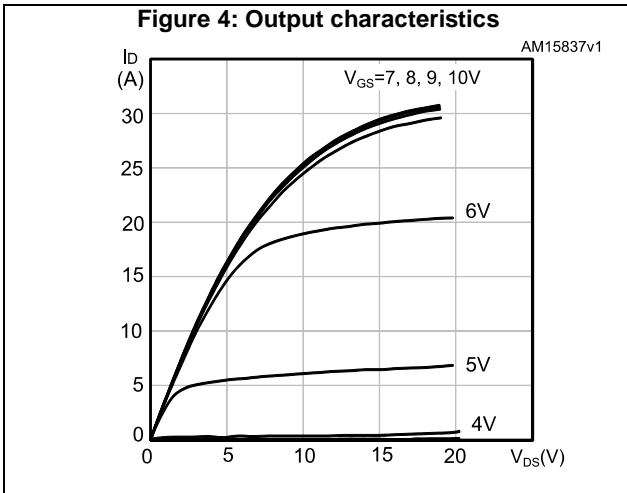
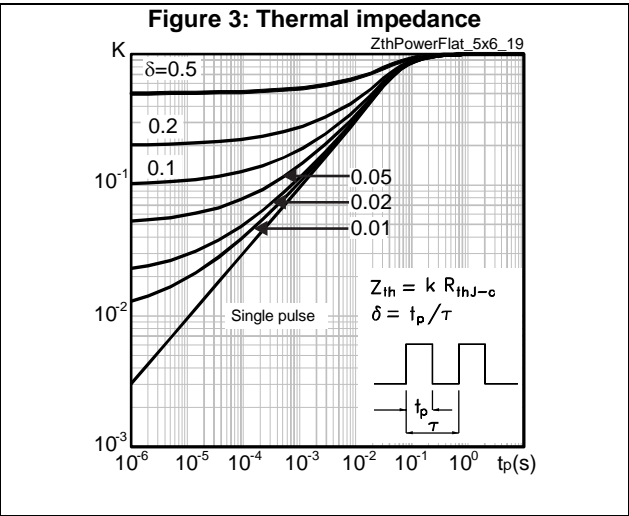
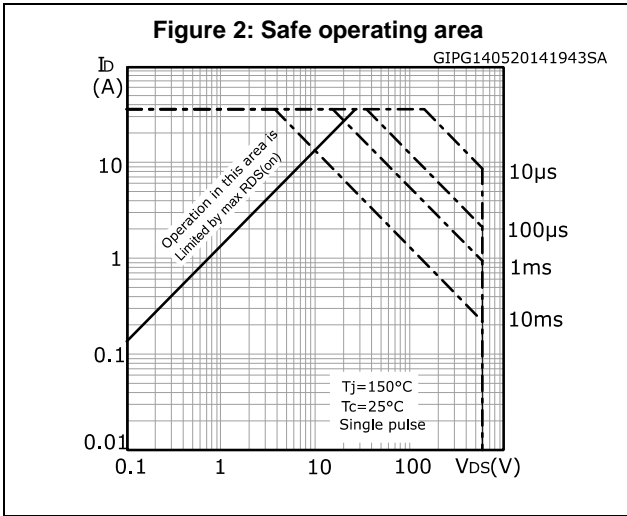
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 13\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 13\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )	-	305		ns
$Q_{rr}$	Reverse recovery charge		-	3.3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	22		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 13\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )	-	417		ns
$Q_{rr}$	Reverse recovery charge		-	4.6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	22.2		A

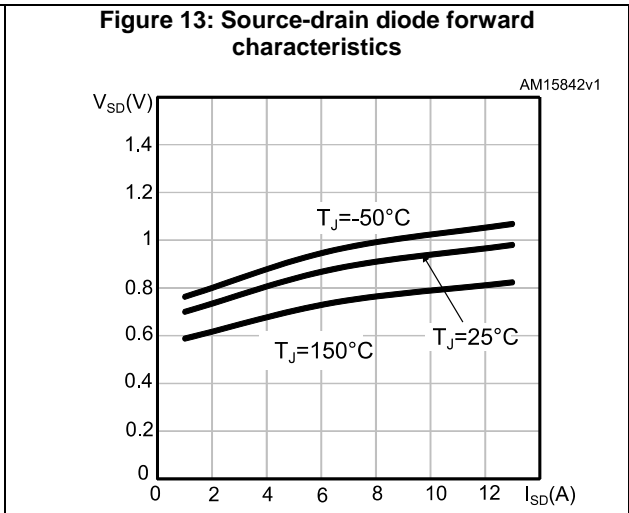
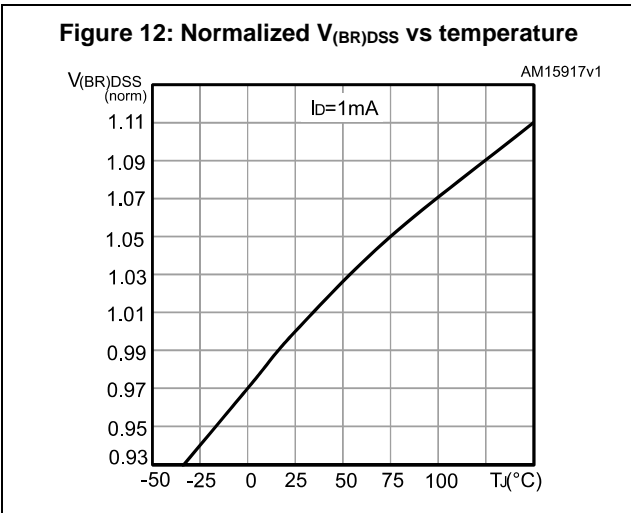
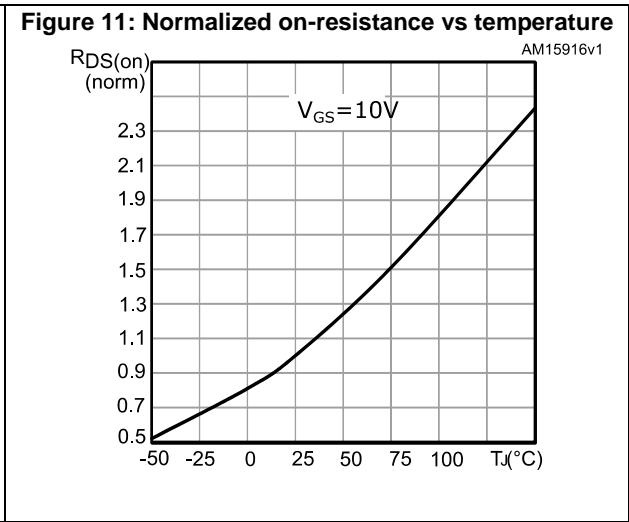
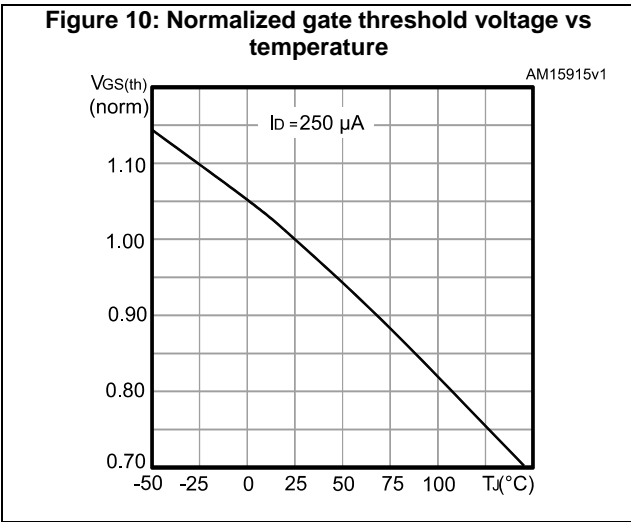
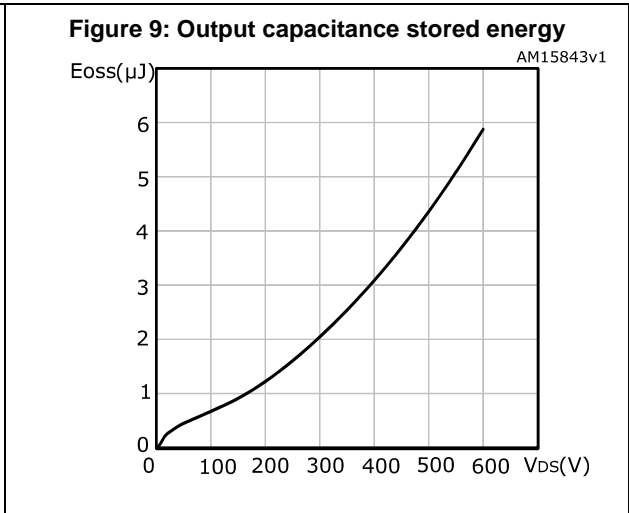
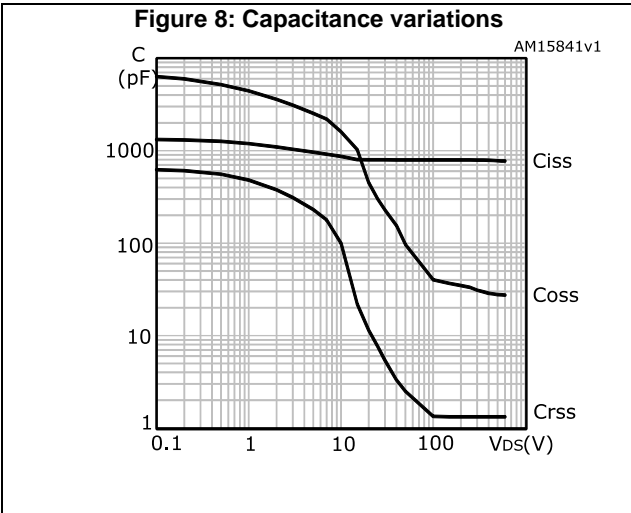
**Notes:**

<sup>(1)</sup>Pulse width is limited by safe operating area.

<sup>(2)</sup>Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

## 2.1 Electrical characteristics (curves)





### 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**



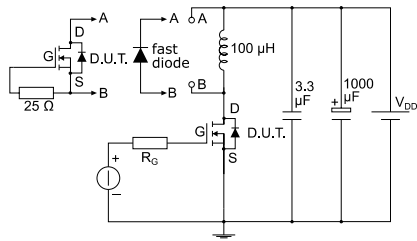
AM01468v1

**Figure 15: Test circuit for gate charge behavior**



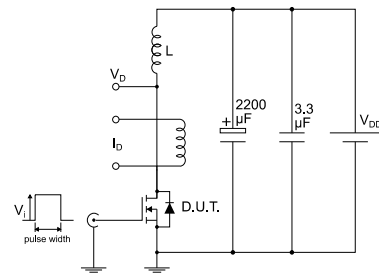
AM01469v1

**Figure 16: Test circuit for inductive load switching and diode recovery times**



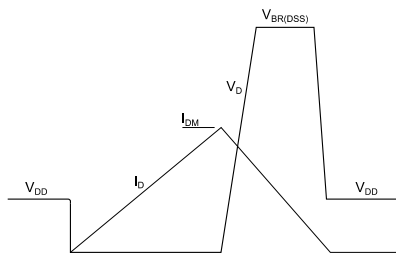
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**Figure 17: Unclamped inductive load test circuit**



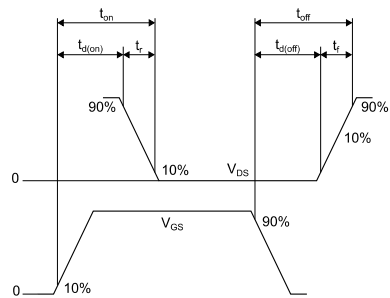
AM01471v1

**Figure 18: Unclamped inductive waveform**



AM01472v1

**Figure 19: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 5x6 HV package information

Figure 20: PowerFLAT™ 5x6 HV package outline

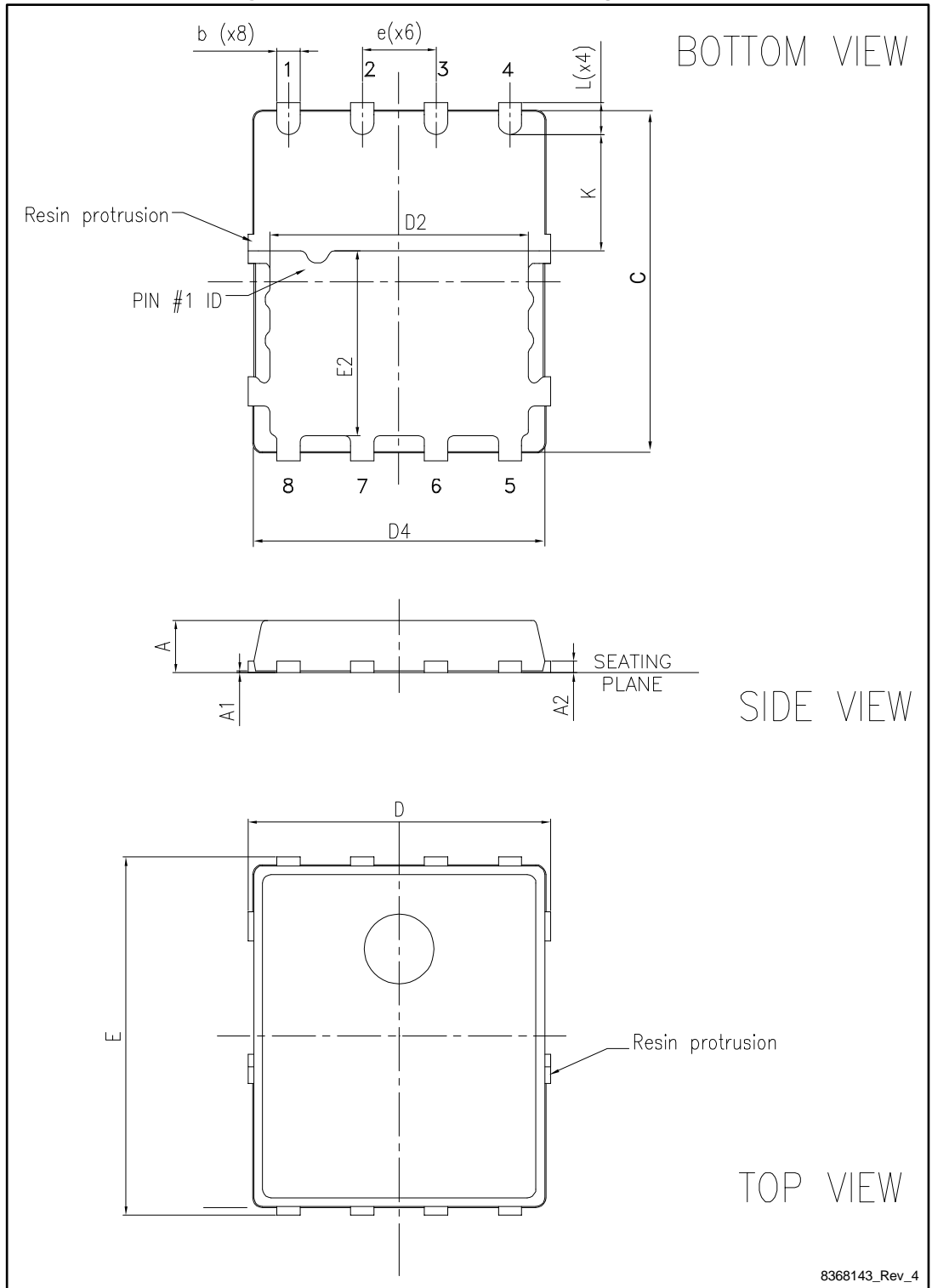
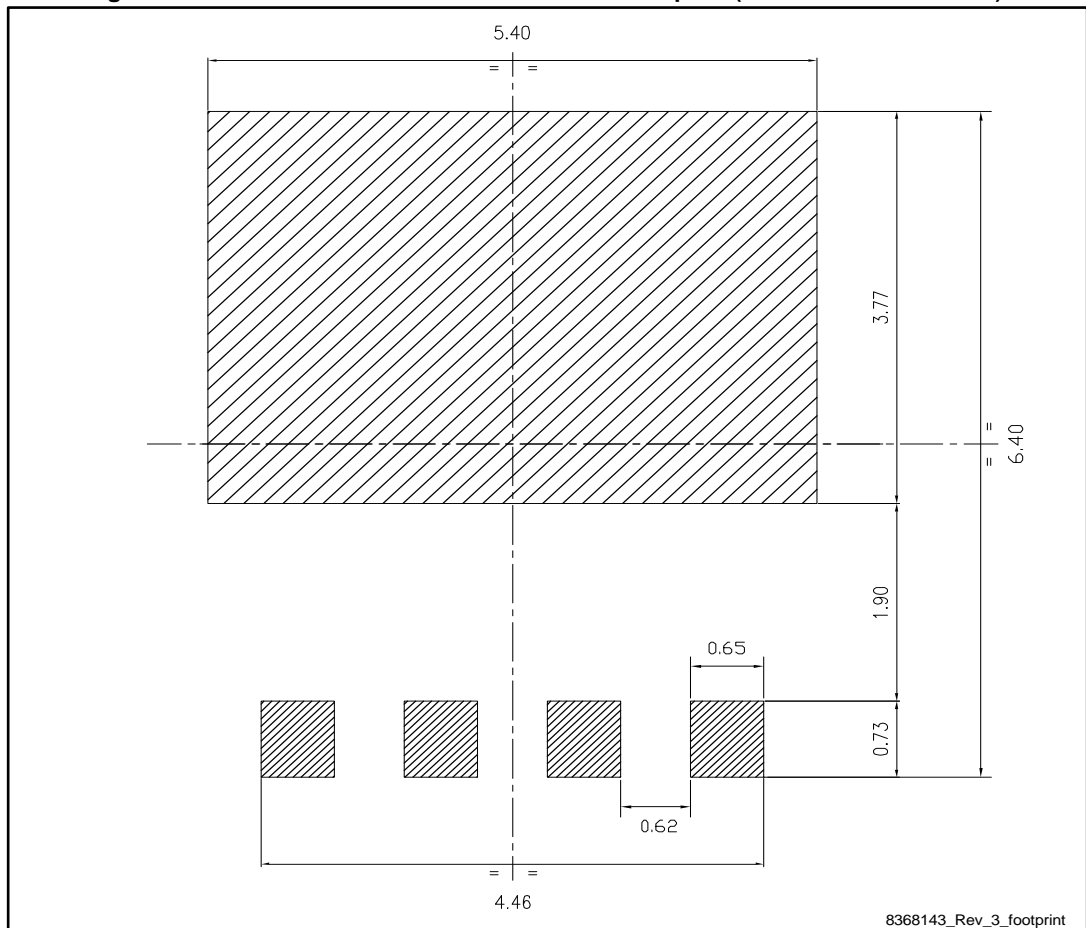


Table 8: PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.8	6	6.1
D	5.10	5.20	5.30
E	6.05	6.15	6.25
E2	3.10	3.20	3.30
D2	4.30	4.40	4.50
D4	4.8	5	5.1
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 21: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



### 4.2 PowerFLAT™ 5x6 packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)

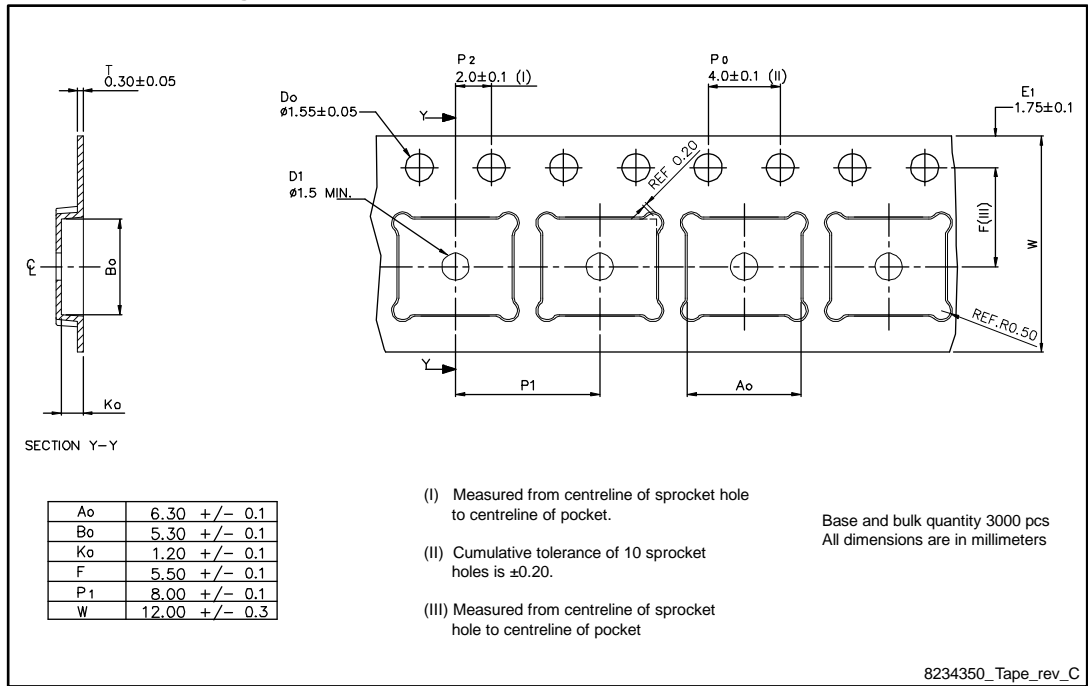


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape

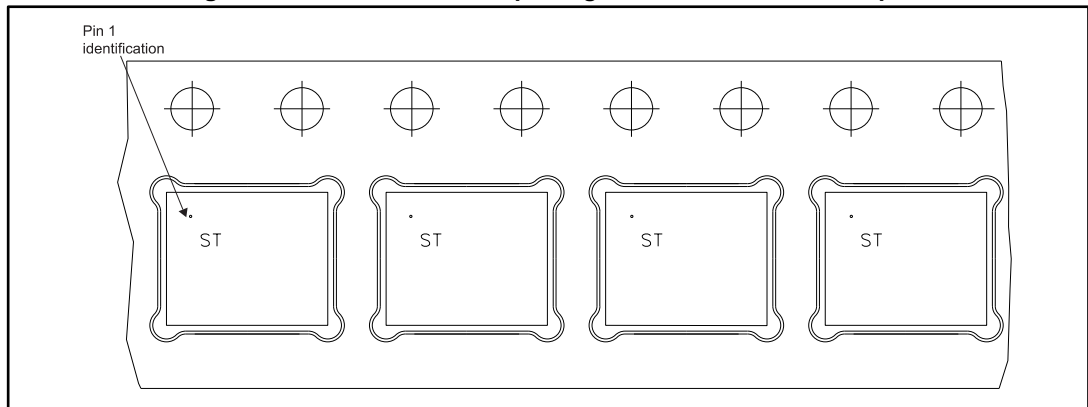
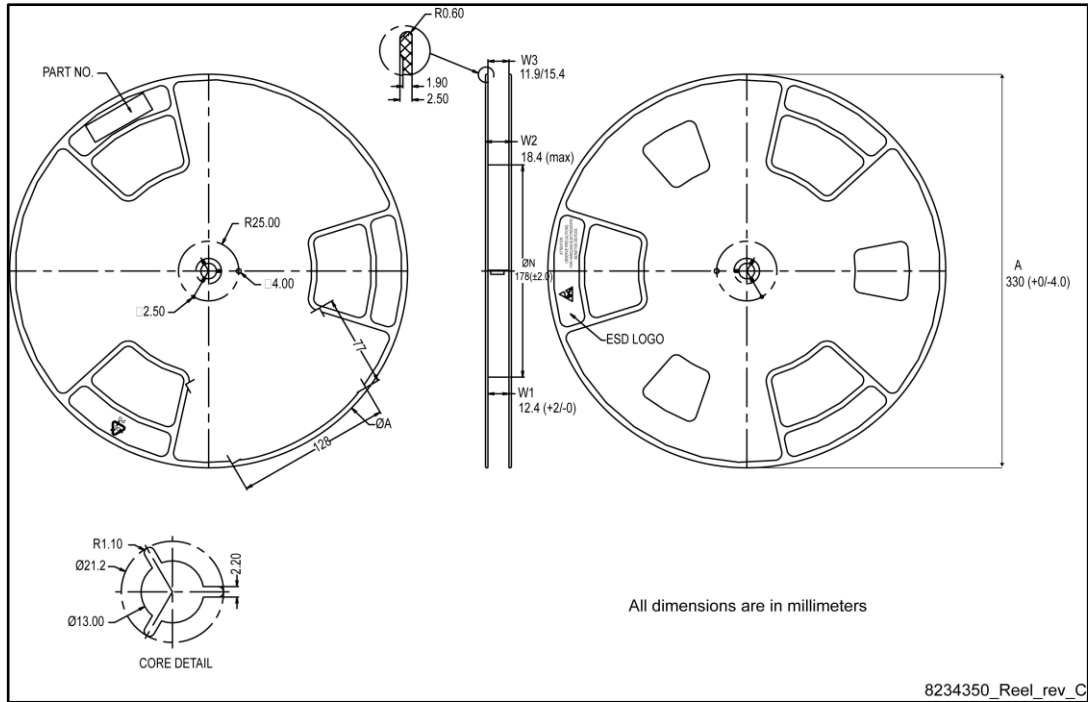


Figure 24: PowerFLAT™ 5x6 reel



## 5 Revision history

**Table 9: Document revision history**

Date	Revision	Changes
12-Jun-2014	1	First release.
02-Aug-2017	2	Updated title, features and description in cover page. Updated <i>Table 4: "On/off states"</i> , <i>Figure 3: "Thermal impedance"</i> , <i>Figure 11: "Normalized on-resistance vs temperature"</i> and <i>Section 4: "Package information"</i> . Minor text changes.

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