60V Synchronous Buck Multi-Chemistry Battery Charger

FEATURES

- **Wide Input Voltage Range: 4.5V to 60V**
- **Wide Battery Voltage Range: 2.4V to 60V**
- **Built-In Charge Algorithms for Lead-Acid and Li-Ion**
- **±0.5% Float Voltage Accuracy**
- **±5% Charge Current Accuracy**
- Maximum Power Point Tracking Input Control
- NTC Temperature Compensated Float Voltage
- Two Open Drain Status Pins
- Thermally Enhanced 28-Lead 4mm × 5mm QFN Package

APPLICATIONS

- Battery Backup for Lighting, UPS Systems, Security Cameras, Computer Control Panels
- Portable Medical Equipment
- Solar-Powered Systems
- Industrial Battery Charging

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DESCRIPTION

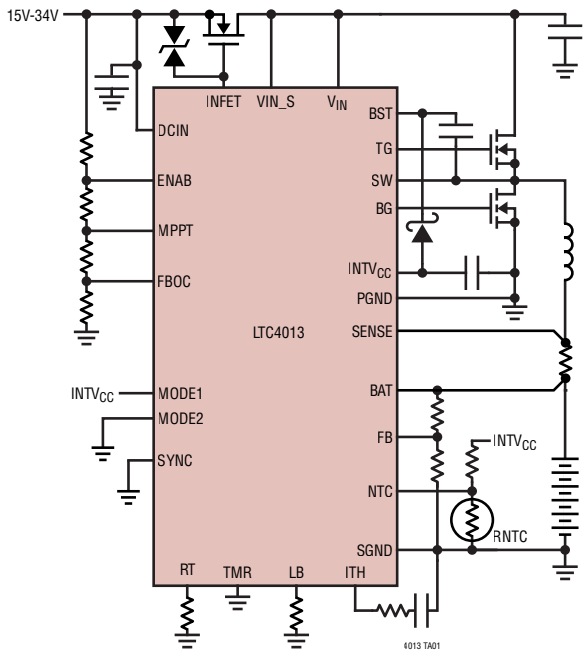
The LTC®4013 is a high voltage battery charger that is well suited for charging a wide range of lead-acid batteries including both vented and sealed types. It supports bulk, float, absorption and equalization charging. The LTC4013 also supports termination options for Li-Ion/Polymer and $LiFePO_4$ batteries.

Charging is performed with a high efficiency synchronous buck (step-down) converter that uses external N-channel MOSFETs. Switching frequency is resistor programmable or can be synchronized to an external clock. Charge current is programmed with an external sense resistor.

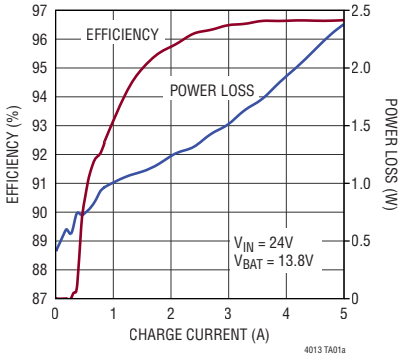
The LTC4013 also includes maximum power point tracking input-voltage regulation for limited power sources such as solar panels. Other features include user-programmable absorption and equalization times, temperature-compensated charge voltage and an external N-channel MOSFET isolation control circuit.

TYPICAL APPLICATION

15V-34V to 6 Cell Lead-Acid (12.6V) 5A Step-Down Battery Charger



Efficiency and Power Loss vs Charge Current



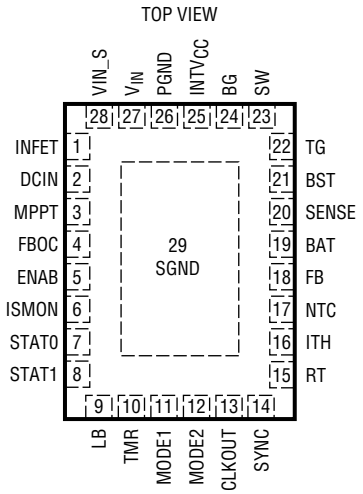
BASED ON APPLICATION ON BACK PAGE

ABSOLUTE MAXIMUM RATINGS

(Note 1)

DCIN, V_{IN}, VIN_S, ENAB, STAT0, STAT1 .... –0.3V to 60V
INFET ..... –0.3V to 73V
BST ..... –0.3V to 66V
STAT0, STAT1 .....5mA
SENSE, BAT ..... –0.3V to 60V
SENSE-BAT ..... –0.3V to 0.3V
FBOC, MPPT, FB, MODE1, MODE2, SYNC,
$INTV_{CC}$, NTC ..... –0.3V to 6V
TMR, LB, ITH ..... –0.3V to 3V
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC4013#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4013EUFD#PBF	LTC4013EUFD#TRPBF	4013	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC4013IUFD#PBF	LTC4013IUFD#TRPBF	4013	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). DCIN, V_{IN}, VIN_S = 18V, ENAB = 1.4V, SYNC = 0V unless otherwise noted.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range (DCIN, V_{IN})			●	4.5		60	V
Battery Voltage Range (BAT)			●	2.4		60	V
ENAB Pin Threshold (Rising) Threshold Hysteresis			●	1.175	1.220 170	1.275	V mV
ENAB Pin Bias Current					10		nA
V_{IN} UVLO		V_{IN} Rising, Power Enabled V_{IN} Rising, Power Disabled			3.45 3.08		V V
DCIN Pin	Operating Current Shutdown Current	Not Switching ENAB = 0V	 ●		480 4	625 7.9	µA µA
V_{IN} Pin	Operating Current Shutdown Current	Not Switching (Notes 3 and 4) ENAB = 0V, RT = 40.2k	 ●		2.1 32	2.8 80	mA µA
BAT Pin	Operating Current Shutdown Current	Not Switching ENAB = 0V	 ●		6.2 0.5	9.3 1.5	µA µA
SENSE Pin	Operating Current Shutdown Current	Not Switching ENAB = 0V	 ●		5.3 0.4	8.1 2.5	µA µA
SW Pin Current in Shutdown		ENAB = 0V, SW = 60V, BST = 66V			0.25		µA
STAT0, STAT1 Enabled Voltage		STAT0, STAT1 Pin Current =1mA STAT0, STAT1 Pin Current = 5mA			0.14 0.77	0.2 1.0	V V
STAT0, STAT1 Leakage Current		STAT0, STAT1 Pin Voltage = 60V	●			1	µA
FB Regulation Voltage (See Tables 2-5)							
Battery Float Voltage $V_{FB(FL)}$		MODE1 = L, H MODE2 = L, H	 ●	2.256 2.244	2.267 2.267	2.278 2.291	V V
		MODE1 = M, MODE2 = L, H	 ●	2.189 2.178	2.200 2.200	2.211 2.223	V V
		MODE1 = L, MODE2 = M	 ●	2.320 2.309	2.332 2.332	2.344 2.356	V V
Battery Absorption Voltage $V_{FB(ABS)}$		MODE1 = H, MODE2 = L, H MODE1 = L, MODE2 = H	 ●	2.355 2.343	2.367 2.367	2.380 2.392	V V
		MODE1 = M, MODE2 = L, H	 ●	2.388 2.376	2.400 2.400	2.412 2.425	V V
Battery Equalization Voltage $V_{FB(EQ)}$		MODE1 = L, H, MODE2 = H, TMR = Cap	 ●	2.487 2.475	2.500 2.500	2.513 2.526	V V
		MODE1 = M, MODE2 = H, TMR = Cap	 ●	2.587 2.574	2.600 2.600	2.613 2.627	V V
Battery Charge Voltage $V_{FB(CHG)}$		MODE1 = H, MODE2 = M	 ●	2.355 2.343	2.367 2.367	2.38 2.392	V V
		MODE1 = M, MODE2 = M	 ●	2.388 2.376	2.400 2.400	2.412 2.425	V V
Battery Recharge Voltage $V_{FB(RECHG)}$		MODE1 = M, H MODE2 = M	 ●	2.284 2.272	2.295 2.295	2.306 2.319	V V
NTC Amplifier Gain		$\Delta V_{FB(FL)}/\Delta V_{NTC}$			0.21		V/V
NTC Amplifier Offset		$\Delta V_{FB(FL)}$ with V_{NTC} = $INTV_{CC}/2$		–15	0	15	mV
FB Pin Current		V_{FB} = 3V			10		nA
LB Pin Current		V_{LB} = 2V		19.6	20	20.4	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). DCIN, V_{IN}, VIN_S = 18V, ENAB = 1.4V, SYNC = 0V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amp						
Error Amp Transconductance	$\Delta I_{ITH}/\Delta(V_{SENSE}–V_{BAT})$ V_{ITH} = 1.8V		1300	1800	2300	µmho
Error Amp Current Source	V_{ITH} =1.8V, V_{FB} = 2.0V, (Float) MODE1 = H, MODE2 = L		–6.5	–10	–13.5	µA
Error Amp Current Sink	V_{ITH} =1.8V, V_{FB} = 2.4V, (Float) MODE1 = H, MODE2 = L		18	27	35	µA
Current Sense (all measured as V_{SENSE} – V_{BAT} unless otherwise noted)						
Maximum Charging Sense Resistor Voltage	In Absorption, Float, Li-Ion Charge, BAT = 14V	●	48	50	52	mV
Equalization and Low Battery Charging Sense Resistor Voltage	BAT = 14V	●	8	10	12.5	mV
Current Sense C/10 Threshold	Termination when TMR = 0	●	2.0	4.6	7.0	mV
Constant Voltage (CV) Threshold	$V_{FB(ABS,EQ)}$ – V_{FB}, Timeout Initiation with Cap on TMR	●		15.6	24.5	mV
Overcurrent Charging Turnoff		●		100	106	mV
ISMON Fullscale Output Voltage	V_{SENSE} – V_{BAT} = 50mV			1.00		V
SENSE Input UVLO	V_{SENSE} Rising (Charging Enabled)	●	1.86	1.97	2.07	V
SENSE Input UVLO Hysteresis	V_{SENSE} Rising to Falling (Charging Disabled)			100		mV
Configuration Pins						
MODE1, MODE2 Pin, Low Threshold		●			0.8	V
MODE1, MODE2 Pin, Mid Threshold		●	1.3		1.8	V
MODE1, MODE2 Pin, High Threshold		●	2.5			V
Timer						
TMR Oscillator High Threshold				1.5		V
TMR Oscillator Low Threshold				0.97		V
Safety Timer Turn on Voltage	TMR Voltage Rising	●	0.45	0.5	0.65	V
Safety Timer Turn on Hysteresis Voltage				250		mV
TMR Source/Sink Current	TMR = 1.25V		8.5	10.0	11.5	µA
TMR Pin Period	CTMR = 0.2µF			20.8		ms
End of Charge Termination Time, t_{EOC}	CTMR = 0.2µF			3.03		hr
Equalization Charge Termination Time	CTMR = 0.2µF, MODE1 = M, H CTMR = 0.2µF, MODE1 = L			0.379 0.758		hr hr
$INTV_{CC}$ Regulator ($INTV_{CC}$ Pin)						
$INTV_{CC}$ Regulation Voltage				5.00		V
$INTV_{CC}$ Dropout Voltage	DCIN = 4.5V, $INTV_{CC}$ = 5mA			4.46		V
$INTV_{CC}$ Supply Short-Circuit Current	$INTV_{CC}$ = 0V		100	175		mA
NMOS FET Drivers						
Non-Overlap Time TG to BG				40		ns
Non-Overlap Time BG to TG				74		ns
Minimum On-Time BG				38		ns
Minimum On-Time TG				37		ns
Minimum Off-Time BG				65		ns
Top Gate Driver Switch On Resistance	BST – SW = 5V, Pull Up BST – SW = 5V, Pull Down			2.3 1.3		Ω Ω
Bottom Gate Driver Switch On Resistance	$INTV_{CC}$ = 5V, Pull Up $INTV_{CC}$ = 5V, Pull Down			2.3 1		Ω Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). DCIN, V_{IN}, VIN_S = 18V, ENAB = 1.4V, SYNC = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BST UVLO	TG Enabled (Rising) TG Disabled (Falling)			4.25 3.81		V V
OSC						
Switching Frequency	R_T = 40.2kΩ R_T = 232kΩ	●	950	1000 200	1050	kHz kHz
SYNC Pin Threshold (Falling Edge)			1.3	1.4	1.5	V
SYNC Pin Hysteresis				190		mV
CLK Output Logic Level	High Low		4.5		 0.5	V V
Input PowerPath Control						
Reverse Turn-Off Threshold Voltage	DCIN – V_{IN}	●	–7.3	–4.4	–1.3	mV
Forward Turn-On Threshold Voltage	DCIN – V_{IN}	●	–7.1	–4.2	–1.1	mV
Forward Turn-On Hysteresis Voltage	DCIN – V_{IN}			0.2		mV
INFET Turn-Off Current	INFET = V_{IN} + 1.5V			–9.0		mA
INFET Turn-On Current	INFET = V_{IN} + 1.5V			60		µA
INFET Clamp Voltage	I_{INFET} = 2µA , DCIN = 12V to 60V V_{IN} = DCIN – 0.1V Measure VINFET – DCIN	●		11.0	12.5	V
INFET Off Voltage	I_{INFET} = –2µA , DCIN = 12V to 59.9V V_{IN} = DCIN +0.1V Measure VINFET – DCIN	●		–2.2	–1.6	V
DCIN to BAT UVLO	Switching Regulator Turn Off (V_{DCIN} – V_{BAT} Falling)			69		mV
	Switching Regulator Turn On (V_{DCIN} – V_{BAT} Rising)			99		mV
MPPT Regulation						
FBOC Voltage Range		●	1.0		3.0	V
MPPT Sample Period				10.2		s
MPPT Sample Pulse Width				271		µs
Regulation Input Offset	Set FBOC Look at MPPT Regulation		–40		40	mV
MPPT Input Burst Mode Turn On Threshold	V_{MPPT} – V_{FBOC} (Converted) , V_{FBOC} = 1.5V V_{SENSE} – V_{BAT} < C/10 Part Enter Burst Mode	●	–45	–32	–15	mV
MPPT Input Burst Mode Hysteresis	FBOC = 1.5V, V_{SENSE} – V_{BAT} < C/10 MPPT Turn Off – Turn On	●	35	62	85	mV

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

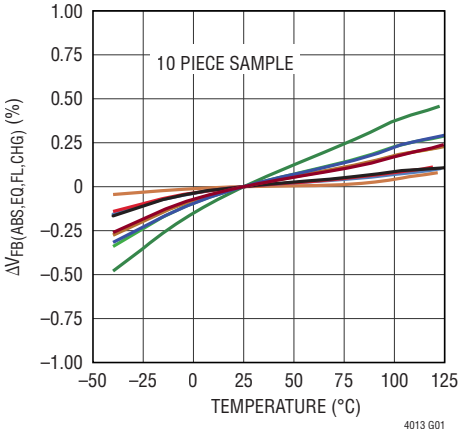
Note 2. The LTC4013 is tested under pulse loaded conditions such that $T_J \approx T_A$. The LTC4013E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4013I is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula: $T_J = T_A + P_D \bullet \theta_{JA}$ where θ_{JA} (in °C/W) is the package thermal impedance. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors. This IC includes over temperature protection that is intended to protect the device during momentary overload. Junction temperature will exceed 125°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3. V_{IN} does not include switching currents.

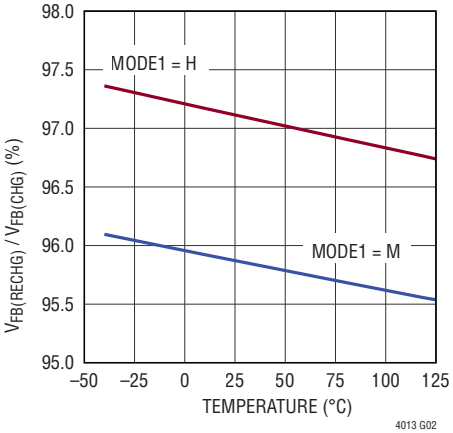
Note 4. I_{VIN} current also includes current that charges capacitance on CLKOUT. This current is approximately $C_{CLKOUT} \bullet 5V \bullet f_{SW}$. For this test C_{CLKOUT} was 100pF, f_{SW} was 1MHz (R_T = 40.2k) so the current included is 0.5mA. In normal operation the CLKOUT capacitance is much less.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

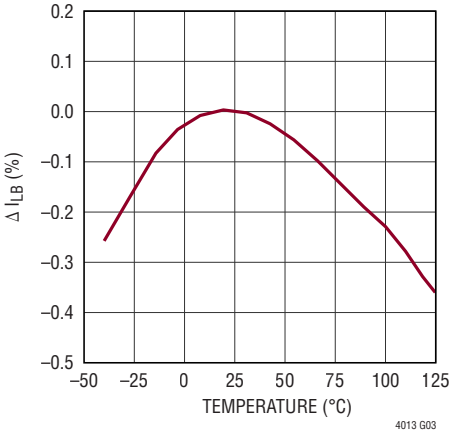
Change in Absorption, Equalization, Float and Li-Ion Charge Voltages vs Temperature



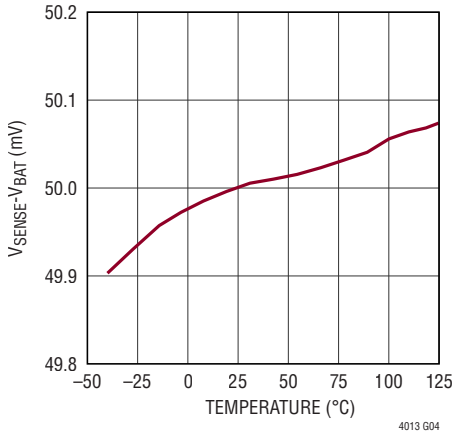
Li-Ion Recharge% vs Temperature



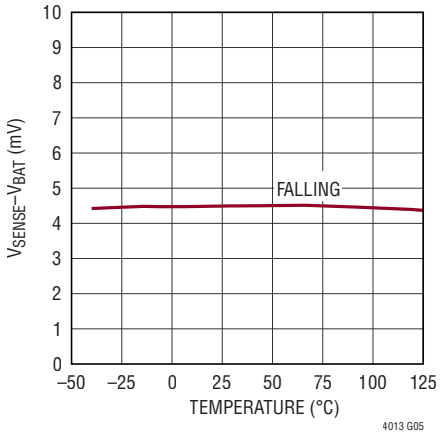
Change In Low Battery (LB) Current vs Temperature



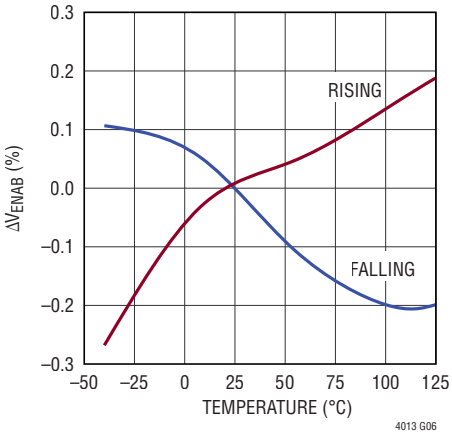
Current Sense Servo Voltage vs Temperature



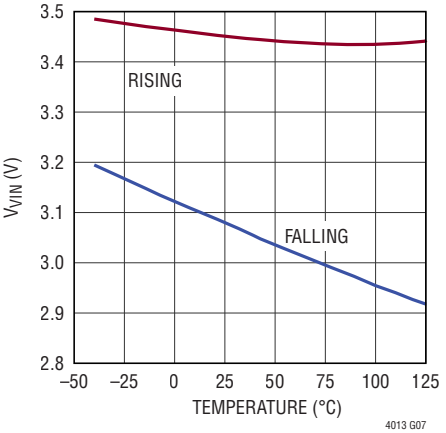
C/10 Threshold vs Temperature



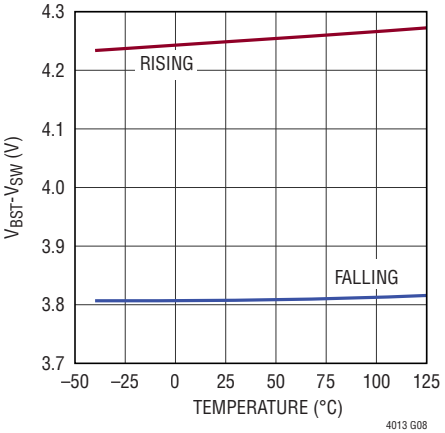
Change in ENAB Voltage vs Temperature



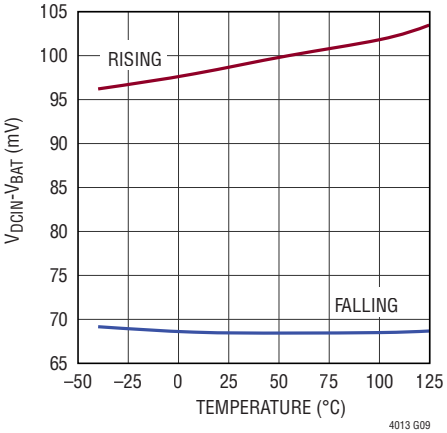
V_{IN} UVLO Voltage vs Temperature



BST UVLO Voltage vs Temperature

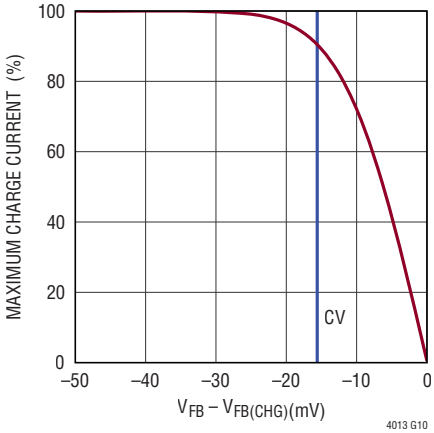


DCIN to BAT UVLO Voltage vs Temperature

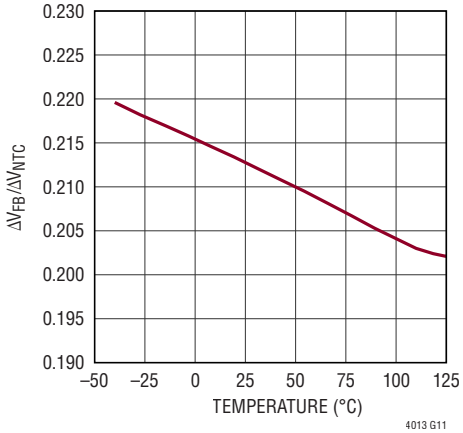


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

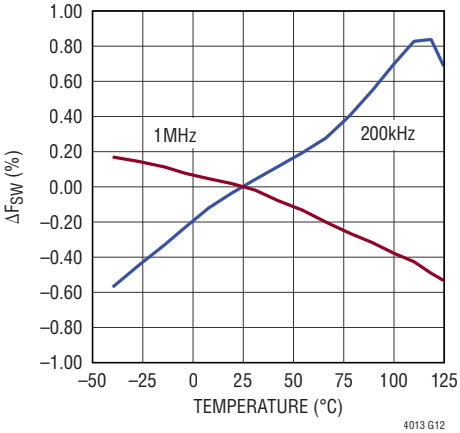
Maximum Charge Current vs ΔV from V_{CHARGE}



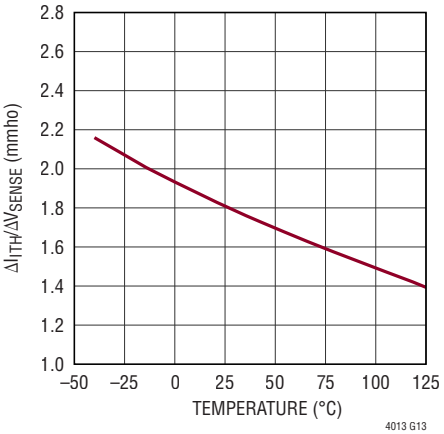
NTC Amplifier Gain vs Temperature



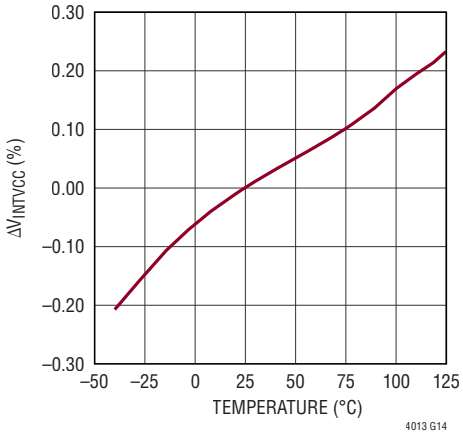
Change in Switching Regulator Frequency vs Temperature



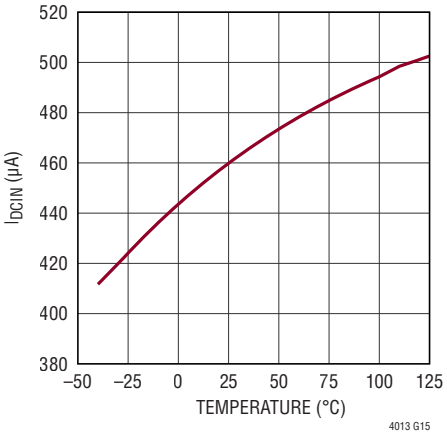
Error Amp Transconductance vs Temperature



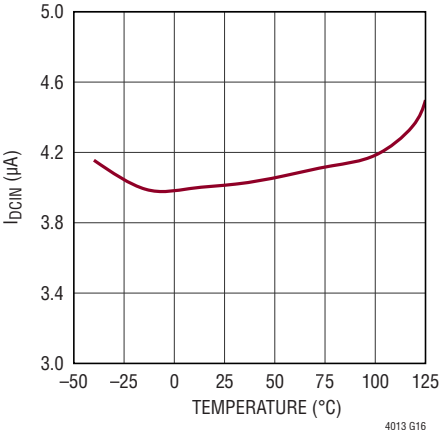
Change in V_{INTVCC} vs Temperature



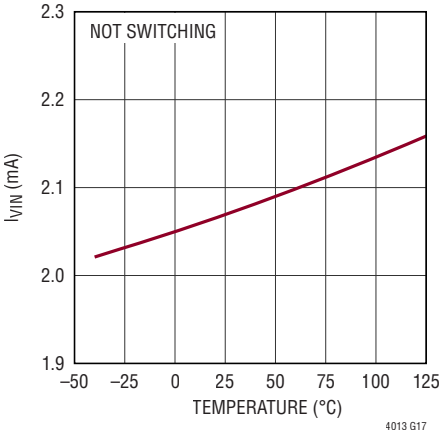
DCIN Operating Current vs Temperature



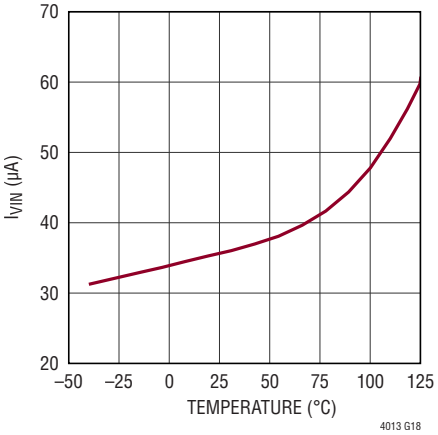
DCIN Current in Shutdown vs Temperature (Note 3)



V_{IN} Operating Current vs Temperature (Note 4)



V_{IN} Current in Shutdown vs Temperature



PIN FUNCTIONS

INFET (Pin 1): Input PowerPath MOSFET Gate Drive. An internal charge pump provides turn-on drive for this pin. This pin should be connected to the gate of an external N-channel MOSFET to prevent battery discharge when DCIN is less than the battery voltage.

DCIN (Pin 2): Input Supply Pin. This pin is used to sense the input voltage to determine whether to enable the INFET charge pump. It also supplies power to the INFET charge pump.

MPPT, FBOC (Pins 3, 4): Maximum Power Point Tracking (MPPT) Regulation Loop Set-Point Pins. The input voltage regulation loop regulates charge current, providing maximum power charging in the presence of a power limited source such as a solar panel. A resistor divider is placed from the input supply to MPPT, FBOC and ground. These pins are used to program the input voltage regulation loop as a percentage of the input open circuit voltage. If the input voltage falls below the programmed percentage of the open-circuit voltage, the MPPT loop will reduce charge current to maintain the target maximum power point voltage at DCIN. If the input voltage regulation feature is not used, connect FBOC to $INTV_{CC}$.

ENAB (Pin 5): Precision Threshold Enable Pin. The enable threshold is 1.22V (rising), with 170mV of hysteresis. In shutdown, all charging functions are disabled and input supply current is reduced.

ISMON (Pin 6): Charge Current Monitor Pin. The voltage on this pin is twenty times the differential voltage between SENSE and BAT and can be used to monitor charge current.

STAT0, STAT1 (Pins 7, 8): Open drain outputs that indicate the charger status. These pins can sink 5mA, enabling them to drive an LED. Specific states are detailed in Table 2.

LB (Pin 9): Low Battery Level Control Pin. A precision 20µA current sourced from LB to an external resistor sets the detection voltage for a deeply discharged battery. If FB stays below LB for 1/8 of the absorption timeout period, charging is stopped. Charging is reinitiated with an ENAB pin toggle, a power cycle or by swapping out the battery.

TMR (Pin 10): Timer Capacitor Pin. A capacitor from this pin to ground sets the time the charger spends in various charging stages. The equalization timeout is a ratio of this time, either 1/4 or 1/8 of the absorption time, depending on the MODE pins settings. The low battery timeout period is 1/8 of the absorption time.

MODE1, MODE2 (Pins 11, 12): Charge Algorithm Control Pins. See Table 1. The LTC4013 supports 2, 3 and 4-stage lead-acid as well as Li-Ion charging algorithms with and without termination. The MODE pins are tri-state and should be strapped to $INTV_{CC}$, ground or left floating.

CLKOUT (Pin 13): Oscillator Frequency Output Pin. This logic output is roughly 180 degrees out of phase with the switching regulator's oscillator.

SYNC (Pin 14): Frequency Synchronization Pin. This pin allows the switching frequency to be synchronized to an external clock. The R_T resistor should be chosen to operate the internal clock 20% slower than the SYNC pulse frequency. Ground SYNC when not in use.

RT (Pin 15): Switching Regulator Frequency Control Pin. A mandatory resistor from RT to ground sets the switching frequency between 200kHz and 1MHz.

ITH (Pin 16): Compensation Control Pin. This pin is used to compensate the switching regulator's constant-current control loop.

NTC (Pin 17): Thermistor Input Pin. With the use of an external NTC thermistor, the NTC pin can be used to develop a temperature dependent charge voltage for lead-acid batteries. NTC pin voltages above 3.3V disable the NTC function. The NTC function is not suitable for Lithium Ion batteries and should be disabled by strapping NTC to $INTV_{CC}$.

FB (Pin 18): Constant-Voltage Feedback Pin. This pin provides feedback for regulating battery voltage during the constant-voltage phase of charging. A resistor divider from the battery to this pin sets the constant-voltage charging level.

PIN FUNCTIONS

BAT, SENSE (Pins 19, 20): Charge Current Sense Pins. Battery charge current is monitored and regulated via a current sense resistor between SENSE and BAT. The constant-current servo voltage between these pins is 50mV. Overcurrent shutdown occurs when the SENSE to BAT voltage exceeds 100mV.

BST (Pin 21): High Side Gate Drive Supply Pin. BST provides a flying 5V supply for the high-side MOSFET driver. Connect a 0.22µF capacitor from this pin to SW. Connect a diode with its cathode to this pin and its anode to the $INTV_{CC}$ pin.

TG (Pin 22): Top Gate Drive Pin. TG drives the gate of the top side external N-channel MOSFET.

SW (Pin 23): Switching Regulator Power Pin. SW connects to the power supply switch node which includes one side of the inductor, the source of the top side MOSFET, the drain of the bottom side MOSFET and the boost capacitor.

BG (Pin 24): Bottom Gate Drive Pin. BG drives the gate of the external bottom side N-channel MOSFET.

$INTV_{CC}$ (Pin 25): Internal V_{CC} Pin. Powered by V_{IN}, this pin is the output of a 5V regulator that powers the internal control logic and analog circuits. Connect a ceramic capacitor from $INTV_{CC}$ to PGND. The BST pin refresh diode anode should also be connected to $INTV_{CC}$.

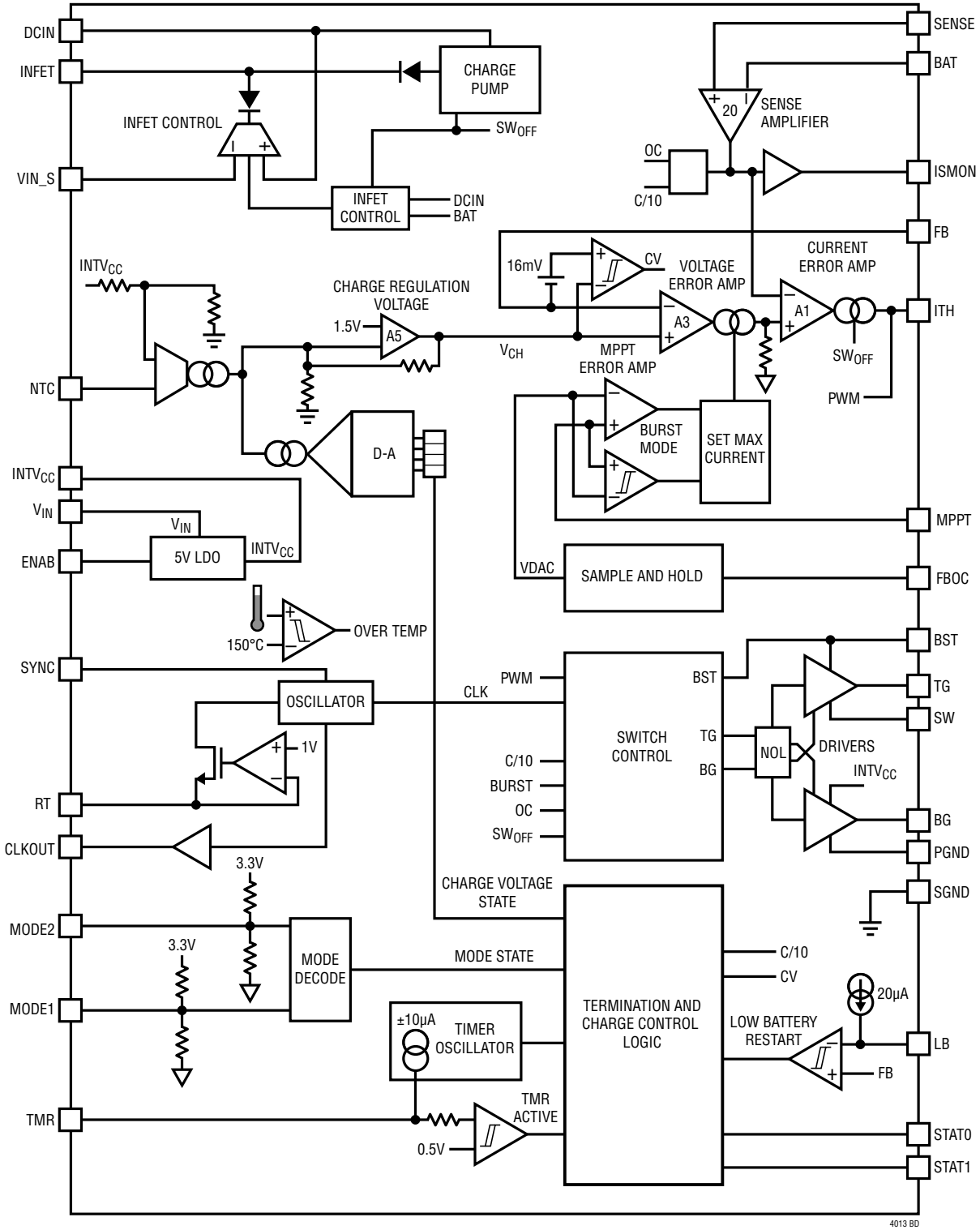
PGND (Pin 26): Power Ground. This is the power ground for the LTC4013. It services only the BG pin drive.

V_{IN} (Pin 27): Input Supply Pin. V_{IN} provides power to the $INTV_{CC}$ internal 5V regulator. It is usually tied to the switching regulator high side MOSFET and should be bypassed with one or more low-ESR capacitors to ground.

VIN_S (Pin 28): Input Supply Sense Input. VIN_S provides a Kelvin input for the V_{IN} connection of the input PowerPath circuitry.

SGND (Exposed Pad Pin 29): Signal Ground Reference. This pin is the quiet ground used as a reference point for critical resistor dividers such as the battery feedback divider, MPPT divider and thermistor. Connect SGND to the output decoupling capacitor negative terminal and battery negative terminal. Solder SGND to a solid ground plane through multiple vias for rated thermal performance.

BLOCK DIAGRAM



OPERATION

OVERVIEW

The LTC4013 is a high-voltage multi-chemistry battery charger with specific focus on lead-acid batteries. It incorporates a step-down (buck) DC/DC synchronous switching controller using external N-channel MOSFETS for high efficiency. It accommodates a wide range of battery voltages from 2.4V to 60V and is optimized for high current charging applications.

Selectable charger profiles are:

2-stage charging: constant-current (bulk) to constant-voltage with and without timer termination.

3-stage lead-acid charging: bulk, absorption and float with low battery restart and either charge-current (C/10) or safety-timer absorption to float transition control.

4-stage lead-acid charging: bulk, absorption, equalization, and float with low battery restart and safety-timer equalization cutoff and safety-timer absorption to float transition control.

Li-Ion constant-current to constant-voltage charging with either charge-current (C/10) or safety-timer charge termination.

DC/DC OPERATION

(See Block Diagram)

The LTC4013 uses a fixed-frequency, average current mode DC/DC converter to regulate charge current. When the battery reaches the charge voltage, current is reduced by a voltage regulation loop.

Battery current is sensed via a resistor placed between SENSE and BAT. The amplified signal is compared to a voltage that represents the maximum allowable charge current and regulates the average current by controlling the duty cycle of the output switches. The current control loop servos the differential voltage between SENSE and BAT to 50mV making I_{CHGMAX} = 50mV/R_{SENSE}. A frequency-compensation pin (ITH) is used to control the constant-current feedback loop stability.

At startup, the maximum current is ramped over approximately 1.6ms to provide soft start. There is an additional burst mode feature used for maximum power point transfer to facilitate low solar panel current operation.

When the battery voltage reaches the programmed charge voltage, error amplifier A3 adjusts the charge current to servo the battery voltage to the programmed level and can reduce the current to zero.

The charge voltage is determined by amplifier A5 and the charge algorithm selected. The voltage can follow a continuous function of temperature controlled by an amplifier connected to the NTC pin. A resistor divider with a thermistor sets the temperature coefficient of the voltage.

The switching regulator's oscillator frequency is set by a resistor from the RT pin to ground. The clock frequency can optionally be synchronized to an external oscillator by using the SYNC pin.

The step-down (buck) switching regulator uses external low $R_{DS(ON)}$ MOSFETs for both high and low side switches to deliver high charge current. When the current level falls below I_{CHGMAX}/10 the bottom MOSFET is disabled and switching operation is discontinuous with only the bottom side MOSFET body diode used for low side conduction. This diode emulation mode ensures the battery is not discharged by continuous conduction.

Supply voltage for the top gate drive is generated by a boost circuit that uses an external diode and boost capacitor charged from $INTV_{CC}$. If BST - SW is below 3.8V (e.g. at startup), the bottom side MOSFET is enabled to refresh the BST capacitor.

Solar Panel Maximum Power Point Tracking

If the MPPT function is enabled (FBOC pin voltage < 3V), the LTC4013 employs an MPPT circuit that compares a stored open-circuit input voltage measurement against the instantaneous DCIN voltage while charging. The LTC4013 then uses an input voltage sense amplifier to reduce the charge current if the DCIN voltage falls below the user

OPERATION

defined percentage of the open-circuit voltage. With this algorithm the LTC4013 optimizes power transfer for a variety of different input sources.

When MPPT is enabled, the LTC4013 periodically measures the open-circuit input voltage. About once every 10.2s the LTC4013 pauses charging, samples the input voltage as measured through a resistor divider at the FBOC pin, and reproduces this value internally with a digital-to-analog converter (DAC). When charging resumes, the DAC voltage, VDAC, is compared against the MPPT pin voltage that is programmed with a resistor divider. If the MPPT voltage falls below VDAC, charge current is reduced to regulate the input voltage at that level. This regulation loop maintains the input voltage at or above a user defined level that corresponds to the peak power available from the applied source. Regular input sampling is useful, for instance, to provide first order temperature compensation of a solar panel.

The sampling time is fixed internally. Switching stops for approximately 1ms every 10.2s. There is an initial 720µs delay allowing DCIN to rise to its open circuit voltage. During the next 300µs, the FBOC pin voltage is sampled and stored. The sampling of DCIN is done at an extremely low duty cycle to have minimal impact on the total charge current. Figure 1 shows a picture of MPPT timing.

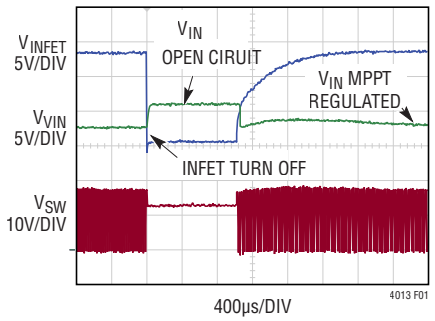


Fig 1. MPPT Timing

MPPT Burst Mode Operation

In low light, it is desirable to improve switching regulator efficiency for maximum power delivery. The LTC4013 contains proprietary circuitry that improves switching regulator efficiency during these conditions. Efficiency is improved by reducing the maximum switching regulator current and periodically disabling the switching regulator, resulting in burst-mode operation. Burst-mode is enabled when MPPT is below the sampled FBOC voltage by approximately 32mV and the current is below $I_{CHGMAX}/10$ (SENSE-BAT < 5mV). The LTC4013 stays in burst-mode until the next sampling period when it is reevaluated. If MPPT is above the sampled FBOC voltage by approximately 32mV then burst-mode is disabled. The net result is that in burst-mode the DCIN voltage has approximately a 64mV hysteretic ripple at the FBOC pin. During burst-mode, maximum current is set to approximately $I_{CHGMAX}/5$ (SENSE-BAT = 10mV).

Battery Charger Operation

There are a variety of battery chemistries and there are numerous online resources and books available for education. One good resource is www.batteryuniversity.com. Many battery manufacturers also provide detailed information.

The LTC4013 provides constant-current/constant-voltage charging. When the battery voltage is below the constant-voltage servo level, charge current is controlled by the constant-current control loop. As the battery charges, its voltage increases and eventually holds at the constant-voltage servo level whereupon charge current tapers naturally toward zero as the battery tops off.

In constant-current charging the charge current is controlled by the fixed servo voltage of 50mV divided by the external sense resistor between SENSE and BAT.

Once the battery voltage increases and the charger is in the constant-voltage charging phase, the battery charge voltage is controlled by the FB pin.

The FB voltage regulation levels are appropriate for a single-cell lead-acid battery. For instance, a 2.267V single-cell float voltage corresponds to a 6-cell battery voltage of 6 • 2.267V = 13.6V.

The LTC4013 also contains a charge cycle timer. This timer is used for the absorption to float transition in 3-stage and 4-stage lead-acid charging, equalization timeout in 4-stage lead-acid charging and constant-voltage timeout in both Li-Ion and 2-stage charging. The timer is activated by connecting a capacitor from the TMR pin to ground. Grounding TMR disables all timer functions.

OPERATION

The LB pin provides a user adjustable low battery voltage setting that sets the re-start level in 2-stage, 3-stage and 4-stage charging and the low battery fault level in Li-Ion charging. The LB pin produces a precision 20µA current which results in a precision voltage when a resistor is placed from LB to ground. The LB pin is compared internally to the FB pin for low battery determination.

Four possible charging algorithms can be selected by pin strapping or manipulating the MODE0 and MODE1 pins (see Table 1). These pins should be tied either low (GND), high ($INTV_{CC}$) or mid (floating). The charge algorithms are described below.

2-Stage Charging

2-stage charging is useful for batteries with no absorption preconditioning. Charging is initiated on input power-up whereupon the battery charges with constant-current at I_{CHGMAX} toward $V_{FB(FL)}$. The STAT0 pin pulls low immediately indicating that charging has begun. Once the battery terminals approach $V_{FB(FL)}$, the constant-voltage control loop takes over holding the battery voltage steady as the charge current naturally tapers to zero. Once the constant-voltage loop takes control, the STAT1 pin also pulls low indicating the change from constant-current to constant-voltage charging.

If a capacitor is used on the TMR pin, the charge cycle terminates after an accumulated period of t_{EOC} in constant-voltage mode at which time STAT0 and STAT1 will indicate termination by switching off. Alternately, if the TMR pin is grounded, 2-stage charging will charge forever at $V_{FB(FL)}$ with no termination.

Charging is re-initiated from termination if the FB-referred battery voltage drops below the LB threshold voltage as set by the LB pin, or if the LTC4013 is powered off and back on by cycling the ENAB pin or input power.

Defective battery protection is enabled if the timer capacitor is used. Whenever the FB-referred battery voltage is below the LB threshold, charge current is automatically reduced to $I_{CHGMAX}/5$. If a defective battery remains below the low battery threshold longer than 1/8 of the timer period ($t_{EOC}/8$) the charge cycle terminates. A defective battery fault is indicated by STAT0 turning off and STAT1 turning on.

There are two voltage settings available for 2-stage charging as noted in Table 1.

2-stage charging for a lead-acid battery has the disadvantage of not fully charging the battery, resulting in diminished capacity over time due to increased deposits on the electrodes.

3-Stage Charging

A more complete lead-acid battery charging method is 3-stage charging utilizing an absorption phase which increases the amount of stored charge in the battery. Because the absorption voltage is above the electrochemical float level, the time that the battery stays in this condition should be limited either by a timer (the safest method) or waiting for the charge current to diminish. Minor gassing of water from the battery can occur from charging the battery above the float voltage, so choosing an appropriate absorption voltage is important for best battery life. Always consult the battery manufacturer for their recommendations.

3-stage charging is initiated on input power-up whereupon the battery charges with constant-current at I_{CHGMAX} toward $V_{FB(ABS)}$. The STAT0 pin pulls low immediately indicating that charging has begun. As the battery voltage approaches $V_{FB(ABS)}$, charge current naturally tapers to zero. When the charge current drops to $I_{CHGMAX}/10$, STAT1 also pulls low and the charge voltage setting changes to the $V_{FB(FL)}$ voltage. At this lower level, the constant-voltage control loop will "capture" and hold the battery voltage as it slowly drops from $V_{FB(ABS)}$ down to $V_{FB(FL)}$.

Alternately, the transition from absorption charging to float charging can be controlled with the timer by placing a capacitor on the TMR pin. When the battery voltage reaches constant-voltage in the absorption phase, the timer begins. At the end of the accumulated timer period in constant-voltage mode at $V_{FB(ABS)}$, the charge voltage changes to the $V_{FB(FL)}$ voltage and will remain there. Again, STAT1 turns on, indicating the transition from the $V_{FB(ABS)}$ charging level to the $V_{FB(FL)}$ charging level.

OPERATION

If a load subsequently pulls the FB-referred battery voltage below the LB pin, or if the LTC4013 is powered off and back on by cycling the ENAB pin or input power, a new 3-stage charge cycle is initiated with a new absorption phase.

Defective battery protection is enabled if the timer capacitor is used. Whenever the FB-referred battery voltage is below the LB threshold, charge current is automatically reduced to $I_{CHGMAX}/5$. If a defective battery remains below the low battery threshold longer than 1/8 of the timer period ($t_{EOC}/8$) the charge cycle terminates. A defective battery fault is indicated by STAT0 turning off and STAT1 turning on.

There are different options for absorption and float voltages. Table 1 details the MODE pins settings and FB voltages. Figure 2 shows an example of a 3-stage charge cycle.

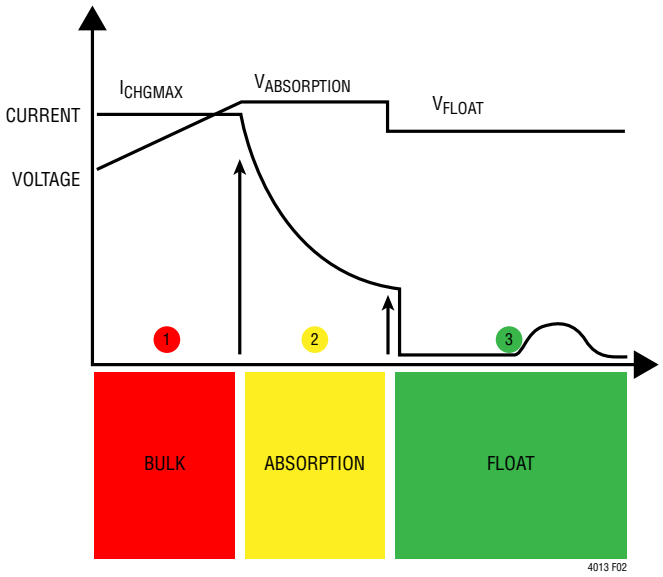


Figure 2. 3-Stage Charge Cycle

4-Stage Charging

A 4-stage charging algorithm adds an equalization phase to the 3-stage method after the absorption phase. The equalization voltage is significantly higher than the absorption voltage and works in two ways. One is to purposely introduce gassing which stirs the battery electrolyte and reduces electrolyte stratification. Equalization also electrochemically eliminates sulfates on the electrodes which is the main cause of battery performance degradation. Sulfates typically form in heavily discharged batteries. Equalization is not done with sealed batteries because of the gassing. If lost water is not replaced, the battery will be degraded. An equalization cycle should be performed on a periodic, service-only, basis only if the manufacturer of the battery approves of the technique and should be monitored for dangerous conditions. Use of 4-stage charging is highly discouraged for solar applications as sporadic light patterns can cause multiple equalization cycles per day. Not all batteries can be charged with a 4-stage cycle so you must consult with your battery manufacturer as to its frequency of use and recommended charge voltage.

Charging is initiated on input power-up whereupon the battery charges with constant-current at I_{CHGMAX} toward $V_{FB(ABS)}$. The STAT0 pin pulls low immediately indicating that charging has begun. As the battery voltage approaches $V_{FB(ABS)}$, charge current naturally tapers to zero and the timer starts. At the end of the timer period, the charge voltage setting changes to the equalization voltage $V_{FB(EQ)}$. The timer is then restarted and the charge current setting is dropped to $I_{CHGMAX}/5$. The equalization phase continues until the end of equalization timeout, either $t_{EOC}/4$ or $t_{EOC}/8$, as programmed by the MODE pins. After the equalization timeout, the charge voltage is reduced to the $V_{FB(FL)}$ voltage and STAT1 turns on indicating the end of the charge cycle. The 4-stage cycle always requires the use of a capacitor on the TMR pin as a safety precaution to ensure that charging time at the high equalization voltage is limited. If the TMR pin is grounded, the 4-stage charge cycle will revert to 3-stage charging with no equalization phase.

The LTC4013 ensures that only one equalization phase will run per power-on cycle. After a 4-stage cycle completes, all subsequent low battery (LB) cycles will only trigger a 3-stage cycle with absorption phase and not a 4-stage cycle with equalization. Only a power-off event or ENAB pin cycle will result in a complete 4-stage equalization cycle.

OPERATION

Defective battery protection is enabled if the timer capacitor is used. Whenever the FB-referred battery voltage is below the LB threshold, charge current is automatically reduced to $I_{CHGMAX}/5$. If a defective battery remains below the low battery threshold longer than 1/8 of the timer period ($t_{EOC}/8$) the charge cycle terminates. A defective battery fault is indicated by STAT0 turning off and STAT1 turning on.

Figure 3 shows an example of a 4-stage charge cycle.

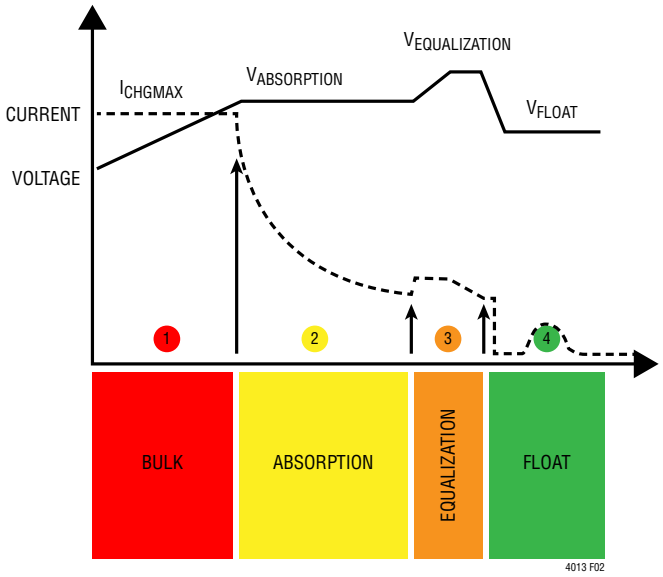


Figure 3. 4-Stage Charge Cycle

Li-Ion Charging

The LTC4013 can also charge Li-Ion batteries including Li-Polymer and $LiFePO_4$.

Charging is initiated on input power-up whereupon the battery charges with constant-current at I_{CHGMAX} toward $V_{FB(CHG)}$. The STAT0 pin pulls low immediately indicating that charging has begun. As the battery voltage approaches $V_{FB(CHG)}$, charge current naturally tapers to zero. The STAT1 pin also turns on indicating constant-voltage operation. There are two options for Li-Ion charge termination. If a capacitor is included on the TMR pin, the timer starts when the battery reaches the constant-voltage regulation point. Once the timer expires (t_{EOC}), charging is terminated. Alternately, if the TMR pin is grounded, the timer is disabled and charging terminates when the charge current drops to 1/10 of I_{CHGMAX} (C/10). Termination is indicated by STAT0 and STAT1 turning off.

The LTC4013 will begin charging again if the FB-referred battery voltage falls below the LiIon recharge level $V_{FB(RECHG)}$. The recharge voltage is either 97.0% or 95.6% of $V_{FB(CHG)}$ depending on the MODE pins. To avoid frequent recharge events due to voltage sag on $LiFePO_4$ batteries, the wider difference is recommended.

Defective battery protection is enabled if the timer capacitor is used. Whenever the FB-referred battery voltage is below the LB threshold, charge current is automatically reduced to $I_{CHGMAX}/5$. If a defective battery remains below the low battery threshold longer than 1/8 of the timer period ($t_{EOC}/8$) the charge cycle terminates. A defective battery fault is indicated by STAT0 turning off and STAT1 turning on.

Mode Pins and Battery Charge Voltages

The LTC4013 provides several different options for setting the $V_{FB(FL)}$, $V_{FB(ABS)}$ and $V_{FB(EQ)}$ voltages. In normal mode, single-cell absorption is approximately 100mV above float (600mV for 6 cells), equalization is then approximately 133mV above absorption (800mV for 6 cells). Another option uses a wider voltage spread where single-cell absorption voltage is 200mV above float (1.2V for 6 cells) and equalization is 200mV above absorption (1.2V for 6 cells). Absolute voltages are adjusted through the FB resistor divider to gain these voltages up proportionately. It is important to consult your battery manufacturer for their suggestion on charging voltages. There is no industry consensus and it depends heavily on the type of battery and anticipated usage.

Table 1 shows the MODE0/1 pin settings to select the charge algorithm and the range of charge voltage settings for the normal and wide spread voltage modes and Table 2 shows the STAT0/1 indicator pin values in various charging states.

OPERATION

Table 1. Mode Pin Settings

Stages	Spread	MODE1	MODE2	VFLOAT	VRecharge	VAbsorb	VEqualize	TEqualize
Li-Ion	Wide	M	M	2.400V	2.295V			
Li-Ion	Normal	H	M	2.367V	2.295V			
2-Stage	n/a	L	L	2.267V				
2-Stage	n/a	L	M	2.333V				
3-Stage	Wide	M	L	2.200V		2.400V		
3-Stage	Normal	H	L	2.267V		2.367V		
4-Stage	Normal	L	H	2.267V		2.367V	2.500V	$t_{EOC}/4$
4-Stage	Normal	H	H	2.267V		2.367V	2.500V	$t_{EOC}/8$
4-Stage	Wide	M	H	2.200V		2.400V	2.600V	$t_{EOC}/8$

Table 2. Status Pin Indications

STAT0	STAT1	Li-Ion / 2-Stage	3-Stage / 4-Stage
OFF	OFF	Not Charging or Terminated	Not Charging
ON	OFF	Charging C_C	Absorb/Equalize Charging
ON	ON	Charging CV	Float Charging
OFF	ON	Low Battery or Thermal Shutdown Fault	

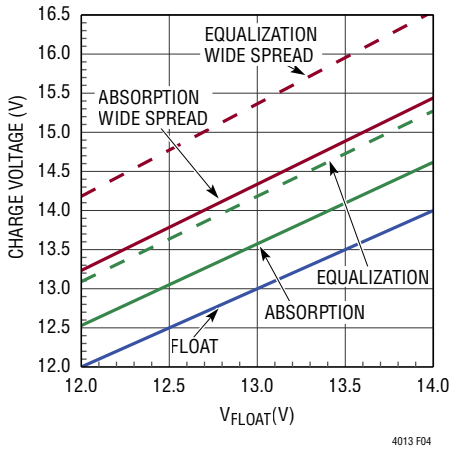
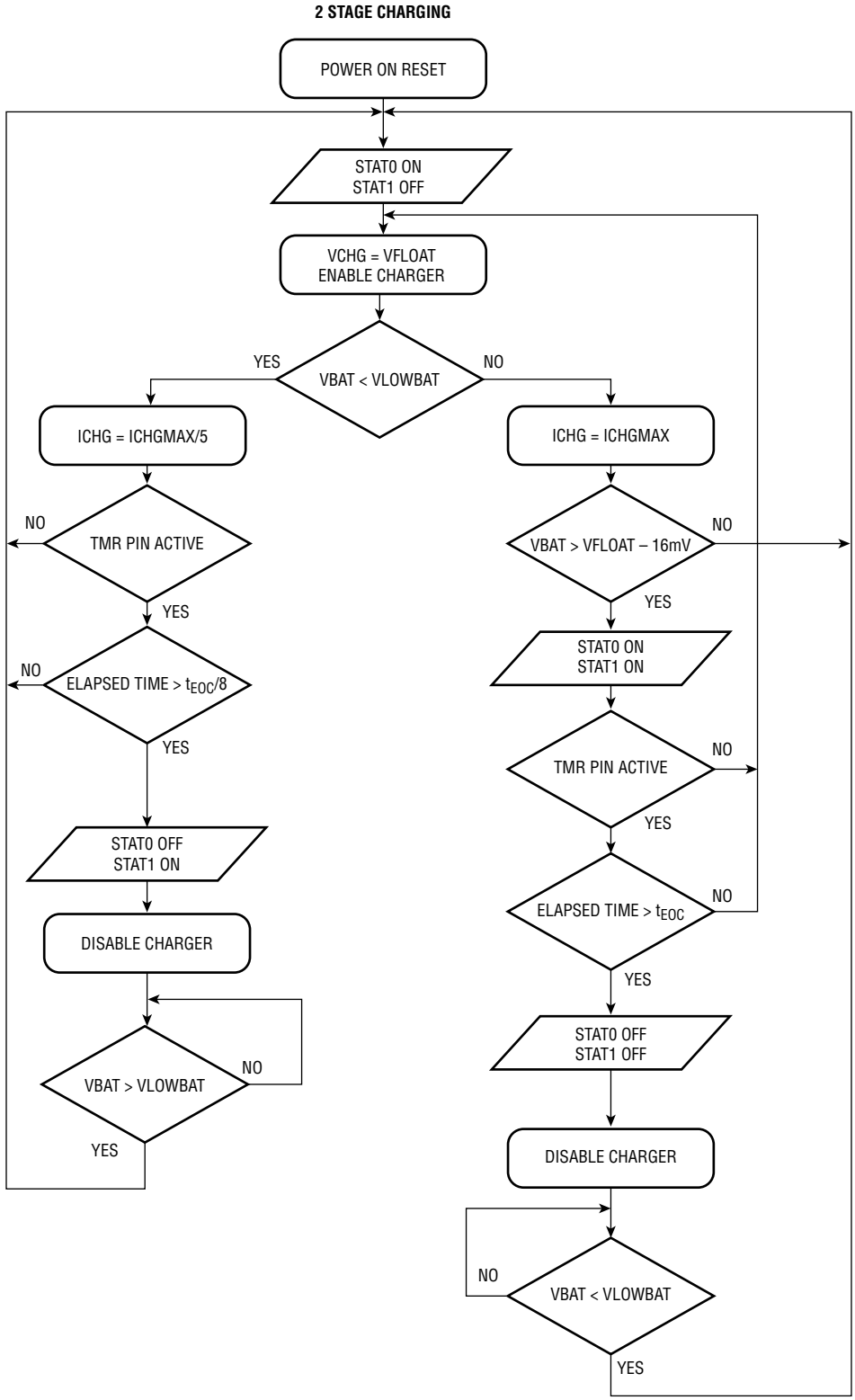


Figure 4. 6 Cell Lead-Acid Charge Voltages with R_{FB1}/R_{FB2} Change

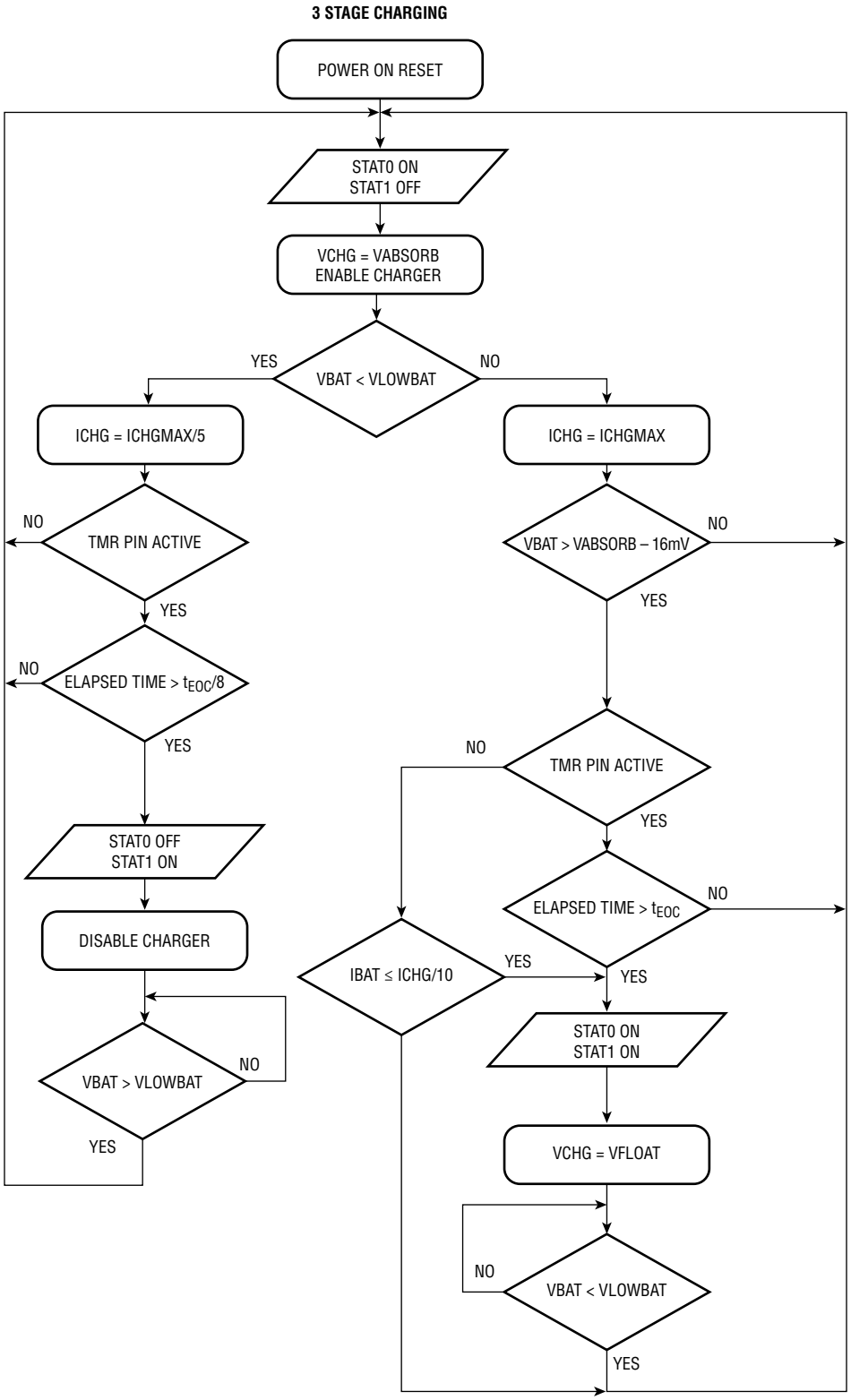
Figure 4 shows the relationship between the float voltage, the absorption and the equalization voltages for a given feedback divider setting.

The following diagrams show the details of each charge algorithm.

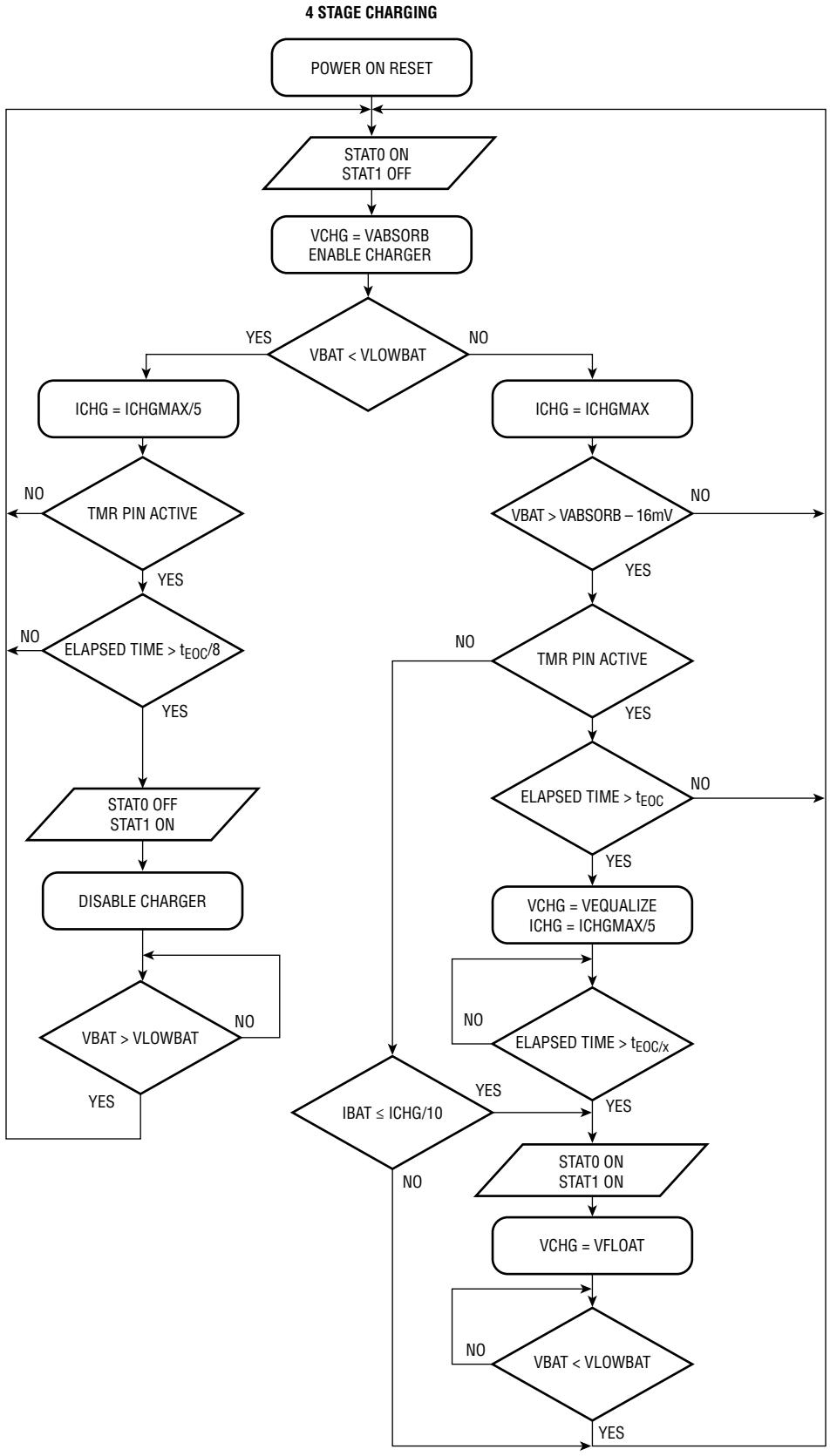
OPERATION


2 STAGE CHARGING
POWER ON RESET
STAT0 ON
STAT1 OFF
VCHG = VFLOAT
ENABLE CHARGER
VBAT < VLOWBAT
YES
NO
ICHG = ICHGMAX/5
ICHG = ICHGMAX
TMR PIN ACTIVE
NO
YES
VBAT > VFLOAT – 16mV
NO
YES
ELAPSED TIME > tEOC/8
NO
YES
STAT0 ON
STAT1 ON
TMR PIN ACTIVE
NO
YES
STAT0 OFF
STAT1 ON
ELAPSED TIME > tEOC
NO
YES
DISABLE CHARGER
STAT0 OFF
STAT1 OFF
VBAT > VLOWBAT
NO
YES
DISABLE CHARGER
NO
VBAT < VLOWBAT
YES

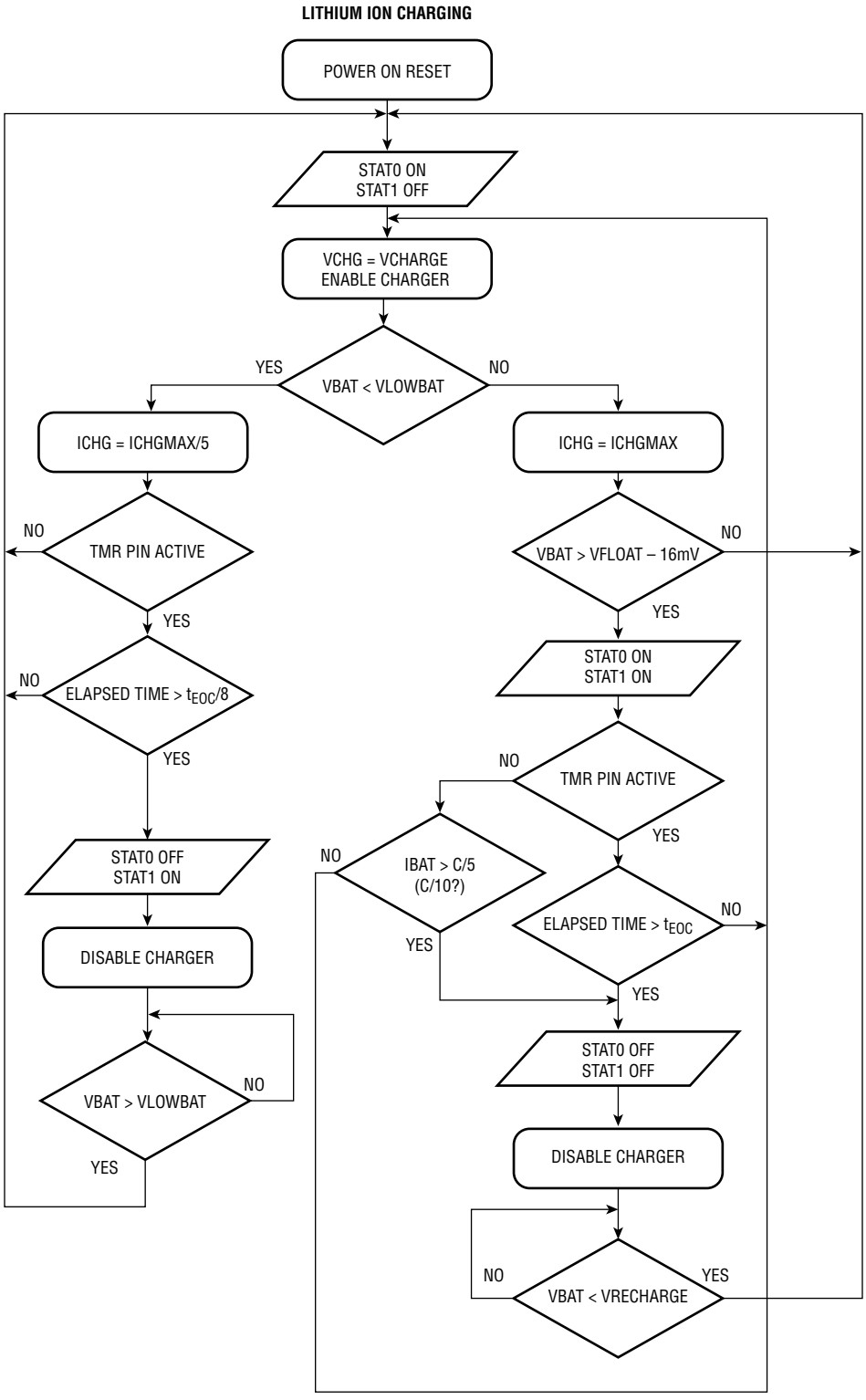
OPERATION


3 STAGE CHARGING
POWER ON RESET
STAT0 ON
STAT1 OFF
VCHG = VABSORB
ENABLE CHARGER
VBAT < VLOWBAT
YES
NO
ICHG = ICHGMAX/5
ICHG = ICHGMAX
TMR PIN ACTIVE
NO
YES
VBAT > VABSORB – 16mV
NO
YES
ELAPSED TIME > tEOC/8
NO
YES
TMR PIN ACTIVE
NO
YES
STAT0 OFF
STAT1 ON
ELAPSED TIME > tEOC
NO
YES
DISABLE CHARGER
IBAT ≤ ICHG/10
YES
YES
STAT0 ON
STAT1 ON
VBAT > VLOWBAT
NO
YES
VCHG = VFLOAT
NO
VBAT < VLOWBAT
YES

OPERATION


4 STAGE CHARGING
POWER ON RESET
STAT0 ON
STAT1 OFF
VCHG = VABSORB
ENABLE CHARGER
VBAT < VLOWBAT
YES
NO
ICHG = ICHGMAX/5
ICHG = ICHGMAX
TMR PIN ACTIVE
NO
YES
VBAT > VABSORB – 16mV
NO
YES
ELAPSED TIME > tEOC/8
NO
YES
TMR PIN ACTIVE
NO
YES
STAT0 OFF
STAT1 ON
ELAPSED TIME > tEOC
NO
YES
DISABLE CHARGER
VCHG = VEQUALIZE
ICHG = ICHGMAX/5
VBAT > VLOWBAT
NO
YES
ELAPSED TIME > tEOC/x
NO
YES
IBAT ≤ ICHG/10
YES
NO
STAT0 ON
STAT1 ON
VCHG = VFLOAT
VBAT < VLOWBAT
NO
YES

OPERATION


LITHIUM ION CHARGING
POWER ON RESET
STAT0 ON
STAT1 OFF
VCHG = VCHARGE
ENABLE CHARGER
VBAT < VLOWBAT
YES
NO
ICHG = ICHGMAX/5
ICHG = ICHGMAX
TMR PIN ACTIVE
NO
YES
VBAT > VFLOAT – 16mV
NO
YES
ELAPSED TIME > tEOC/8
NO
YES
STAT0 ON
STAT1 ON
TMR PIN ACTIVE
NO
YES
STAT0 OFF
STAT1 ON
IBAT > C/5
(C/10?)
NO
YES
ELAPSED TIME > tEOC
NO
YES
DISABLE CHARGER
STAT0 OFF
STAT1 OFF
VBAT > VLOWBAT
NO
YES
DISABLE CHARGER
VBAT < VRECHARGE
NO
YES

OPERATION

Charge Voltage Temperature Compensation

The LTC4013 can use a thermistor to adjust the battery charge voltage as a function of temperature. The change in FB-referred charge voltage from its nominal level is given by ΔV_{FB} = (VNTC - $VINTV_{CC}$/2) • 0.21. Voltages above 3.3V disable the NTC feature. The transfer function, when combined with a thermistor, is stronger than necessary. It is configured this way so that any thermistor can be diluted with a low drift resistor to achieve the desired temperature coefficient. To avoid the 3.3V NTC disable threshold, the LTC4013 requires that the dilution resistor be placed in parallel with the thermistor rather than in series. The bias resistor from $INTV_{CC}$ to NTC should be equal to the parallel combination of the thermistor at 25°C and the dilution resistor.

Figure 5 shows the NTC circuit configuration and Table 3 shows some common temperature coefficient and associated resistor settings using a 10k, ß = 3380K thermistor.

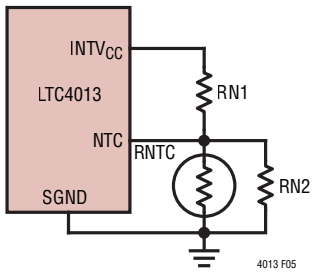


Figure 5. NTC Configuration for Temperature Compensation

Table 3. Charge Voltage TC Examples Using ß = 3380 RNTC

TC (WRT V_{FB})	RN1	RN2
–2.5mV/°C	2.49k	3.32k
–5.0mV/°C	4.99k	10.0k

Figure 6 shows the diluted thermistor voltage vs temperature and Figure 7 shows the resultant charge voltage vs temperature.

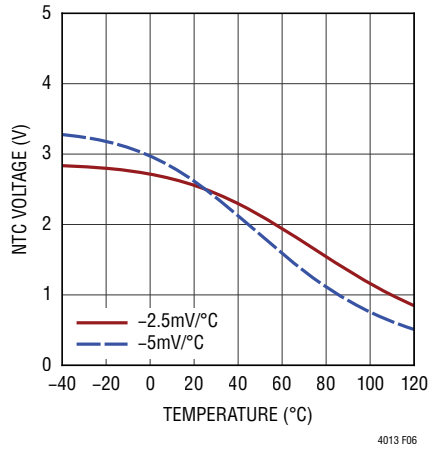


Figure 6. Diluted Thermistor Voltage vs Temperature

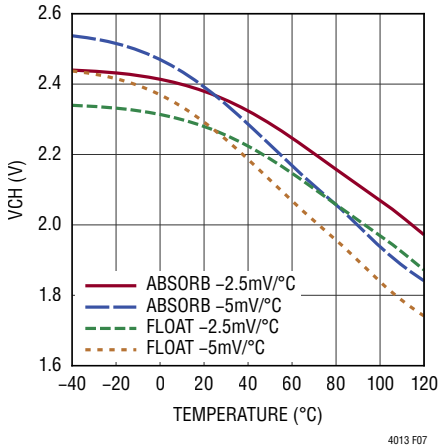


Figure 7. FB-Referred Charge Voltage vs Temperature

Since the thermistor is used to adjust charge voltage vs battery temperature, it is ideally placed in thermal contact with the battery. This is not always practical so the next best thing is to position the resistor to sense the battery's ambient temperature.

Charge Termination Timer

The LTC4013 supports timer-based functions wherein battery charge cycle control occurs after a specific amount of time. Timer termination is engaged when a capacitor (C_{TMR}) is connected from the TMR pin to ground. For a desired end-of-cycle time (t_{EOC}) C_{TMR} follows the relation:

C_{TMR} (µF) = t_{EOC} (Hr) • 0.066

OPERATION

The absorption and Li-Ion termination timer cycles start when the charger transitions from constant-current to constant-voltage charging. Equalization timing starts immediately upon transition to the equalization charge state and low battery timing commences when FB falls below LB.

Low Battery (LB) Pin

The LB pin is used to program the low battery level and is compared internally to the FB pin voltage. The LB pin sources a very precise 20µA current so the threshold voltage can be programmed simply by placing a resistor from LB to ground. For instance, 100k to ground sets the LB pin to 2.0V. In 2-stage and Li-Ion charging a transition below the LB threshold triggers a new charge cycle if terminated. In 3-stage and 4-stage a transition below the LB threshold returns the charger to the absorption charging phase. In all four modes, Li-Ion, 2-stage, 3-stage and 4-stage, and with a timer capacitor present, the low battery fault timer starts and the charge current is reduced to C/5. All four modes terminate charging if the low-battery timer expires.

A commonly used low-battery voltage for a 6 cell battery is 10.4V which represents the voltage with one of 6 cells shorted. This LB voltage is set with an 86.6k resistor for 1.73V/cell, or 10.4V/6 with a 6-to-1 FB divider.

Output Current Monitoring

Charge current can be determined by observing the voltage at the ISMON pin. ISMON follows the expression:

$$ISMON = 20 \bullet (V_{SENSE} - V_{BAT}).$$

Programming Switching Frequency

The LTC4013 has an operational switching frequency range between 200kHz and 1MHz which is programmed with an external resistor from the RT pin to ground. Table 4 shows resistor values and their corresponding switching frequencies. An approximate formula is:

$$R_T(k\Omega) = \frac{40.2}{f_{SW}^{1.088}\ (MHz)}$$

Table 4. R_T Resistor Value

Switching Frequency	R_T (Ω)
1MHz	40.2k
750kHz	54.9k
500kHz	86.6k
300kHz	150k
200kHz	232k

Switching Frequency Synchronization

The internal oscillator may also be synchronized to an external clock through the SYNC pin. The signal applied to the SYNC pin must have a logic low below 1.3V and a logic high above 1.7V. The input sync frequency must be 20% higher than the frequency that would otherwise be determined by the resistor at the RT pin. Input signals outside of these specified parameters cause erratic switching behavior and subharmonic oscillations. When synchronizing to an external clock, be aware that there is a fixed delay from the input clock edge to the edge of the signal at the SW pin. Ground the SYNC pin if synchronization to an external clock is not required.

INFET Behavior

The LTC4013 controls an input N-Channel MOSFET via an on-chip charge pump on INFET. The MOSFET provides a blocking path to prevent battery discharge when the input voltage is below the battery voltage. It also disconnects the input supply from the charger to measure the input voltage with no load for Maximum Power Point Tracking (MPPT).

Undervoltage Lockouts

The INFET charge pump and switching regulator are enabled when all four UVLO comparators are satisfied and the ENAB pin is above its precision enable threshold. Specifically, V_{IN} must be above its absolute threshold of 3.45V, DCIN must be greater than BAT by at least 99mV and must also be within 4mV of V_{IN}. A fourth UVLO requires that the battery voltage at SENSE be above its UVLO level of approximately 1.97V.

OPERATION

If the conditions above are not met then INFET is turned off and sinks current pulling INFET to approximately 2.2V below the lower voltage of DCIN or V_{IN}. If the input voltage is more than the gate breakdown of the external transistor, a TVS diode is required to prevent the disable current or pin leakage from pulling INFET all the way to ground. For MPPT applications requiring two transistors at INFET, a conventional diode will suffice as it will pull down the common source node safely.

Thermal Shutdown

The LTC4013 has thermal shutdown that disables charging at approximately 160°C. When the LTC4013 has cooled to 150°C, charging resumes. Thermal shutdown protects the device from excessive gate drive power and excess internal LDO power dissipation but does not necessarily prevent excess power dissipation in the external MOSFETS or other external components.

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Setting Charge Current

Charge current, I_{CHGMAX}, is determined by the current sense resistor between SENSE and BAT. The servo voltage is 50mV making the charge current 50mV/R_{SENSE}. For a 10A charge current R_{SENSE} should be 5mΩ. Accuracy requires the use of 4-terminal sense resistors or careful attention to ensure a Kelvin connection to the sense resistor. Figure 18 shows two examples. Size the resistor for power dissipation with PR_{SENSE} = I_{CHGMAX} • 50mV. For example, the 10A sense resistor needs to be at least ½Watt. Susumu, Panasonic and Vishay offer a wide variety of accurate sense resistors.

Inductor Selection

Size the inductor so that the peak-to-peak ripple current is approximately 30% of the maximum charging current. This is a reasonable trade-off between inductor size and ripple. Inductance can be computed with the following equation:

$$L = \frac{V_{IN} \bullet V_{BAT} - V_{BAT}^2}{0.3 \bullet f_{SW} \bullet I_{CHGMAX} \bullet V_{IN}}$$

where V_{BAT} is the battery voltage, V_{IN} is the input voltage, I_{CHGMAX} is the maximum charge current and f_{SW} is the switching frequency. Choose the saturation current for the inductor to be at least 20% higher than the maximum charge current.

To protect against faults, there is an overcurrent comparator which terminates switching when the voltage between the SENSE and BAT pins exceeds 100mV. When tripped, switching is stopped for a minimum of 4 switch cycles.

Switching Regulator MOSFET Selection

Key parameters for MOSFET selection are: total gate charge (Q_G), on-resistance ($R_{DS(ON)}$), gate to drain charge (Q_{GD}), gate-to-source charge (Q_{GS}), gate resistance (R_G), breakdown voltage (maximum V_{GS} and V_{DS}) and drain current (maximum I_D). The following guidelines provide information to make the selection process easier. Table 5 lists some recommended manufacturers.

The rated drain current for both MOSFETs must be greater than the maximum inductor current. Peak inductor current is approximately:

$$I_{LMAX} = I_{CHGMAX} + \frac{V_{IN} \bullet V_{BAT} - V_{BAT}^2}{2 \bullet f_{SW} \bullet L \bullet V_{IN}}$$

The rated drain current is temperature dependent, and most data sheets include a table or graph of rated drain current versus temperature.

The rated V_{DS} must be higher than the maximum input voltage (including transients) for both MOSFETs.

The LTC4013 will drive the gates of the switching MOSFETs with about 5V ($INTV_{CC}$) with respect to their sources. However, during start-up and recovery conditions, the gate drive signals may be as low as 3V. Therefore, to ensure that the LTC4013 operates properly, use logic level threshold MOSFETs with a V_T of about 2V or less. For a robust design, ensure that the rated maximum V_{GS} is at least 7V.

Power loss in the switching MOSFETs is related to the on-resistance, $R_{DS(ON)}$; gate resistance, R_G; gate-to-drain charge, Q_{GD} and gate-to-source charge, Q_{GS}. Power lost to the on-resistance is an ohmic loss, $I^2R_{DS(ON)}$, and usually dominates for input voltages less than 15V. Power lost while charging the gate capacitance typically dominates for voltages greater than 15V. When operating at higher input voltages, efficiency is optimized by selecting a high side MOSFET with higher $R_{DS(ON)}$ and lower Q_G. The total power loss in the high side MOSFET is approximated by the sum of ohmic losses and transition losses:

$$P_{HIGH_LOSS} = \frac{V_{BAT}}{V_{IN}} \bullet I_L^2 \bullet R_{DS(ON)} \bullet \rho_T +$$

$$\frac{V_{IN} \bullet I_L}{5V} \bullet (Q_{GD} + Q_{GS}) \bullet (2 \bullet R_G + R_{PU} + R_{PD}) \bullet f_{SW}$$

ρT is a dimensionless temperature dependent factor in the MOSFET's on-resistance. Using 70°C as the maximum ambient operating temperature, ρT is roughly equal to 1.3. RPD and RPU are the LTC4013 high side gate driver output impedances: 2.3Ω and 1.3Ω, respectively.

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For the low side MOSFET the power loss is approximated by:

$$P_{LOW_LOSS} = \left(1 - \frac{V_{BAT}}{V_{IN}}\right) \bullet I_L{}^2 \bullet R_{DS(ON)} \bullet \rho_T +$$

$$\frac{V_{IN} \bullet I_L}{5V} \bullet (Q_{GD} + Q_{GS}) \bullet (2 \bullet R_G + R_{PU} + R_{PD}) \bullet f_{SW}$$

$$+ V_f \bullet 2 \bullet f_{SW} \bullet I_L \bullet tnol$$

Where V_f is the voltage drop of the lower MOSFET bulk diode, typically 0.7V, and tnol is the non-overlap time, approximately 50ns. The last term in this expression represents the loss due to the body diode that is active during the non-overlap time.

In addition to the above requirements, it is desirable for the bottom MOSFET to have lower gate-drain capacitance as it minimizes coupling to BGATE when the SW pin rises. This coupling may momentarily turn on the bottom side MOSFET creating shoot-through that, at best, reduces efficiency and at worst can destroy the MOSFET.

While it is possible to get high and low side MOSFETs bonded in a common package, excessive power dissipation may require two separate packages or even that multiple high or low side MOSFETS be used at the high-power levels. Using multiple packages spreads the heat over a larger PCB area improving overall board temperature and efficiency.

At lower V_{IN}, the top side MOSFET is on longer and low $R_{DS(ON)}$ helps lower dissipation but at higher input voltage the transient losses increase and can dominate. For the bottom side MOSFET the opposite is true. Optimization for best efficiency suggests different top and bottom MOSFETs.

A good approach to MOSFET sizing is to select the high side MOSFET first, then the low side MOSFET. The trade-off between $R_{DS(ON)}$, Q_G, and Q_{GS} for the high side MOSFET is evident in the following example of charging a 6 cell lead-acid battery from a 30V source at 20A. V_{BAT} is equal to 14V, f_{SW} = 200kHz.

For the top side MOSFET the BSC018N04LS is a suitable 40V N-channel MOSFETs with an $R_{DS(ON)}$ of 2.0mΩ at 4.5V, Q_G = 60nC, Q_{GS} = 25nC, Q_{GD} = 10nC, RG = 1.3Ω. The bottom side MOSFET is a BSC093N04LS with an $R_{DS(ON)}$ of 11.0mΩ at 4.5V, Q_G = 8.6nC, Q_{GS} = 4.9nC, Q_{GD} = 2nC, RG = 1.0Ω. Power loss for the MOSFETs is shown in Figures 8 and 9. Observe that the total power loss at 30V is just over 5W for the top switch and about 4W for the bottom switch.

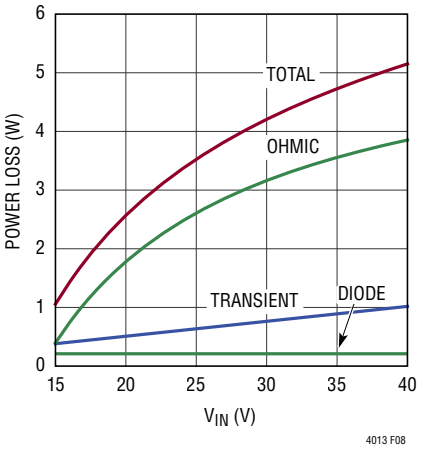

Figure 8. Bottom MOSFET Power Loss Example

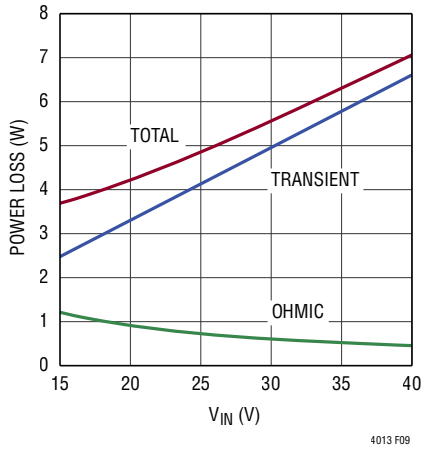

Figure 9. Top MOSFET Power Loss Example

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$R_{DS(ON)}$ and Q_G are inversely related so selecting a top side MOSFET with higher $R_{DS(ON)}$ and lower Q_G might lower top side losses. Conversely the bottom side MOSFET is dominated by ohmic losses so a larger MOSFET may be better if total Q_{GD} is kept to a minimum.

Supplying gate charge current has its own loss and represents a potential limitation at higher voltages, most of which is dissipated from the internal LDO. The power dissipated in the IC is: $P_{LDO}=(V_{IN}-5)\bullet(Q_{GL}+Q_{GH})\bullet f_{SW}$ where Q_{GL} is the low side gate charge and Q_{GH} is the high side gate charge. Figure 10 shows the curve of maximum gate charge current vs input voltage for a power loss of 0.5W. This power level would add 22°C of temperature rise to the die at 43°C/W thermal resistance. Dividing the Y axis value by f_{SW} gives the maximum Q_G that can be charged (the sum of top and bottom gates). For instance, at 30V and 500kHz Q_G is under 20mA/0.5MHz = 40nC.

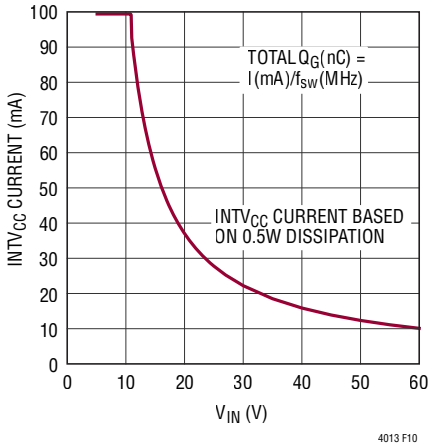

Figure 10. Maximum $INTV_{CC}$ current

If desired operation places the internal 5V regulator out of the allowable region, gate drive power must be supplied externally. This could be done by carefully driving the $INTV_{CC}$ pin with tight regulation to 5.5V (do not exceed the 6V absmax) or by supplying 5V power for the BST drive (top gate Q_G) via the anode of the BST drive diode. Table 5 lists power MOSFET manufacturers that make devices appropriate for LTC4013.

Table 5. Suggested MOSFET Suppliers

Manufacturer	Web Site
Infineon	www.infineon.com
Renesas	www.renesas.com
Fairchild	www.fairchildsemi.com
Vishay	www.vishay.com
NXP/Philips	www.nxp.com

DCIN Capacitance Selection

High quality capacitance is required on DCIN as DCIN provides power to the INFET charge pump and is also used for input voltage sensing. Since most of the switching regulator transients are handled by the V_{IN} capacitor, a smaller capacitor on DCIN is adequate. In fact, DCIN capacitance should be kept low to ensure that the DCIN pin achieves the panel open circuit voltage during the MPPT VOC measurement delay of about 720µs. A maximum 4.7µF high quality ceramic capacitor is recommended.

Input Supply Capacitor Selection

The switching power stage draws high current with fast switching edges, so high quality, low ESR, low ESL decoupling capacitors are required to minimize voltage glitches on the V_{IN} supply. The capacitor(s) must have an adequate ripple current rating. RMS ripple current $I_{VIN(RMS)}$ follows the relation:

$$I_{VIN(RMS)} \approx I_{CHGMAX} \bullet DC \bullet \sqrt{\frac{1}{DC}-1}$$

where I_{CHGMAX} is the maximum charge current set by R_{SENSE}.

$$I_{VIN(RMS)} \approx \frac{I_{CHGMAX}}{2}$$

The required input capacitance C_{IN} is determined by the desired input ripple voltage (ΔV_{IN}):

$$C_{IN} \geq \frac{I_{CHGMAX}}{\Delta V_{IN} \bullet f_{SW}} \bullet \frac{V_{BAT(MAX)}}{V_{IN(MIN)}}$$

where f_{SW} is the operating frequency, $V_{BAT(MAX)}$ is the DC/DC converter maximum output voltage and $V_{IN(MIN)}$

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is the minimum input operating voltage. Keeping ΔV_{IN} below 100mV is a good starting point. As an example, let I_{CHGMAX} = 10A, ΔV_{IN} = 0.1V, f_{SW} = 500k, $V_{BAT(MAX)}$ = 15V, $V_{IN(MIN)}$ = 18V then C_{IN} is greater than 167µF.

Meeting these requirements at higher voltages may require multiple capacitors and possibly a mixture of capacitor types. Because of the fast switching edges it is important that the total decoupling capacitance have low ESR and ESL to avoid sharp voltage spikes. The best practice is to use several low-ESR ceramic capacitors as part of the capacitance, with higher density capacitors utilized for bulk requirements. X7R capacitors tend to maintain their capacitance over a wide range of operating voltages and temperatures. Minimize the loop created by the input capacitor, the high side MOSFET and the low side MOSFET to reduce radiation components. See Linear Technology application notes AN139 and AN144 for more information on EMI.

Battery Capacitor Selection

The output of the charger is the battery which represents a large effective capacitance. Because the battery often has significant wiring connecting it to the charger, additional decoupling output capacitors at the charger are needed. The BAT node is also used for voltage sensing so better performance is obtained with lower voltage ripple at the BAT and FB pins. The BAT capacitor needs to have low ESR to reduce output ripple. To achieve the lowest possible ESR, use several low-ESR ceramic capacitors in parallel. Lower output voltage applications may benefit from the use of high density POSCAP capacitors which are easily destroyed when exposed to over-voltage conditions. To prevent this, select POSCAP capacitors that have a voltage rating that is at least 20% higher than the regulated voltage.

The ripple current on these capacitors is the same as the inductor ripple. Since, in general, inductor selection is chosen to have ripple current equal to or below 30% of I_{CHGMAX}, an adequate ripple current rating for the BAT capacitor(s) is 0.4 • I_{CHGMAX}. The capacitors also need to be surge rated to the maximum output current.

Sizing for output ripple voltage is similar to input decoupling:

$$C_{BAT} \geq \frac{0.4 \bullet I_{CHGMAX}}{\Delta V_{BAT} \bullet f_{SW}}$$

For example, if I_{CHGMAX} = 10A, ΔV_{BAT} = 0.1V, f_{SW} = 500k then choose C_{BAT} greater than 80µF.

$INTV_{CC}$ LDO Output, and BST Supply

$INTV_{CC}$ provides power to the LTC4103 but also provides charge to the gate drives. The boosted supply pin allows the use of an N-channel top MOSFET switch for increased conversion efficiency and lower cost. The BST capacitor is connected from SW to BST with a low leakage 1A Schottky diode connected from $INTV_{CC}$ to BST. The diode must be rated for a reverse voltage greater than the input supply voltage maximum.

C_{BST} is sized to hold the BST rail reasonably constant when delivering gate charge to the MOSFET. A good rule of thumb is:

$$C_{BST} > 50 \bullet \frac{Q_{GH}}{V_{GS}} = 10 \bullet Q_{GH}$$

where Q_{GH} is the top side MOSFET Q_G at 5V.

For example, if the top gate charge is 20nC charged to $INTV_{CC}$ at 5V, then keep the C_{BST} capacitance larger than 0.2µF.

C_{BST} is charged during the bottom switch on time. The LTC4013 maintains a minimum top gate off time to provide this charge. If the LTC4013 is in discontinuous mode with the bottom switch off and the boost voltage drops, the bottom side switch is enabled to provide BST capacitor charging.

Since BST capacitor charge current is drawn from the $INTV_{CC}$ capacitor, C_{BST} needs to be sized to have minimal drop during recharge. A good starting point for high-current MOSFETs with high gate charge is to set C_{INTVCC} larger than 4.7µF. Connect it as close as possible to the exposed pad underneath the package. Because of the fast high-current edges, use a low-ESR ceramic capacitor with ESR typically lower than 20mΩ. For driving MOSFETs with gate charge larger than 44nC, size $INTV_{CC}$ with 0.5µF/nC of total gate charge (top plus bottom MOSFETs).

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Enable (ENAB) Pin

The LTC4013 has an ENAB pin that allows it to be enabled when the input voltage reaches a particular threshold using a resistor divider from DCIN to ENAB (see Figure 11). The turn-on threshold at ENAB is approximately 1.22V (rising), with 170mV of hysteresis. In shutdown, all charging functions are disabled and input supply current is reduced to around 40µA.

Typical ENAB pin input bias current is 10nA which needs to be accounted for when using high value resistors. Choose REN1 and then:

$$R_{EN2} = R_{EN1} \bullet \left(\frac{V_{ENAB}}{1.22} - 1 \right)$$

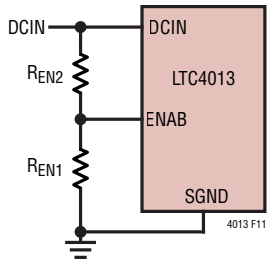

Figure 11. ENAB Resistor Divider

Frequency Compensation

The LTC4013 uses average current mode control for precise regulation of the charge current. Figure 12 shows an overview of the control loop. The current is measured via the sense amplifier and compared against the target value. The error amplifier, in conjunction with compensation components R_C and C_C, sets the duty cycle that controls the inductor current.

Use the following equations to compute the compensation component sizing:

$$R_C = \frac{350V\Omega \bullet f_{SW} \bullet L}{R_{SENSE} \bullet V_{IN}}$$

$$C_C \geq \frac{10}{2\pi \bullet \frac{f_{SW}}{10} \bullet R_C} = \frac{R_{SENSE} \bullet V_{IN}}{22V\Omega \bullet f_{SW}^2 \bullet L}$$

where f_{SW} is the switching frequency, L is the inductance value, V_{IN} is the input voltage and R_{SENSE} is the sense resistor.

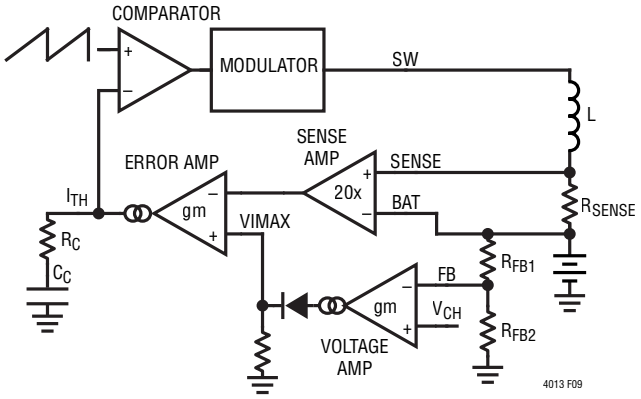

Figure 12. Switching Regulator Control Loop

In some circumstances, an additional roll-off capacitor, C_{C2}, from ITH to ground is helpful. Make $C_{C2} = C_C /100$.

A separate voltage amplifier modulates the maximum current as the battery voltage approaches the charge voltage level. Since the charge voltage regulation loop monitors battery voltage, it is generally controlled by a very slow-moving node. However, the battery ESR, combined with the output capacitance, produces an in-band pole potentially resulting in unstable operation. The voltage regulation loop is compensated by adding a capacitor to the FB input, producing a dominant, low-frequency, pole as shown in Figure 13. The pole frequency, set by the parallel combination of the feedback resistors and the capacitor, is typically set to ~1/1000 of the switching frequency.

$$C_{FB} \geq \frac{200\Omega}{R_{FB2}} \bullet C_{BAT}$$

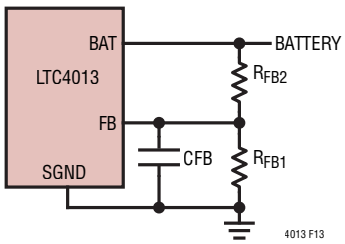

Figure 13. FB Voltage Filtering

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Maximum Power Point Tracking (MPPT)

MPPT is used to regulate the input voltage to maximize power transfer from a power limited source. The first step is to determine the maximum power voltage. For a solar panel, this can be determined from the data sheet. A resistor divider between the input source and the FBOC and MPPT pins is used to program the LTC4013 to regulate the input source at its maximum power voltage. The FBOC pin is used to sample the input source open circuit voltage when charging is paused while the MPPT pin is used to regulate the maximum power voltage when the charger is running. The MPPT resistor divider should be configured as shown in Figure 14.

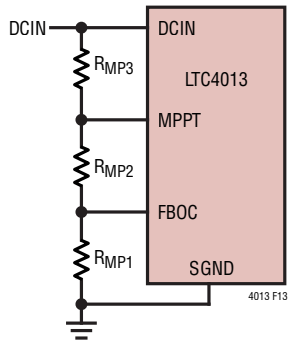

Figure 14. Resistor Divider for MPPT

Choose the attenuation ratio of FBOC to DCIN (K_F) so V_{FBOC} is between 1.0V and 3.0V when the input voltage is at its highest (i.e. open circuit, $V_{DCIN}(OC)$). The attenuation ratio of MPPT to DCIN is set so that VMPPT equals the chosen V_{FBOC} when DCIN is at the maximum power voltage, $V_{DCIN}(MP)$. The following equations define those conditions:

$$\frac{V_{FBOC}}{V_{DCIN(OC)}} = \frac{R_{MP1}}{R_{MP1}+R_{MP2}+R_{MP3}} = K_F$$

$$\frac{V_{MPPT}}{V_{DCIN(MP)}} = \frac{R_{MP1}+R_{MP2}}{R_{MP1}+R_{MP2}+R_{MP3}}$$

When the MPPT loop is in regulation, the MPPT voltage equals the FBOC voltage as measured during the open circuit interval. Reworking the above equations to define the ratio of the DCIN voltage at regulation and open circuit as K_R gives:

$$\frac{V_{DCIN(MP)}}{V_{DCIN(OC)}} = \frac{R_{MP1}}{R_{MP1}+R_{MP2}} = K_R$$

This equation can be written to solve for R_{MP2} as a function of R_{MP1} and the DCIN ratio K_R:

$$R_{MP2} = R_{MP1} \bullet \left(\frac{1}{K_R} - 1\right)$$

Substituting that for R_{MP2} in the equation for K_F and solving for R_{MP3}:

$$R_{MP3} = R_{MP1} \bullet \left(\frac{1}{K_F} - \frac{1}{K_R}\right)$$

The design procedure is:

1. Choose R_{MP1} such that V_{FBOC} = 1.0V to 3.0V. Current in the resistor string of 5µA to 50µA is recommended.
2. Calculate R_{MP2} based on R_{MP1} and the ratio, K_R, between the maximum power voltage and the open circuit voltage.
3. Calculate R_{MP3} based on R_{MP1}, and the K_R and K_F ratios.

As an example, consider a solar panel with an open circuit voltage $V_{DCIN}(OC)$ = 24V and a maximum power voltage $V_{DCIN}(MP)$ = 17V. Choose V_{FBOC} = 1.5V. Then calculate:

$$K_F = \frac{1.5V}{24V} = 0.0625$$

$$K_R = \frac{17V}{24V} = 0.708$$

$$R_{MP1} = \frac{1.5V}{30\mu A} = 50k \text{ (Choose 30µA in Divider)}$$

$$R_{MP2} = 50k \bullet \left(\frac{1}{0.708} - 1\right) = 20.6k$$

$$R_{MP3} = 50k \bullet \left(\frac{1}{0.0625} - \frac{1}{0.708}\right) = 729k$$

As another example, consider charging a battery from a source with an open-circuit voltage of 30V and a source impedance of 5Ω. This resistive supply has a short circuit

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current of 6A, and the peak available power of 45W occurs with a load of 3A at 50% of VOC. MPPT settings would have $V_{DCIN}(OC)$ = 30V, V_{FBOC} = 1.5V,

$$K_F = \frac{V_{FBOC}}{V_{DCIN(OC)}} = \frac{1.5V}{30V} = 0.05$$

$$K_R = \frac{V_{DCIN(MP)}}{V_{DCIN(OC)}} = \frac{15V}{30V} = 0.5$$

Again with 30µA in R_{MP1}, R_{MP1} = 50k then

$$R_{MP2} = 50k \bullet \left(\frac{1}{0.5} - 1 \right) = 50k \text{ and}$$

$$R_{MP3} = 50k \bullet \left(\frac{1}{0.05} - \frac{1}{0.5} \right) = 900k$$

If the MPPT function is not needed, it can be disabled by tying FBOC to $INTV_{CC}$.

Additional MPPT Considerations

MPPT operation requires the use of back-to-back MOSFETs for the input PowerPath to allow open circuit DCIN voltage measurement. When using back-to-back MOSFETs the sources are tied together, drains on the outside. A single MOSFET cannot be used because the body diode clamps DCIN to V_{IN} when the input MOSFET is off, resulting in incorrect measurement of the DCIN open circuit voltage.

Because MPPT operation involves large changes in input voltage, ensure that the programmed maximum power voltage is greater than both 4.5V and is at least 100mV above the battery voltage.

A lead capacitor, C_{MPPT}, from DCIN to MPPT can compensate the input voltage regulation loop during MPPT operation.

Battery Stacks

Batteries are often stacked serially to increase voltage and reduce current. The LTC4013 charges voltage stacks of up to 60V. However, when stacking cells or a battery of cells, cell/battery balancing should be employed. Omitting cell balancing can quickly result in a degenerate scenario of rapidly diverging cell voltages with possible cell failure over several charge-discharge cycles.

Plugging in a Battery

Care must be taken when hot plugging a battery into the charging circuit. Discharged capacitors can cause very high battery discharge current as the battery voltage and the capacitor voltage equalize. Figure 15 shows the current path which has very little series impedance between the battery and capacitor.

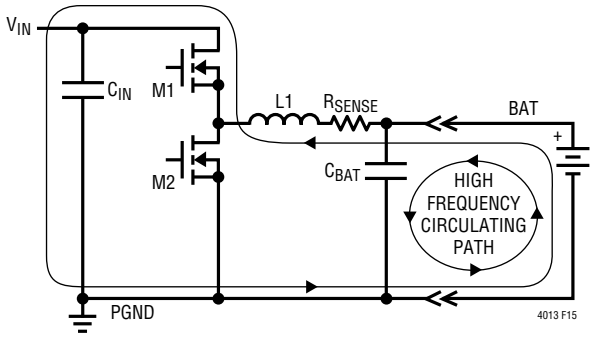

Figure 15. Current Flow During Hot Plugging of Battery

As with other hot-swap issues, the first step is to reduce capacitance. It is also possible to partially precharge the capacitors using power from V_{IN}. However, this must be done carefully to avoid a direct current path from the battery back to the input supply. Any application circuit must be bidirectional to support battery charging through a low impedance path while controlling the reverse current during a hot plug event. See ideal diode application circuit, Figure 19.

System Load During Charging

If there is a system load on the battery when charging it can interfere with the charging algorithms. For instance, if the load is greater than I_{CHGMAX}/10 the charger might not detect an end of charge condition. Careful management of the load can help. Current is monitored through the sense resistor and reported on ISMON so it may be possible to use this signal to help detect charge algorithm problems.

Starting Without a Battery

The LTC4013 requires the SENSE voltage to be above 1.97V to run. This ensures that the SENSE amplifier has sufficient headroom to operate. Normally this requirement

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is met if a battery is present. There are conditions where this may not be met, such as testing without a battery. For the switching regulator to start, the voltage on SENSE needs to be pulled up. A simple method is shown in Figure 16. In this case a few milliamperes of current are taken from $INTV_{CC}$ and used to charge the capacitance on BAT. Once SENSE is above its UVLO threshold, the switching regulator will turn on and will charge the node at higher currents, typically C/5 for battery voltages below LB. Once the battery voltage is above 4.3V, there is no longer a drain on $INTV_{CC}$.

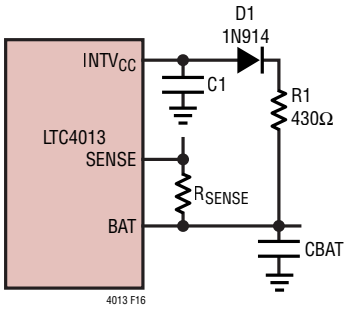

Figure 16. SENSE Precharge

INFET Mosfet(s)

Input N-channel MOSFETs are needed for blocking battery discharge when the input is below the battery as well as for decoupling DCIN from V_{IN} for open circuit panel voltage measurement during MPPT. MPPT operation requires back-to-back MOSFETs but if MPPT is not employed then a single MOSFET can be used with the source on the DCIN side. If a single MOSFET is used then V_{IN} is charged up initially through the body diode of the MOSFET. Pick MOSFETs with low $R_{DS(ON)}$ as they conduct all charger current and select breakdown voltage to stand off maximum supply voltage.

Layout Considerations

A general switching regulator layout overview is found in Linear Technology application notes, AN-136, AN-139 and AN-144.

For high current applications, current path traces need to meet current density guidelines as well as having minimal IR drops. There will also be substantial switching transients. The switch drivers on the LTC4013 are designed to drive large capacitances and generate significant transient currents. Carefully consider supply bypass capacitor locations to avoid corrupting the signal ground reference (SGND) used by the IC.

Keep the high-frequency circulation path area as shown in Figure 17 minimized and avoid sharing that path with SGND as sensitive circuits like the error amplifier and voltage reference are referred to SGND.

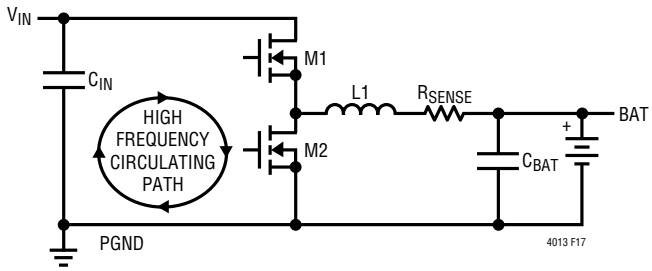

Figure 17. High-Frequency Radiation Path

Effective grounding is achieved by considering switch current in the ground plane and the return current paths of each respective bypass capacitor and power transistor. The V_{IN} bypass return, $INTV_{CC}$ bypass return, and the sources of the ground-referred switch FETs carry PGND currents. SGND originates at the negative terminal of the BAT bypass capacitor and is the small signal reference for the LTC4013. Do not run small traces to separate ground paths. A solid ground plane is crucial.

During the dead-time between the synchronous bottom switch and top switch conduction, the body diode of the synchronous MOSFET conducts the inductor current. Commutating the body diode of this MOSFET requires a significant charge contribution from the top switch during initiation, creating a current spike in the top switch. At the instant the body diode commutates, a current discontinuity is created between the inductor and top switch, with parasitic inductance causing the switch node to transition in response to this discontinuity. High current and excessive parasitic inductance can generate extremely high dv/dt during this transition. This high dv/dt transition can sometimes cause avalanche breakdown in the synchronous MOSFET, generating shoot-through

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current via parasitic turn-on of the synchronous MOSFET. Layout practice and component orientation that minimizes parasitic inductance on the switched nodes are critical for reducing these effects.

When the bottom side MOSFET is turned off, gate drive currents return to the LTC4013 PGND pin from the MOSFET source. The BST supply refresh surge current also returns through this same path. Orient the MOSFET such that the PGND return current does not corrupt the SGND reference.

The high di/dt loop formed by the switch MOSFETs and the input capacitor (C_{VIN}) should have short, wide traces to minimize high-frequency noise and voltage stress from inductive ringing. Surface mount components are necessary to reduce parasitic inductance from component leads. Switch path current can be controlled by orienting the power FETs and the input decoupling capacitors near each other. Locate the $INTV_{CC}$, and BST capacitors near the LTC4013. These capacitors carry the MOSFET gate drive currents. Locate the small-signal components away from high-frequency switching nodes (TG, BG, SW and BST). High current switching nodes are oriented across the top of the LTC4013 package to simplify layout.

Locate the battery charger feedback resistors and MPPT resistors near the LTC4013 and minimize the length of the high impedance feedback nodes.

Route the SENSE and BAT traces together, keeping them as short as possible, and avoid corruption of these lines by high current and hi dv/dt switching nodes.

The LTC4013 packaging has been designed to efficiently remove heat from the IC via the exposed backside pad. Solder the pad to a footprint that contains muiltiple vias to the ground plane. This reduces both the electrical ground resistance and thermal resistance.

Accurate sensing of charge current is dependent on good printed circuit board layout as shown in Figure 18. 4 terminal sense resistors are the best option but it is possible to get good results with 2 terminal devices.

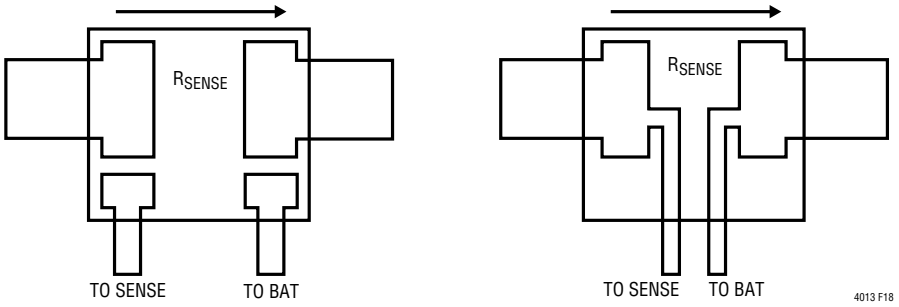

Figure 18. Sense Resistor PCB Layout

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Figure 19. Ideal Diode to Block Current Surge When Hot Plugging Battery

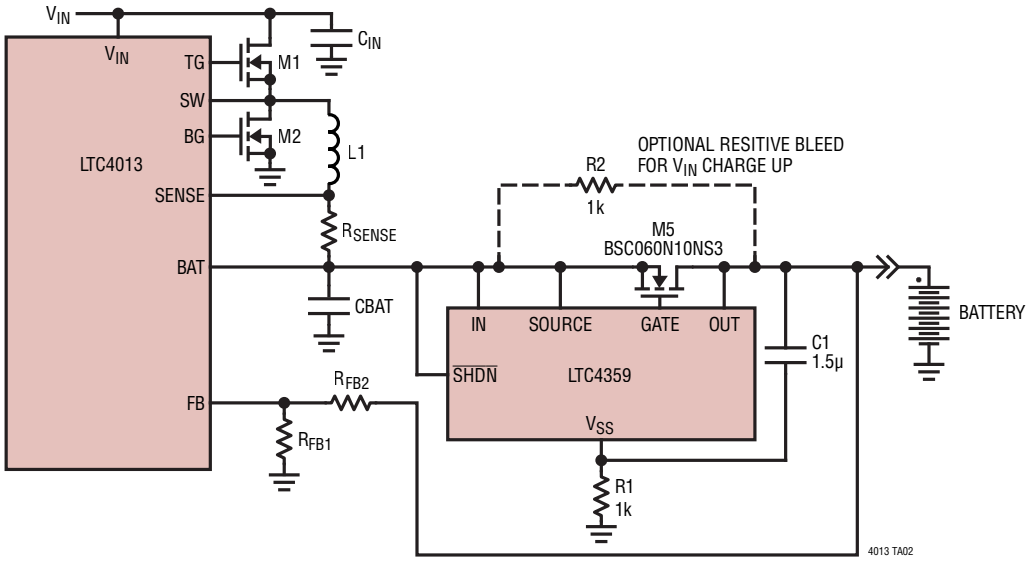

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Figure 20. 6 Cell, 5A Lead Acid Charger with 24V Solar Panel Input and MPPT Optimization

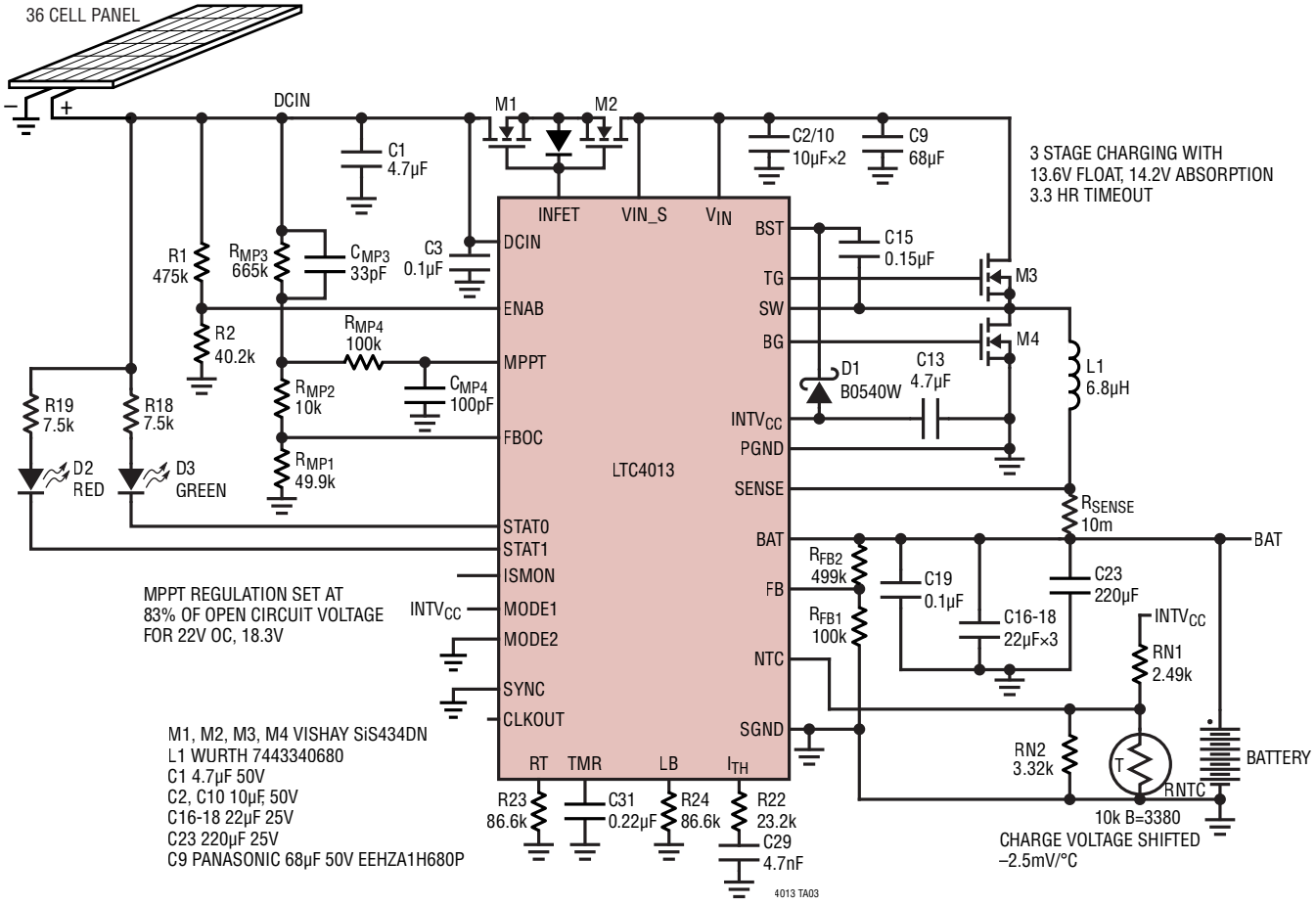

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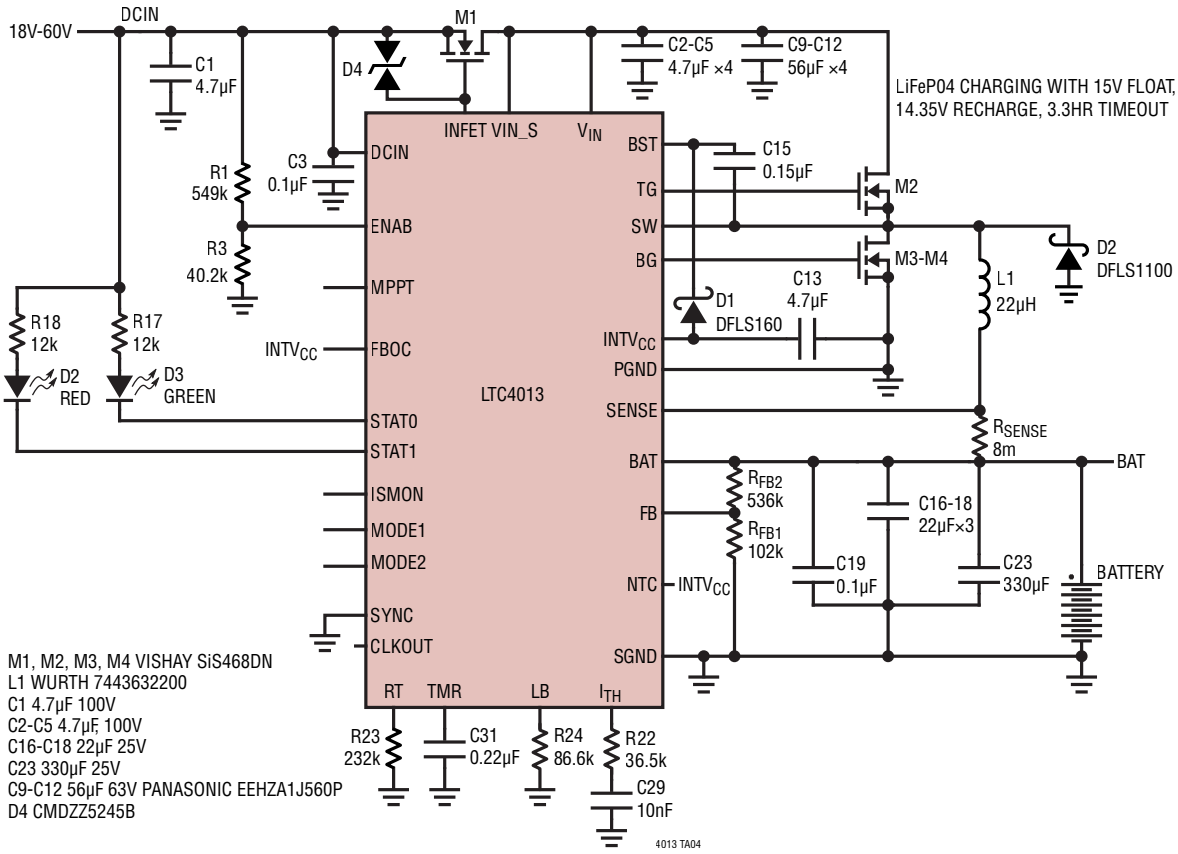
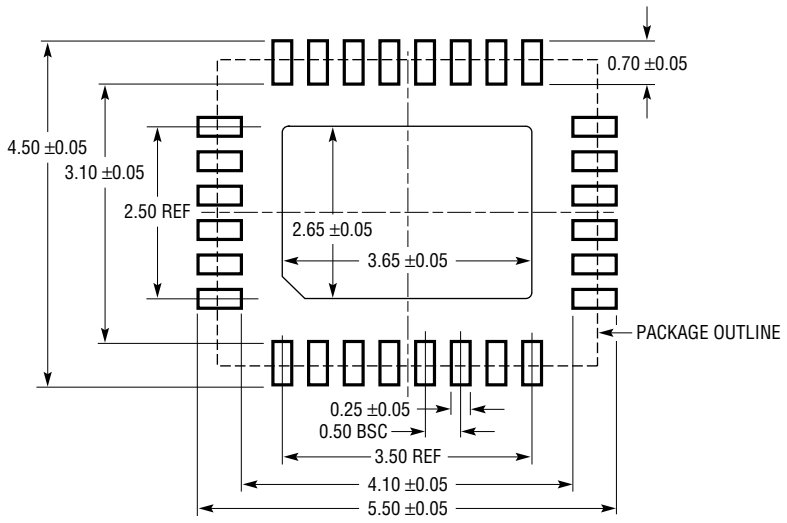
Figure 21. 18V-60V 6.25A LiFePO$_4$ 15V SLA Replacement Battery Charger



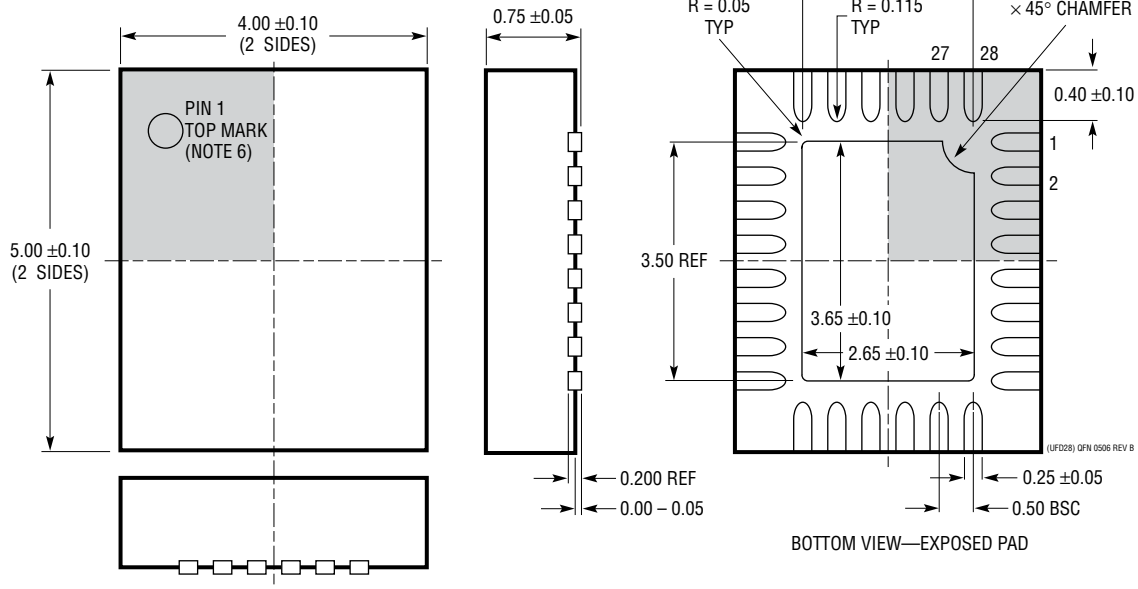
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4013#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

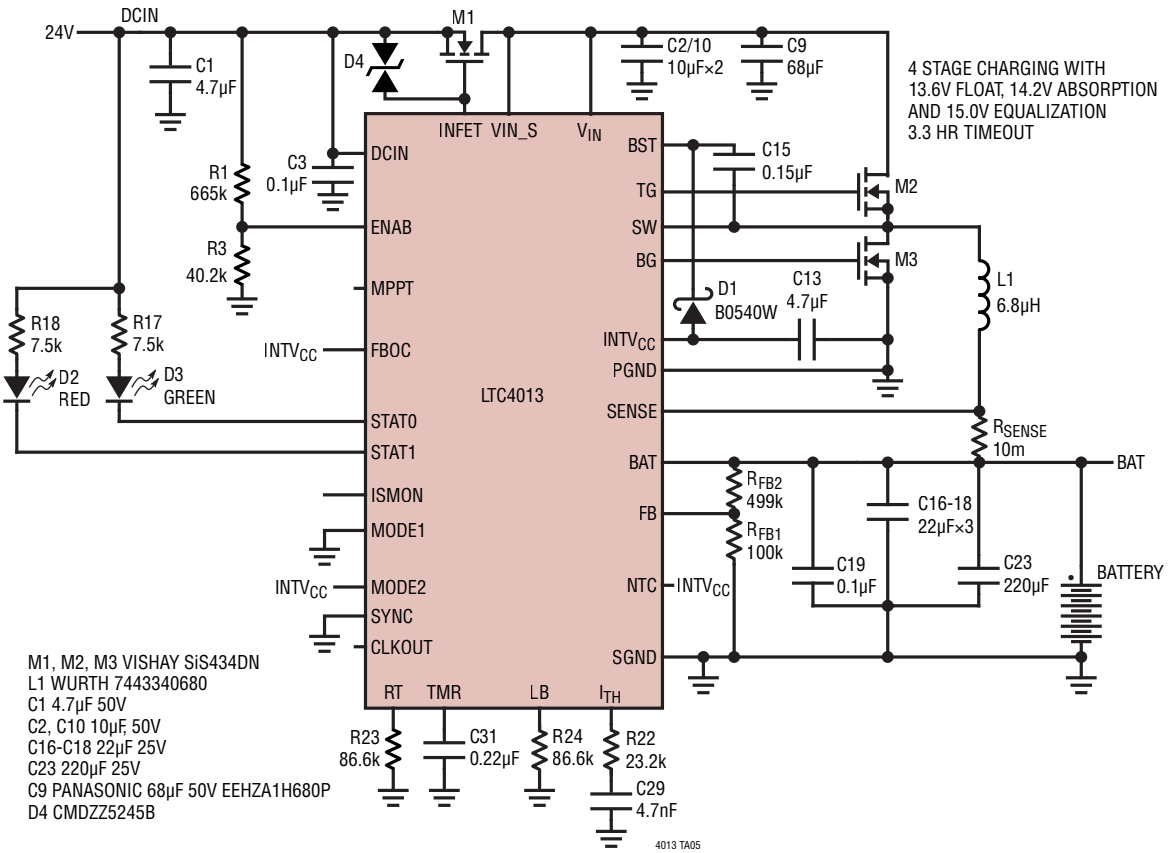
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/18	Added min value to Battery Voltage Range (BAT) spec	3
		Segregated Charger State Diagram by Mode	17-20
		Clarified Device Operation	1-38

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Figure 22. 24V 5A 6 Cell Lead Acid Charger with Absorption and Equalization Charging



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4020	55V Buck-Boost Multi-Chemistry Battery Charger	Li-Ion and Lead Acid Charge Algorithms
LTC4000/LTC4000-1	High Voltage High Current Controller for Battery Charging	3V to 60V Input and Output Voltage. Pair with a DC/DC Converter. LTC4000- 1 Has MPPT
LTC4015	Multichemistry Buck Battery Charger Controller with Digital Telemetry System	4.5V to 35V Synchronous Buck Battery Charger with Multiple System Monitors and Coulomb Counter
LTC3305	Lead Acid Battery Balancer	Balance up to Four 12V Lead Acid Batteries in Series. Stand Alone Operation
LT8710	Synchronous SEPIC/ Inverting/Boost Controller with Output Current Control	2, 3-Stage Lead Acid Charger with C/10 Termination
LT3652/LTC3652HV	2A Battery Charger with Power Tracking	Multi-Chemistry, Onboard Termination, Input Supply Voltage Regulation Loop for Peak Power Tracking. 4.95V to 34V input Up to 2A Charger Current.
LT3651-4.x/LT3651-8.x	Monolithic 4A Switch Mode Synchronous Li-Ion Battery Charger	Standalone, 4.75V ≤ V_{IN} ≤ 32V (40V Abs Max), 4A, Programmable Charge Current Timer or C/10 Termination
LT8490	High Voltage High Current Buck-Boost Controller Battery Charger	6V to 80V Input and Output Voltage. Single Inductor. MPPT

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