SN65LVDS301 Programmable 27-Bit Parallel-to-Serial Transmitter

1 Features

- FlatLink™3G serial interface technology
- Compatible with FlatLink3G receivers such as SN65LVDS302
- Input supports 24-bit RGB video mode interface
- 24-Bit RGB data, 3 control bits, 1 parity bit and 2 reserved bits transmitted over 1, 2 or 3 differential lines
- SubLVDS differential voltage levels
- Effective data throughput up to 1755 Mbps
- Three operating modes to conserve power
  - Active-mode QVGA 17.4 mW (typ)
  - Active-mode VGA 28.8 mW (typ)
  - Shutdown mode 0.5 µA (typ)
  - Standby mode 0.5 µA (typ)
- Bus swap for increased PCB layout flexibility
- 1.8-V supply voltage
- ESD rating > 2 kV (HBM)
- Pixel clock range of 4 MHz–65 MHz
- Failsafe on all CMOS inputs
- Packaging: 80 pin 5mm × 5mm nFBGA®
- Very low EMI meets SAE J1752/3 'M'-spec

2 Applications

- Wearables (non-medical)
- Tablets
- Mobile phones
- Portable electronics
- Gaming
- Retail automation & payment
- Building automation

3 Description

The SN65LVDS301 serializer device converts 27 parallel data inputs to 1, 2, or 3 Sub Low-Voltage Differential Signaling (SubLVDS) serial outputs. It loads a shift register with 24 pixel bits and 3 control bits from the parallel CMOS input interface. In addition to the 27 data bits, the device adds a parity bit and two reserved bits into a 30-bit data word. Each word is latched into the device by the pixel clock (PCLK). The parity bit (odd parity) allows a receiver to detect single bit errors. The serial shift register is uploaded at 30, 15, or 10 times the pixel-clock data rate depending on the number of serial links used. A copy of the pixel clock is output on a separate differential output.

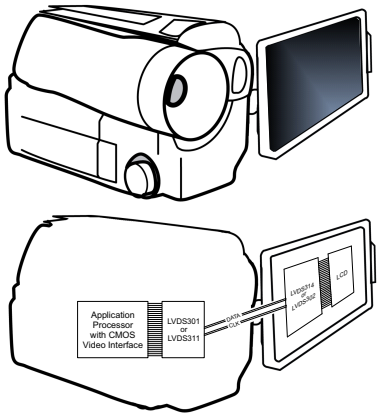
FPC cabling typically interconnects the SN65LVDS301 with the display. Compared to parallel signaling, the LVDS301 outputs significantly reduce the EMI of the interconnect by over 20 dB. The electromagnetic emission of the device itself is very low and meets the meets SAE J1752/3 'M'-spec. (see Figure 6-22)

The SN65LVDS301 is characterized for operation over ambient air temperatures of –40°C to 85°C. All CMOS inputs offer failsafe features to protect them from damage during power-up and to avoid current flow into the device inputs during power-up. An input voltage of up to 2.165 V can be applied to all CMOS inputs while V_{DD} is between 0V and 1.65V.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS301	nFBGA (80)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2012) to Revision E (October 2020)	Page
• NOTE: The device in the MicroStar Jr. BGA packaging were redesigned using a laminate nFBGA package. This nFBGA package offers datasheet-equivalent electrical performance. It is also footprint equivalent to the MicroStar Jr. BGA. The new package designator in place of the discontinued package designator will be updated throughout the datasheet	1
• Changed u*jr ZQE to nFBGA ZXH	1
• Changed u*jr ZQE to nFBGA ZXH	3
• Changed u*jr ZQE to nFBGA ZXH, updated thermal information	5
• Added overview	22

5 Pin Configuration and Functions

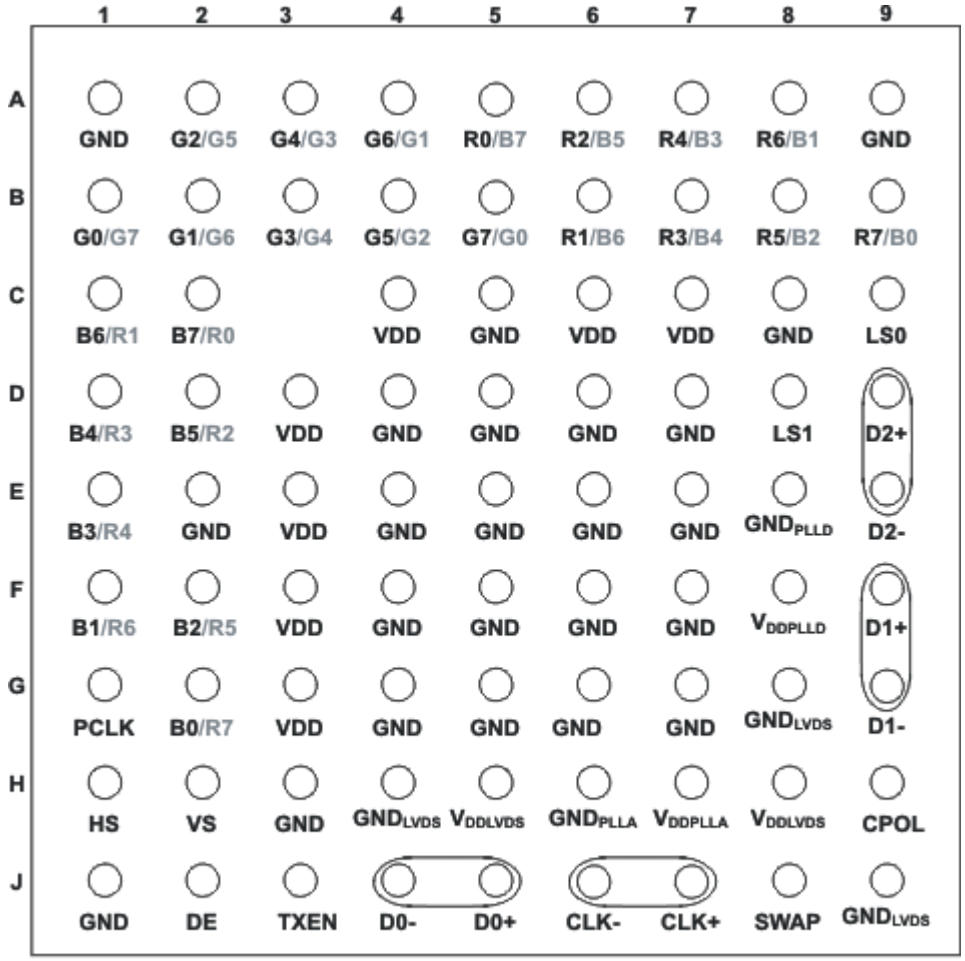


Figure 5-1. 80-Ball ZXH (Top View)

Pin Functions

NAME	PIN	I/O	DESCRIPTION
D0+, D0–	J5, J4	SubLVDS Out	SubLVDS Data Link (active during normal operation)
D1+, D1–	F9, G9		SubLVDS Data Link (active during normal operation when LS0 = high and LS1 = low, or LS0 = low and LS1=high; high impedance if LS0 = LS1 = low)
D2+, D2–	D9, E9		SubLVDS Data Link (active during normal operation when LS0 = low and LS1 = high, high-impedance when LS1 = low)
CLK+, CLK–	J7, J6		SubLVDS output Clock; clock polarity is fixed

Pin Functions (continued)

NAME	PIN	I/O	DESCRIPTION
R0–R7	A5/C2, B6/C1, A6/D2, B7/D1, A7/E1, B8/F2, A8/F1, B9/G2	CMOS IN	Red Pixel Data (8); pin assignment depends on SWAP pin setting
G0–G7	B1/B5, B2/A4, A2/B4, B3/A3, A3/B3, B4/A2, A4/B2, B5/B1		Green Pixel Data (8); pin assignment depends on SWAP pin setting
B0–B7	B9/G2, A8/F1, B8/F2, A7/E1, B7/D1, A6/D2, B6/C1, A5/C2		Blue Pixel Data (8); pin assignment depends on SWAP pin setting
HS	H1		Horizontal Sync
VS	H2		Vertical Sync
DE	J2		Data Enable
PCLK	G1		Input Pixel Clock; rising or falling clock polarity is selected by control input CPOL
LS0, LS1	C9, D8		Link Select (Determines active SubLVDS Data Links and PLL Range) See Table 8-2
TXEN	J3		Disables the CMOS Drivers and Turns Off the PLL, putting device in shutdown mode 1 – Transmitter enabled 0 – Transmitter disabled (Shutdown) Note: The TXEN input incorporates glitch-suppression logic to avoid device malfunction on short input spikes. It is necessary to pull TXEN high for longer than 10 µs to enable the transmitter. It is necessary to pull the TXEN input low for longer than 10 µs to disable the transmitter. At power up, the transmitter is enabled immediately if TXEN = 1 and disabled if TXEN = 0
CPOL	H9	CMOS In	Input Clock Polarity Selection 0 – rising edge clocking 1 – falling edge clocking
SWAP	J8	CMOS In	Bus Swap swaps the bus pins to allow device placement on top or bottom of pcb. See pinout drawing for pin assignments. 0 – data input from B0...R7 1 – data input from R7...B0
V_{DD}	C4	Power Supply(1)	Supply Voltage
GND	A1, A9, C5, C8, D4, D5, D6, D7, E2, E4, E5, E6, E7, F4, F5, F6, F7, G4, G5, G6, G7, H3, J1		Supply Ground
V_{DDLVDS}	H5, H8		SubLVDS I/O supply Voltage
GND_{LVDS}	G8, H4		SubLVDS Ground
V_{DDPLLA}	H7		PLL analog supply Voltage
GND_{PLLA}	H6		PLL analog GND
V_{DDPLLD}	F8		PLL digital supply Voltage
GND_{PLLD}	E8		PLL digital GND

(1) For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

6 Specifications

6.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage range, V_{DD} (2), V_{DDPLLA}, V_{DDPLLD}, V_{DDLVDS}		-0.3 to 2.175	V
Voltage range at any input or output terminal	When V_{DDx} > 0 V	-0.5 to 2.175	V
	When V_{DDx} ≤ 0 V	-0.5 to V_{DD} + 2.175	V
Electrostatic discharge	Human Body Model(3) (all Pins)	±3	kV
	Charged-Device Mode(4)l (all Pins)	±500	V
	Machine Model(5) (all pins)	±200	
Continuous power dissipation		See Dissipation Rating Table	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminals.
(3) In accordance with JEDEC Standard 22, Test Method A114-A.
(4) In accordance with JEDEC Standard 22, Test Method C101.
(5) In accordance with JEDEC Standard 22, Test Method A115-A

6.2 Thermal Information

THERMAL METRIC(1)		SN65LVDS301 ZXH (nFBGA) 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.3 Recommended Operating Conditions (1)

			MIN	NOM	MAX	UNIT
V_{DD} V_{DDPLLA} V_{DDPLLD} V_{DDLVDS}	Supply voltages		1.65	1.8	1.95	V
$V_{DDn(PP)}$	Supply voltage noise magnitude (all supplies)	Test set-up see Figure 7-5				mV
		f(PCLK) ≤ 50 MHz; f(noise) = 1 Hz to 2 GHz			100	
		f(PCLK) > 50 MHz; f(noise) = 1 Hz to 1 MHz			100	
		f(PCLK) > 50 MHz; f(noise) > 1 MHz			40	
f_{PCLK}	Pixel clock frequency	1-Channel transmit mode, see Figure 8-4	4		15	MHz
		2-Channel transmit mode, see Figure 8-5	8		30	
		3-Channel transmit mode, see Figure 8-6	20		65	
		Frequency threshold Standby mode to active mode(2), see Figure 7-9	0.5		3	
t_H x f_{PCLK}	PCLK input duty cycle		0.33		0.67	
T_A	Operating free-air temperature		–40		85	°C
$t_{jit(per)PCLK}$	PCLK RMS period jitter(3)	Measured on PCLK input			5	ps-rms
$t_{jit(TJ)PCLK}$	PCLK total jitter				$0.05/f_{PCLK}$	s
$t_{jit(CC)PCLK}$	PCLK peak cycle-to-cycle jitter(4)				$0.02/f_{PCLK}$	s
PCLK, R[0:7], G[0:7], B[0:7], VS, HS, DE, PCLK, LS[1:0], CPOL, TXEN, SWAP						
V_{IH}	High-level input voltage		$0.7×V_{DD}$		V_{DD}	V
V_{IL}	Low-level input voltage				$0.3×V_{DD}$	V
t_{DS}	Data set up time prior to PCLK transition	f (PCLK) = 65 MHz; see Figure 7-1	2.0			ns
t_{DH}	Data hold time after PCLK transition		2.0			ns

(1) Unused single-ended inputs must be held high or low to prevent them from floating.
(2) PCLK input frequencies lower than 500 kHz force the SN65LVDS301into standby mode. Input frequencies between 500 kHz and 3 MHz may or may not activate the SN65LVDS301. Input frequencies beyond 3 MHz activate the SN65LVDS301.
(3) Period jitter is the deviation in cycle time of a signal with respect to the ideal period over a random sample of 100,000 cycles.
(4) Cycle-to-cycle jitter is the variation in cycle time of a signal between adjacent cycles; over a random sample of 1,000 adjacent cycle pairs.

6.4 Device Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
I_{DD}	1ChM	V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(CLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at V_{DD}, alternating 1010 serial bit pattern	f_{PCLK} = 4 MHz		9.0	11.4	mA
			f_{PCLK} = 6 MHz		10.6	12.6	
			f_{PCLK} = 15 MHz		16	18.8	
		V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at V_{DD}, typical power test pattern (see Table 7-2)	f_{PCLK} = 4 MHz		8.0		mA
			f_{PCLK} = 6 MHz		8.9		
			f_{PCLK} = 15 MHz		14.0		
	2ChM	V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(CLK)}$=$R_{L(Dx)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at V_{DD}, alternating 1010 serial bit pattern;	f_{PCLK} = 8 MHz		13.7	15.9	mA
			f_{PCLK} = 22 MHz		18.4	22.0	
			f_{PCLK} = 30 MHz		21.4	25.8	
		V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at V_{DD}, typical power test pattern (see Table 7-3)	f_{PCLK} = 8 MHz		11.5		mA
			f_{PCLK} = 22 MHz		16.0		
			f_{PCLK} = 30 MHz		19.1		
	3ChM	V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at V_{DD}, alternating 1010 serial bit pattern	f_{PCLK} = 20 MHz		20.0	22.5	mA
			f_{PCLK} = 65 MHz		29.1	36.8	
		V_{DD} =V_{DDPLLA}=V_{DDPLLD}=V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, TXEN at V_{DD}, typical power test pattern (see Table 7-4)	f_{PCLK} = 20 MHz		15.9		mA
			f_{PCLK} = 65 MHz		24.7		
	Standby Mode		V_{DD} = V_{DDPLLA} = V_{DDPLLD} = V_{DDLVDS}, $R_{L(PCLK)}$=$R_{L(D0)}$=100 Ω, V_{IH}=V_{DD}, V_{IL}=0 V, all inputs held static high or static low		0.61	10	µA
	Shutdown Mode				0.55	10	µA

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.

6.5 Output Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
subLVDS output (D0+, D0–, D1+, D1–, D2+, D1–, CLK+, and CLK–)						
$V_{OCM(SS)}$	Steady-state common-mode output voltage	Output load see Figure 7-3	0.8	0.9	1.0	V
$V_{OCM(SS)}$	Change in steady-state common-mode output voltage		–10		10	mV
$V_{OCM(PP)}$	Peak-to-peak common mode output voltage				75	mV
$\|V_{OD}\|$	Differential output voltage magnitude $\|V_{Dx+} - V_{Dx-}\|$, $\|V_{CLK+} - V_{CLK-}\|$		100	150	200	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage between logic states		–10		10	mV
$Z_{OD(CLK)}$	Differential small-signal output impedance	TXEN at V_{DD}		210		Ω
I_{OSD}	Differential short-circuit output current	V_{OD} = 0 V, f_{PCLK} = 28 MHz			10	mA
I_{OS}	Short circuit output current(2)	V_O = 0 V or V_{DD}		5		
I_{OZ}	High-impedance state output current	V_O = 0 V or V_{DD}(max), TXEN at GND	–3		3	µA

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.
(2) All SN65LVDS301 outputs tolerate shorts to GND or V_{DD} without permanent device damage.

6.6 Input Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
PCLK, R[0:7], G[0:7], B[0:7], VS, HS, DE, PCLK, LS[1:0], CPOL, TXEN, SWAP						
I_{IH}	High-level input current	V_{IN} = 0.7 × V_{DD}	–200		200	nA
I_{IL}	Low-level input current	V_{IN} = 0.3 × V_{DD}	–200		200	
C_{IN}	Input capacitance			1.5		pF

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.

6.7 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_r	20%-to-80% differential output signal rise time	See Figure 7-2 and Figure 7-3		250		500	ps
t_f	20%-to-80% differential output signal fall time	See Figure 7-2 and Figure 7-3		250		500	
f_{BW}	PLL bandwidth (3dB cutoff frequency)	Tested from PCLK input to CLK output, See Figure 6-1 (3)	f_{PCLK} = 22 MHz			0.082 × f_{PCLK}	MHz
			f_{PCLK} = 65 MHz			0.07 × f_{PCLK}	
$t_{pd(L)}$	Propagation delay time, input to serial output (data latency Figure 7-4)	TXEN at V_{DD}, V_{IH}=V_{DD}, V_{IL}=GND, R_L=100 Ω	1-channel mode	0.8/f_{PCLK}	1/f_{PCLK}	1.2/f_{PCLK}	s
			2-channel mode	1.0/f_{PCLK}	1.21/f_{PCLK}	1.5/f_{PCLK}	
			3-channel mode	1.1/f_{PCLK}	1.31/f_{PCLK}	1.6/f_{PCLK}	
t_H × f_{CLK0}	Output CLK duty cycle		1-channel and 3-channel mode	0.45	0.50	0.55	
			2-channel mode	0.49	0.53	0.58	
t_{GS}	TXEN Glitch suppression pulse width(2)	V_{IH}=V_{DD}, V_{IL}=GND, TXEN toggles between V_{IL} and V_{IH}, see Figure 7-7 and Figure 7-8		3.8		10	µs
t_{pwrup}	Enable time from power down (↑TXEN)	Time from TXEN pulled high to CLK and Dx outputs enabled and transmit valid data; see Figure 7-8			0.24	2	ms
t_{pwrdn}	Disable time from active mode (↓TXEN)	TXEN is pulled low during transmit mode; time measurement until output is disabled and PLL is Shutdown; see Figure 7-8			0.5	11	µs
t_{wakup}	Enable time from Standby (↕PCLK)	TXEN at V_{DD}; device in standby; time measurement from PCLK starts switching to CLK and Dx outputs enabled and transmit valid data; see Figure 7-8			0.23	2	ms
t_{sleep}	Disable time from Active mode (PCLK stopping)	TXEN at V_{DD}; device is transmitting; time measurement from PCLK input signal stops until CLK + Dx outputs are disabled and PLL is disabled; see Figure 7-8			0.4	100	µs

(1) All typical values are at 25°C and with 1.8 V supply unless otherwise noted.
(2) The TXEN input incorporates glitch-suppression circuitry to disregard short input pulses. t_{GS} is the duration of either a high-to-low or low-to-high transition that is suppressed.
(3) The Maximum Limit is based on statistical analysis of the device performance over process, voltage, and temp ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

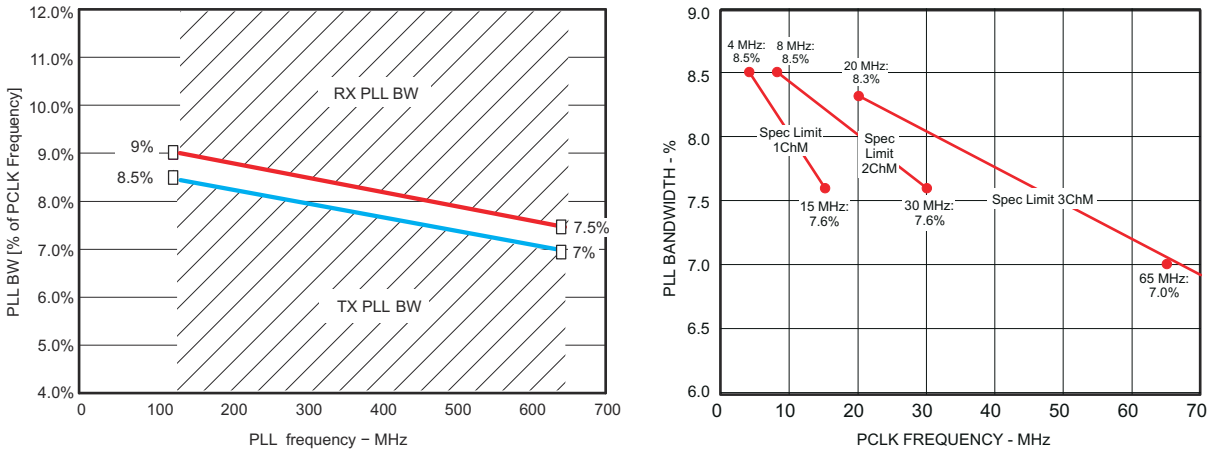


Figure 6-1. LVDS301 PLL Bandwidth (also showing the LVDS302 PLL bandwidth)

6.8 Timing Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PPOSX}	Output Pulse Position, ↑↓serial data to ↑CLK; see (1) (2) and Figure 7-6	1ChM: x=0..29, f_{PCLK}=15 MHz; TXEN at V_{DD}, V_{IH}=V_{DD}, V_{IL}=GND, R_L=100 Ω, test pattern as in Table 7-7 (3)	$\frac{x}{30 \cdot f_{PCLK}} - 330\ ps$		$\frac{x}{30 \cdot f_{PCLK}} + 330\ ps$	ps
		1ChM: x=0..29, f_{PCLK}=4 MHz to 15 MHz (4)	$\frac{x - 0.1845}{30 \cdot f_{PCLK}}$		$\frac{x + 0.1845}{30 \cdot f_{PCLK}}$	
		2ChM: x = 0..14, f_{PCLK} = 30 MHz TXEN at V_{DD}, V_{IH}=V_{DD}, V_{IL}=GND, R_L=100 Ω, test pattern as in Table 7-8 (3)	$\frac{x}{15 \cdot f_{PCLK}} - 330\ ps$		$\frac{x}{15 \cdot f_{PCLK}} + 330\ ps$	
		2ChM: x=0..14, f_{PCLK}= 8 MHz to 30 MHz (4)	$\frac{x - 0.1845}{15 \cdot f_{PCLK}}$		$\frac{x + 0.1845}{15 \cdot f_{PCLK}}$	
		3ChM: x=0..9, f_{PCLK}=65 MHz, TXEN at V_{DD}, V_{IH}=V_{DD}, V_{IL}=GND, R_L=100 Ω, test pattern as in Table 7-9 (3)	$\frac{x}{10 \cdot f_{PCLK}} - 210\ ps$		$\frac{x}{10 \cdot f_{PCLK}} + 210\ ps$	
		3ChM: x=0..9, f_{PCLK}=20 MHz to 65 MHz (4)	$\frac{x - 0.153}{10 \cdot f_{PCLK}}$		$\frac{x + 0.153}{10 \cdot f_{PCLK}}$	

(1) This number also includes the high-frequency random and deterministic PLL clock jitter that is not traceable by the SN65LVDS302 receiver PLL; tPPosx represents the total timing uncertainty of the transmitter necessary to calculate the jitter budget when combined with the SN65LVDS302 receiver;

(2) The pulse position min/max variation is given with a bit error rate target of 10^{-12}; The measurement estimates the random jitter contribution to the total jitter contribution by multiplying the random RMS jitter by the factor 14; Measurements of the total jitter are taken over a sample amount of > 10^{-12} samples.

(3) The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temp ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

(4) These Minimum and Maximum Limits are simulated only.

6.9 Device Power Dissipation

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
P_D	Device Power Dissipation	V_{DDx} = 1.8 V, T_A = 25°C	f_{CLK} = 4 MHz	14.4		mW
			f_{CLK} = 65 MHz	44.5		
		V_{DDx} = 1.95 V, T_A = –40°C	f_{CLK} = 4 MHz		22.3	mW
			f_{CLK} = 65 MHz		71.8	

6.10 Typical characteristics

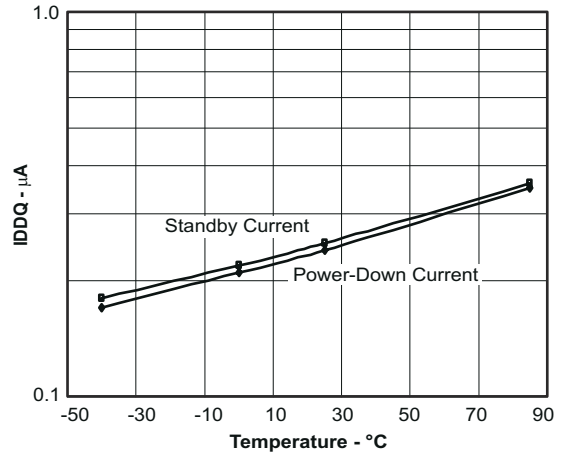


Figure 6-2. Powerdown, Standby Supply Current vs Temperature

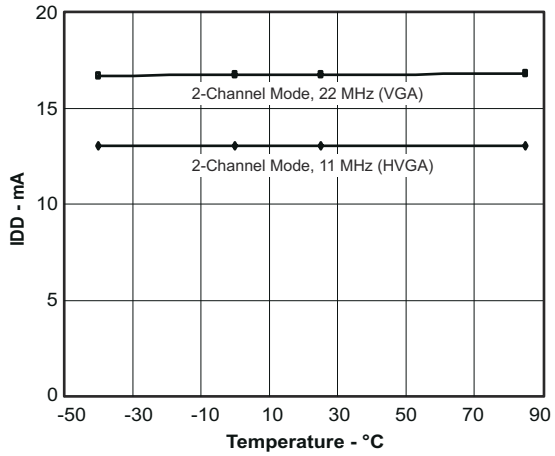


Figure 6-3. Supply Current I_{DD} vs Temperature

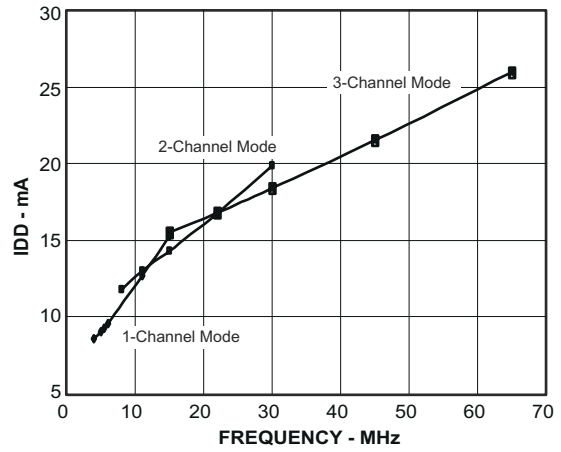


Figure 6-4. Supply Current vs PCLK Frequency

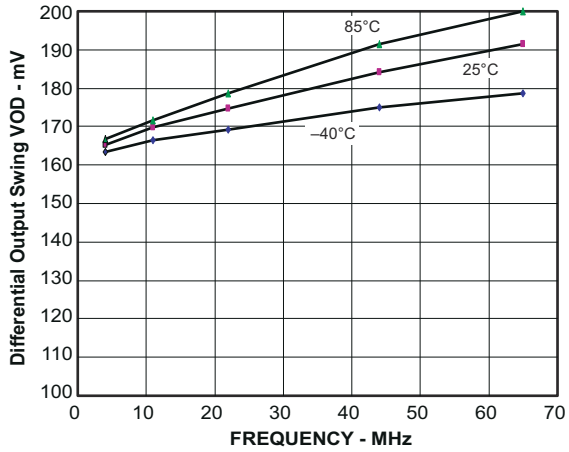


Figure 6-5. Differential Output Swing vs PCLK Frequency

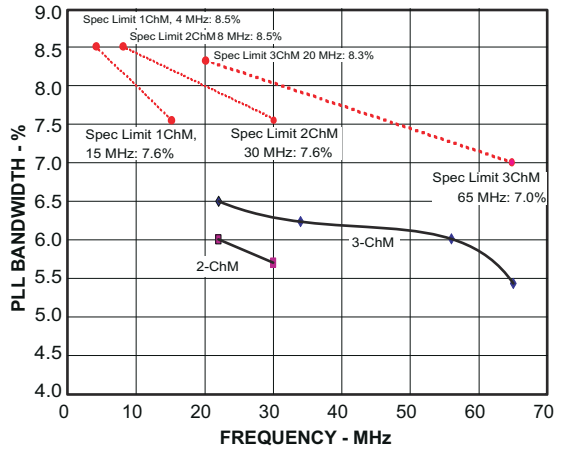


Figure 6-6. PLL Bandwidth

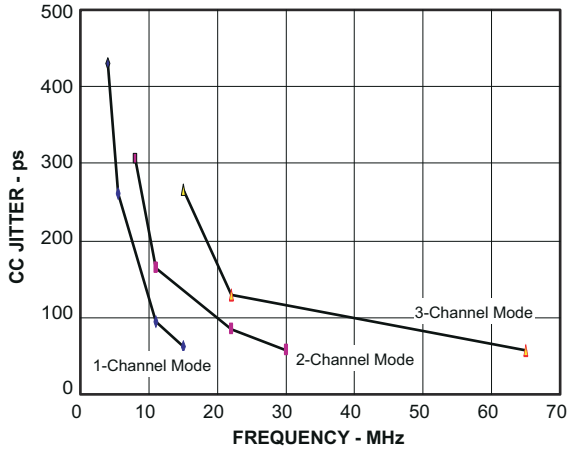


Figure 6-7. Cycle-to-cycle Output Jitter vs PCLK Frequency

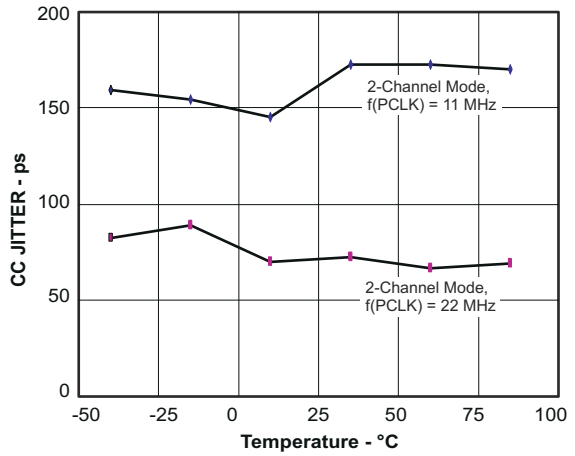


Figure 6-8. Cycle-to-cycle Output Jitter vs Temperature

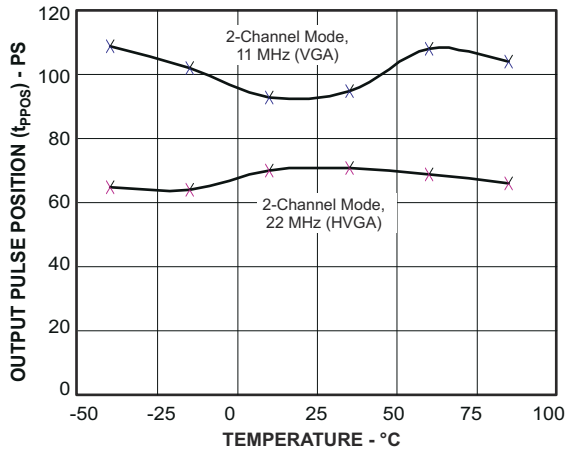


Figure 6-9. Output Pulse Position vs Temperature

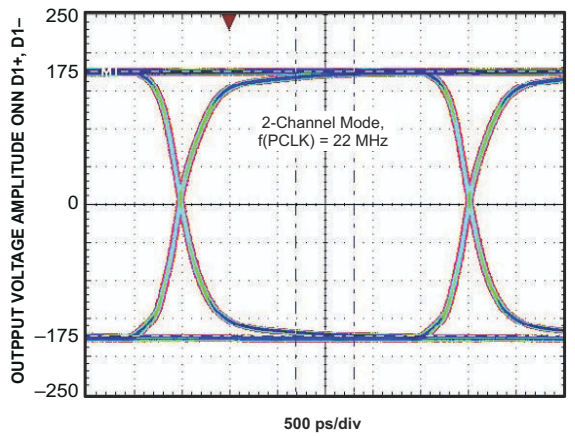


Figure 6-10. Data Eye Pattern, 2-channel Mode

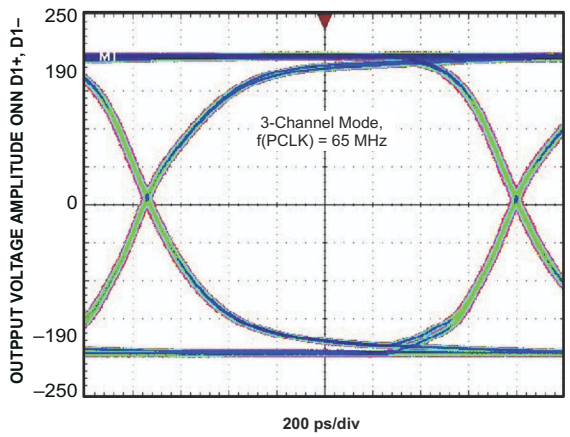


Figure 6-11. Data Eye Pattern, 3-channel Mode

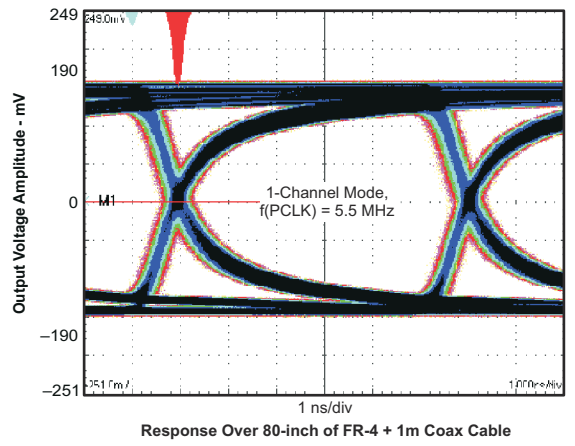


Figure 6-12. QVGA Output Waveform

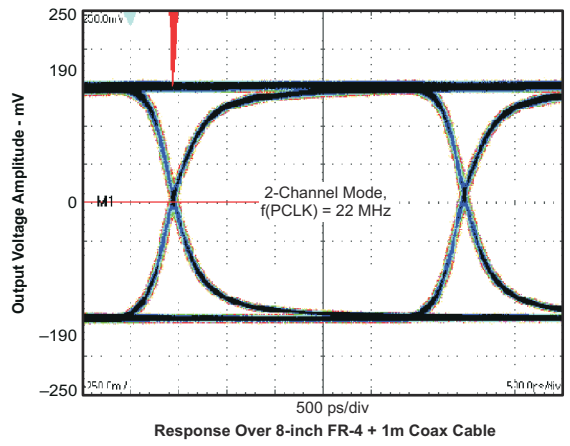


Figure 6-13. VGA 2-channel Output Waveform

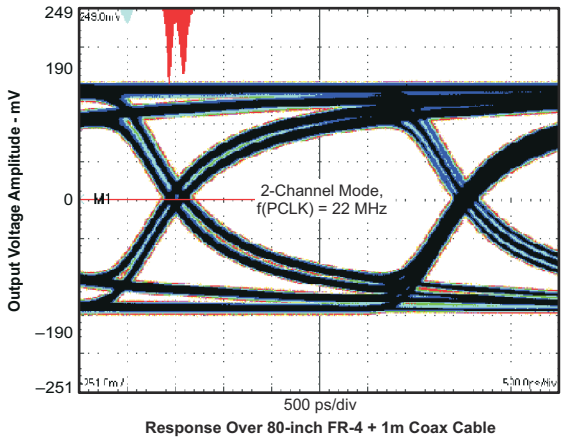


Figure 6-14. VGA 2-channel Output Waveform

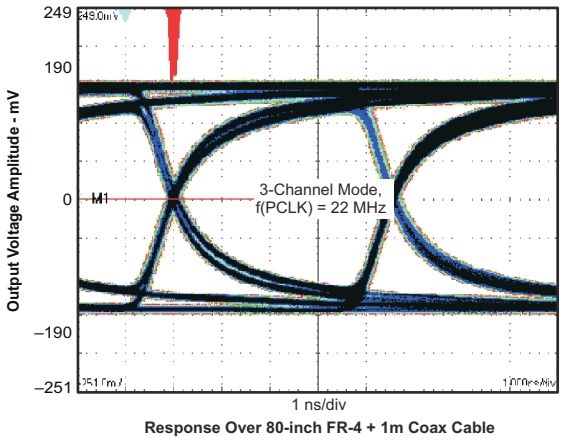


Figure 6-15. VGA 3-channel Output Waveform

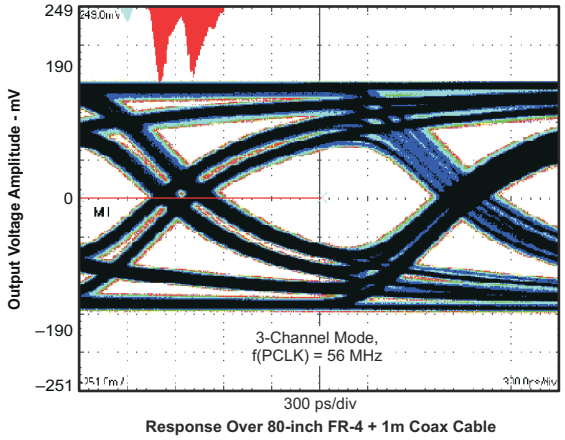


Figure 6-16. XGA 3-channel Output Waveform

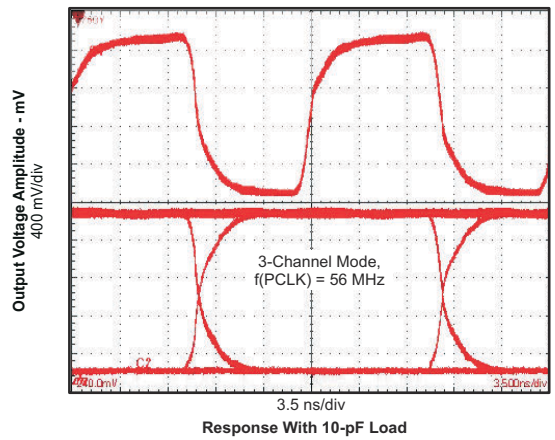


Figure 6-17. XGA 3-channel Output Waveform on the SN65LVDS302 when driven by the SN65LVDS301

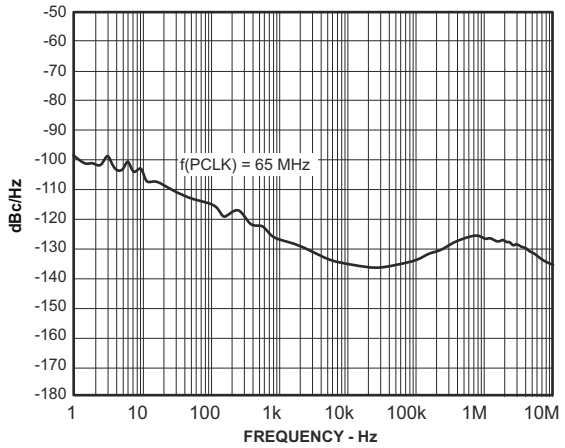


Figure 6-18. PLL Phase Noise

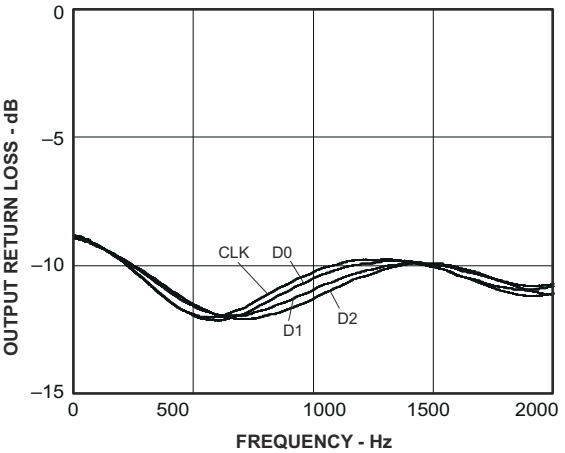


Figure 6-19. Output Return Loss

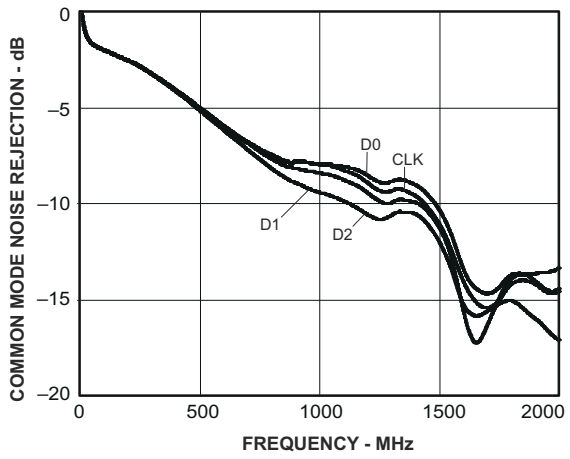


Figure 6-20. Output Common Mode Noise Rejection

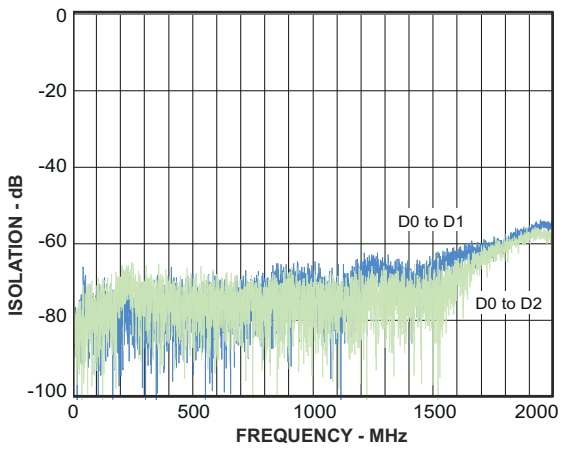


Figure 6-21. Crosstalk

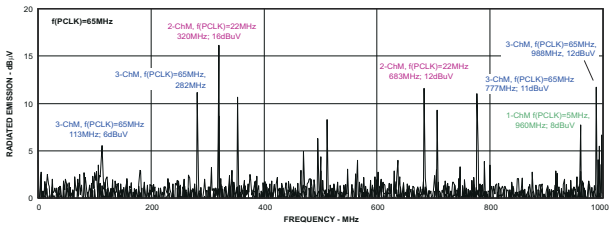


Figure 6-22. GTEM SAE J1752/3 EMI Test

7 Parameter Measurement Information

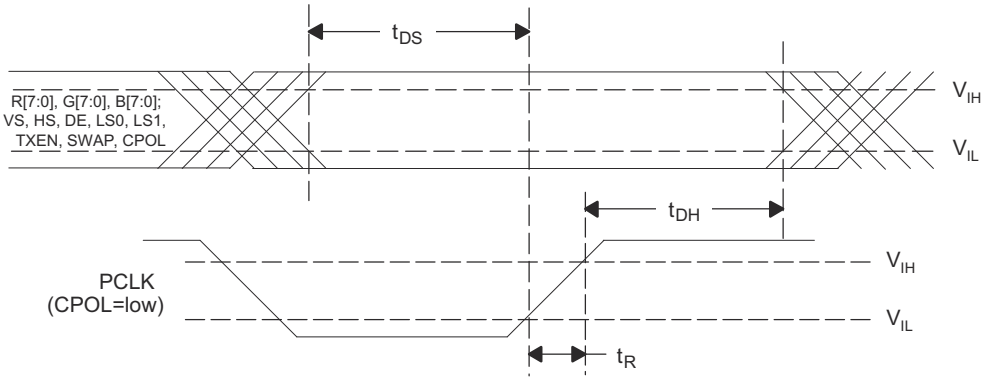


Figure 7-1. Setup/Hold Time

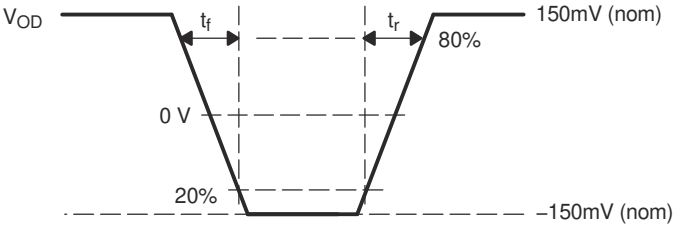
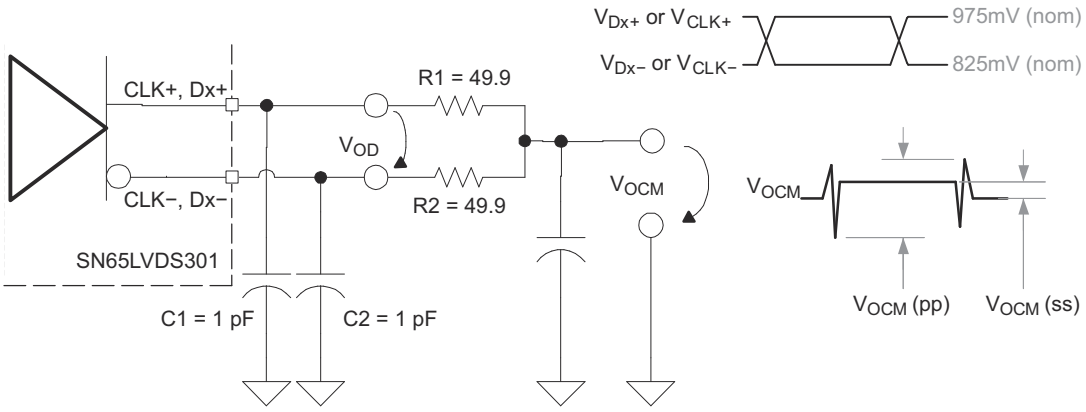


Figure 7-2. Rise and Fall Time Definitions



NOTES:
A. 20 MHz output test pattern on all differental outputs (CLK, D0, D1, and D2):
this is achieved by: 1. Device is set to 3-channel-mode;
2. f_{PCLK} = 20 MHz
3. Inputs R[7:3] = B[7:3] connected to V_{DD}, all other data inputs set to GND.
B. C1, C2 and C3 includes instrumentation and fixture capacitance; tolerance ± 20%; C, R1 and R2 tolerance ± 1%.
C. The measurement of V_{OCM}(pp) and V_{OC}(ss) are taken with test equipment bandwidth >1 GHz.

Figure 7-3. Driver Output Voltage Test Circuit and Definitions

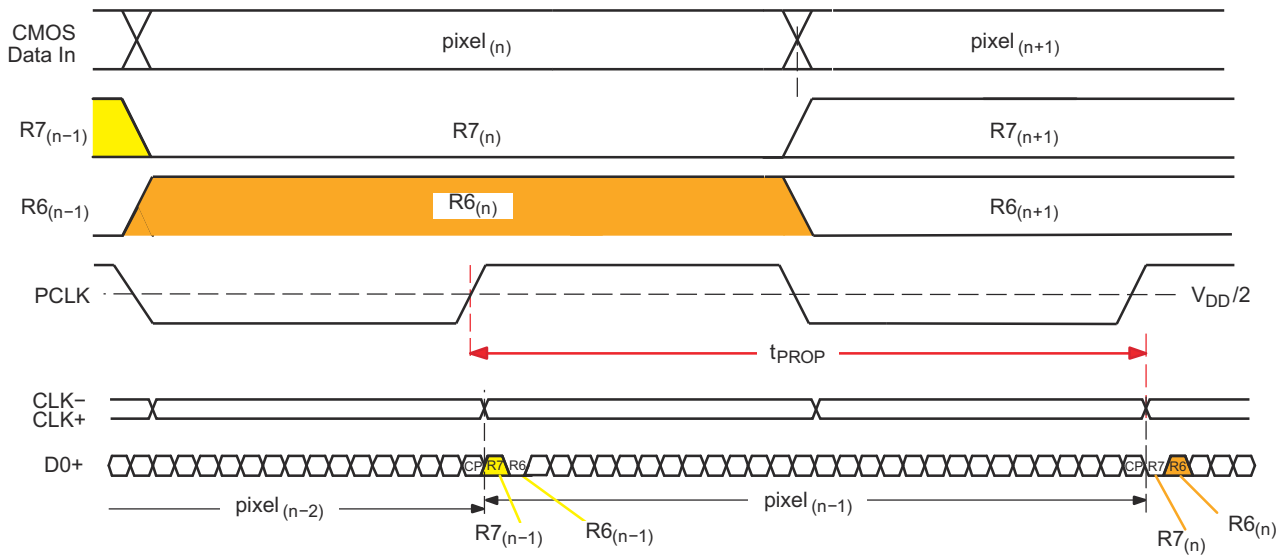


Figure 7-4. $t_{pd(L)}$ Propagation Delay Input to Output (LS0 = LS1 = 0; CPOL = 0)

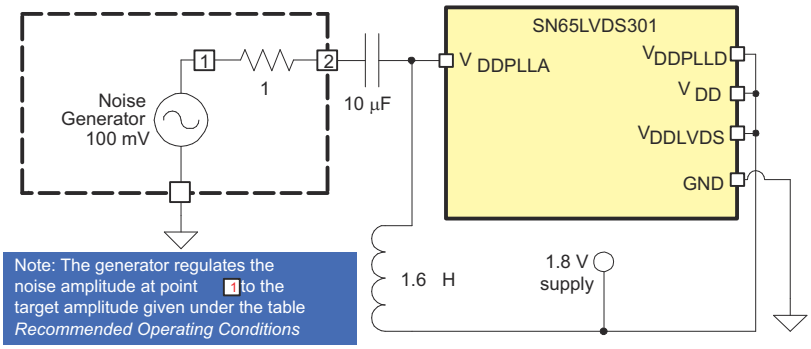


Figure 7-5. Power Supply Noise Test Set-Up

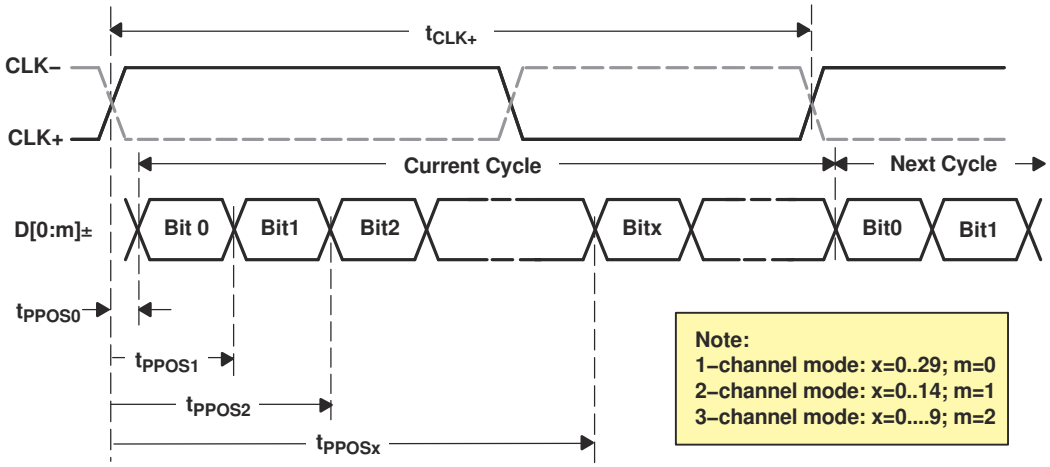


Figure 7-6. $t_{SK(0)}$ SubLVDS Output Pulse Position Measurement

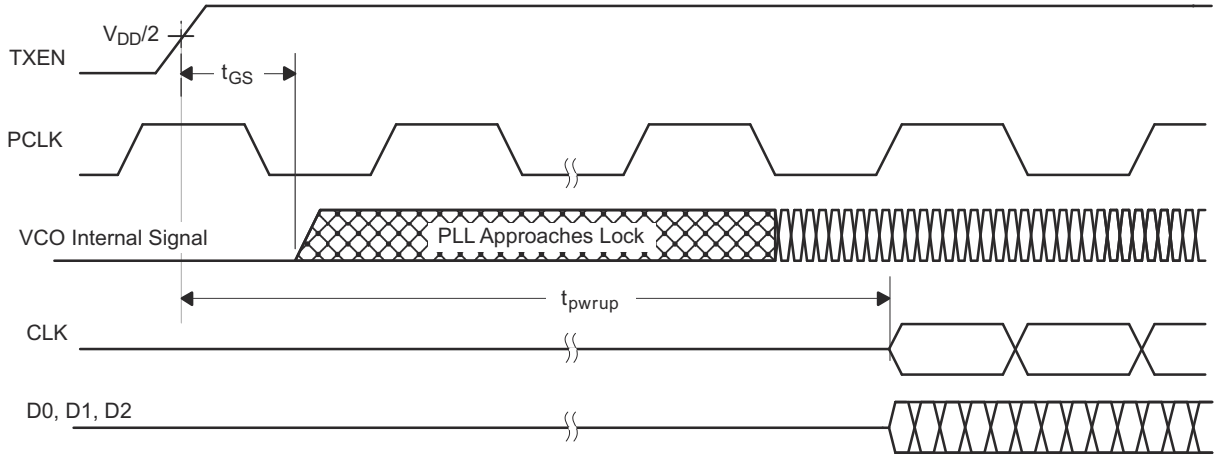


Figure 7-7. Transmitter Behavior While Approaching Sync

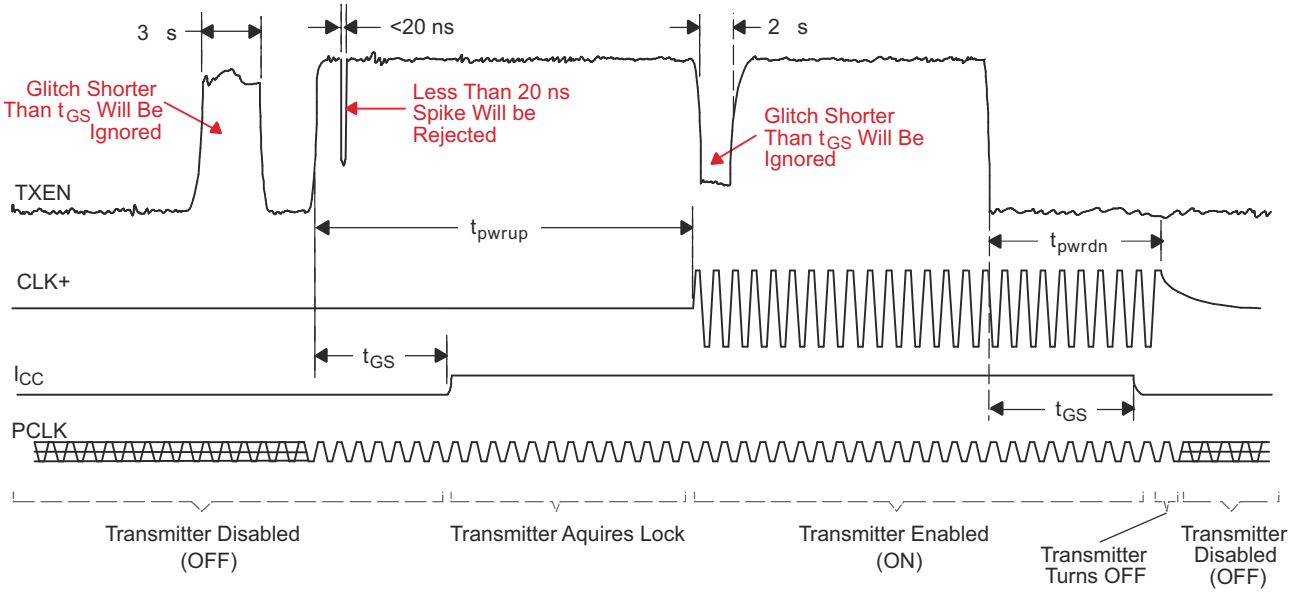


Figure 7-8. Transmitter Enable Glitch Suppression Time

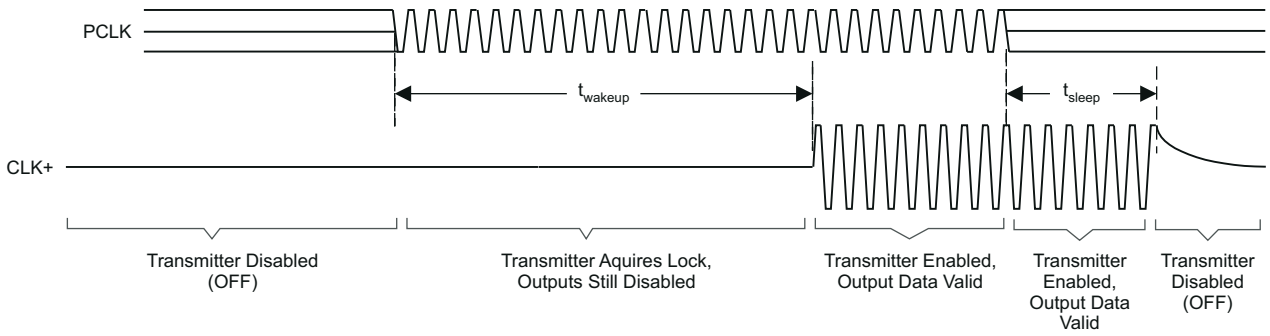


Figure 7-9. Standby Detection

7.1.1 Power Consumption Tests

Table 7-1 shows an example test pattern word.

Table 7-1. Example Test Pattern Word

Word	R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x7C3E1E7

7				C				3				E				1				E				7			
R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	0	VS	HS	DE
0	1	1	1	1	1	0	0	0	0	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1

7.1.1.1 Typical IC Power Consumption Test Pattern

The typical power consumption test patterns consists of sixteen 30-bit transmit words in 1-channel mode, eight 30-bit transmit words in 2-channel mode and five 30-bit transmit words in 3-channel mode. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

7.1.1.2

Table 7-2. Typical IC Power Consumption Test Pattern, 1-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000007
2	0xFFF0007
3	0x01FFF47
4	0xF0E07F7
5	0x7C3E1E7
6	0xE707C37
7	0xE1CE6C7
8	0xF1B9237
9	0x91BB347
10	0xD4CCC67
11	0xAD53377
12	0xACB2207
13	0xAAB2697
14	0x5556957
15	0xAAAAAB3
16	0xAAAAAA5

Table 7-3. Typical IC Power Consumption Test Pattern, 2-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000001
2	0x03F03F1
3	0xBFFBFF1
4	0x1D71D71
5	0x4C74C71
6	0xC45C451
7	0xA3aA3A5
8	0x5555553

Table 7-4. Typical IC Power Consumption Test Pattern, 3-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0xFFFFFF1
2	0x0000001
3	0xF0F0F01
4	0xCCCCCC1
5	0xAAAAAA7

7.1.2 Maximum Power Consumption Test Pattern

The maximum (or worst-case) power consumption of the SN65LVDS301 is tested using the two different test patterns shown in Table 7-5 and Table 7-6. The test patterns consist of sixteen 30-bit transmit words in 1-channel mode, eight 30-bit transmit words in 2-channel mode and five 30-bit transmit words in 3-channel mode. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

Table 7-5. Worst-Case Power Consumption Test Pattern

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0xAAAAAA5
2	0x5555555

Table 7-6. Worst-Case Power Consumption Test Pattern

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000000
2	0xFFFFFF7

7.1.3 Output Skew Pulse Position & Jitter Performance

The following test patterns are used to measure the output-skew pulse position and the jitter performance of the SN65LVDS301. The jitter test pattern stresses the interconnect, particularly to test for ISI. Very long run-lengths of consecutive bits incorporate very high and low data rates, maximinges switching noise. Each pattern is self-repeating for the duration of the test.

Table 7-7. Transmit Jitter Test Pattern, 1-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000001
2	0x0000031
3	0x00000F1
4	0x00003F1
5	0x0000FF1
6	0x0003FF1
7	0x000FFF1
8	0x0F0F0F1
9	0x0C30C31
10	0x0842111
11	0x1C71C71
12	0x18C6311
13	0x1111111
14	0x3333331
15	0x2452413
16	0x22A2A25
17	0x5555553
18	0xDB6DB65
19	0xCCCCCC1
20	0xEEEEEE1
21	0xE739CE1
22	0xE38E381
23	0xF7BDEE1
24	0xF3CF3C1
25	0xF0F0F01
26	0xFFF0001
27	0xFFFC001
28	0xFFFF001
29	0xFFFFC01
30	0xFFFFF01
31	0xFFFFFC1
32	0xFFFFFF1

Table 7-8. Transmit Jitter Test Pattern, 2-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000001
2	0x000FFF3
3	0x8008001
4	0x0030037
5	0xE00E001
6	0x00FF001
7	0x007E001
8	0x003C001
9	0x0018001
10	0x1C7E381
11	0x3333331
12	0x555AAA5
13	0x6DBDB61
14	0x7777771
15	0x555AAA3
16	0xAAAAAA5
17	0x5555553
18	0xAAA5555
19	0x8888881
20	0x9242491
21	0xAAA5571
22	0xCCCCCC1
23	0xE3E1C71
24	0xFFE7FF1
25	0xFFC3FF1
26	0xFF81FF1
27	0xFE00FF1
28	0x1FF1FF1
29	0xFFCFFC3
30	0x7FF7FF1
31	0xFFF0007
32	0xFFFFFF1

Table 7-9. Transmit Jitter Test Pattern, 3-Channel Mode

Word	Test Pattern: R[7:4], R[3:0], G[7:4], G[3:0], B[7-4], B[3-0], 0,VS,HS,DE
1	0x0000001
2	0x0000001
3	0x0000003
4	0x0101013
5	0x0303033
6	0x0707073
7	0x1818183
8	0xE7E7E71
9	0x3535351
10	0x0202021
11	0x5454543
12	0xA5A5A51
13	0xADADAD1
14	0x5555551
15	0xA6A2AA3
16	0xA6A2AA5
17	0x5555553
18	0x5555555
19	0xAAAAAA1
20	0x5252521
21	0x5A5A5A1
22	0xABABAB1
23	0xFDFCFD1
24	0xCAAACA1
25	0x1818181
26	0xE7E7E71
27	0xF8F8F81
28	0xFCFCFC1
29	0xFEFEFE1
30	0xFFFFFF1
31	0xFFFFFF5
32	0xFFFFFF5

8 Detailed Description

8.1 Overview

The SN65LVDS301 is a serialising device where the input paralle data is converted to Sub Low-Voltage Differential Signaling (SubLVDS) serial outputs. The SN65LVDS301 supports three power modes (Shutdown, Standby and Active) to conserve power. When transmitting, the PLL locks to the incoming pixel clock PCLK and generates an internal high-speed clock at the line rate of the data lines. The parallel data are latched on the rising or falling edge of PCLK as selected by the external control signal CPOL. The serialized data is presented on the serial outputs D0, D1, D2 with a recreated PCLK generated from the internal high-speed clock, output on the CLK output. If PCLK stops, the device enters a standby mode to conserve power

The parallel (CMOS) input bus offers a bus-swap feature. The SWAP pin configures the input order of the pixel data to be either R[7:0]. G[7:0], B[7:0], VS, HS, DE or B[0:7]. G[0:7], R[0:7], VS, HS, DE. This gives a PCB designer the flexibility to better match the bus to the host controller pinout or to put the transmitter device on the top side or the bottom side of the PCB.

Two Link Select lines LS0 and LS1 control whether 1, 2 or 3 serial links are used. The TXEN input may be used to put the SN65LVDS301 in a shutdown mode. The SN65LVDS301 enters an active Standby mode if the input clock PCLK stops.

8.2 Functional Block Diagram

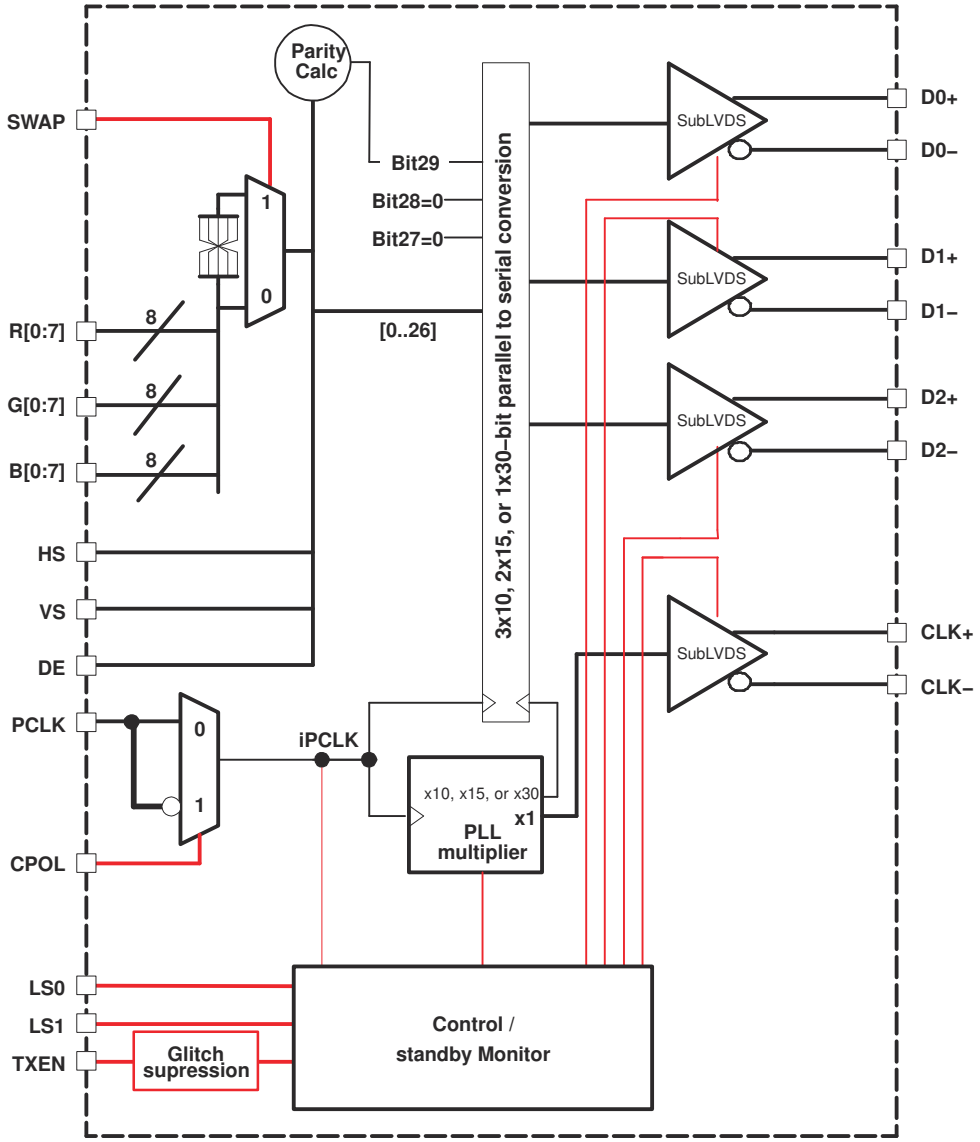


Figure 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Swap Pin Functionality

The SWAP pin allows the pcb designer to reverse the RGB bus to minimize potential signal crossovers in the PCB routing. The two drawings beneath show the RGB signal pin assignment based on the SWAP-pin setting.

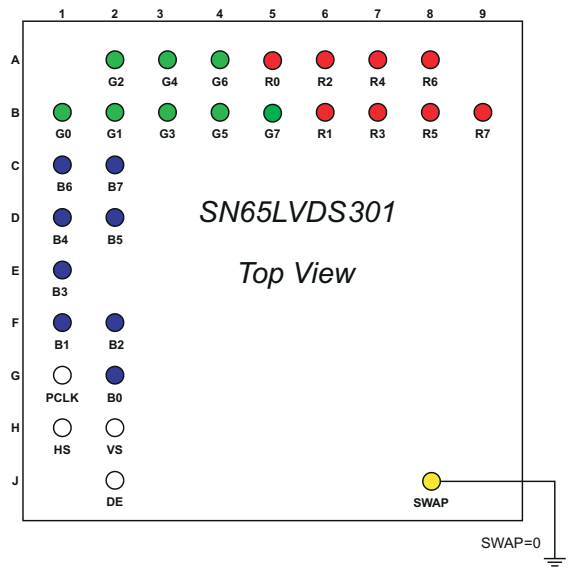


Figure 8-2. SWAP PIN = 0

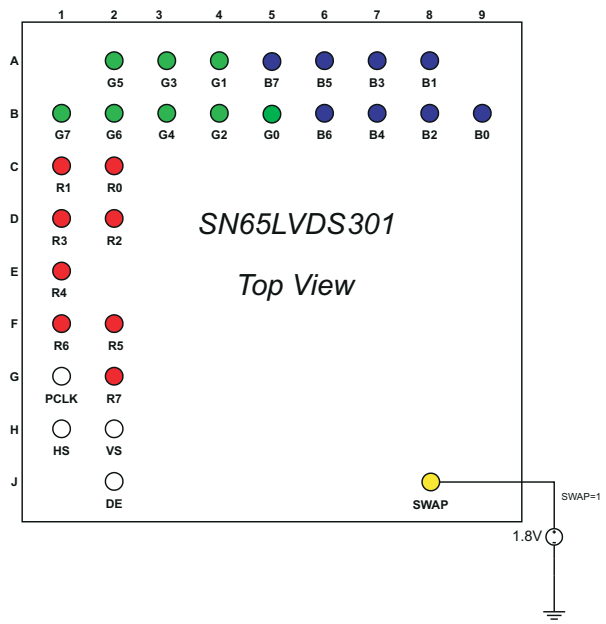


Figure 8-3. SWAP PIN = 1

Table 8-1. NUMERIC PIN LIST

PIN	SWAP	SIGNAL	PIN	SWAP	SIGNAL	PIN	SWAP	SIGNAL
A1	—	GND	**C1**	0	B6	**F1**	0	B1
A2	0	G2		1	R1		1	R6
	1	G5	**C2**	0	B7	**F2**	0	B2
A3	0	G4		1	R0		1	R5
	1	G3	**C3**	UNPOPULATED		**F3**	—	VDD
A4	0	G6	**C4**	—	VDD	**F4**	—	GND
	1	G1	**C5**	—	GND	**F5**	—	GND
A5	0	R0	**C6**	—	VDD	**F6**	—	GND
	1	B7	**C7**	—	VDD	**F7**	—	GND
A6	0	R2	**C8**	—	GND	**F8**	—	V_{DDPLLD}
	1	B5	**C9**	—	LS0	**F9**	—	D1+
A7	0	R4	**D1**	0	B4	**G1**	—	PCLK
	1	B3		1	R3	**G2**	0	B0
A8	0	R6	**D2**	0	B5		1	R7
	1	B1		1	R2	**G3**	—	V_{DD}
A9	—	GND	**D3**	—	VDD	**G4**	—	GND
B1	0	G0	**D4**	—	GND	**G5**	—	GND
	1	G7	**D5**	—	GND	**G6**	—	GND
B2	0	G1	**D6**	—	GND	**G7**	—	GND
	1	G6	**D7**	—	GND	**G8**	—	GND_{LVDS}
B3	0	G3	**D8**	—	LS1	**G9**	—	D1–
	1	G4	**D9**	—	D2+	**H1**	—	HS
B4	0	G5	**E1**	0	B3	**H2**	—	VS
	1	G2		1	R4	**H3**	—	GND
B5	0	G7	**E2**	—	GND	**H4**	—	GND_{LVDS}
	1	G0	**E3**	—	VDD	**H5**	—	V_{DDLVDS}

Table 8-1. NUMERIC PIN LIST (continued)

PIN	SWAP	SIGNAL	PIN	SWAP	SIGNAL	PIN	SWAP	SIGNAL
B6	0	R1	E4	—	GND	H6	—	GND_{PLLA}
	1	B6	E5	—	GND	H7	—	V_{DDPLLA}
B7	0	R3	E6	—	GND	H8	—	V_{DDLVDS}
	1	B4	E7	—	GND	H9	—	CPOL
B8	0	R5	E8	—	GND_{PLLD}	J1	—	GND
	1	B2	E9	—	D2–	J2	—	DE
B9	0	R7				J3	—	TXEN
	1	B0				J4	—	D0–
						J5	—	D0+
						J6	—	CLK–
						J7	—	CLK+
						J8	—	SWAP
						J9	—	GND_{LVDS}

8.3.2 Parity Bit Generation

The SN65LVDS301 transmitter calculates the parity of the transmit data word and sets the parity bit accordingly. The parity bit covers the 27 bit data payload consisting of 24 bits of pixel data plus VS, HS and DE. The two reserved bits are not included in the parity generation. ODD Parity bit signaling is used. The transmitter sets the Parity bit if the sum of the 27 data bits result in an even number of ones. The Parity bit is cleared otherwise. This allows the receiver to verify Parity and detect single bit errors.

8.4 Device Functional Modes

8.4.1 Serialization Modes

The SN65LVDS301 transmitter has three modes of operation controlled by link-select pins LS0 and LS1. Table 8-2 shows the serializer modes of operation.

Table 8-2. Logic Table: Link Select Operating Modes

LS1	LS0		Mode of Operation	Data Links Status
0	0	1ChM	1-channel mode (30-bit serialization rate)	D0 active; D1, D2 high-impedance
0	1	2ChM	2-channel mode (15-bit serialization rate)	D0, D1 active; D2 high-impedance
1	0	3ChM	3-channel mode (10-bit serialization rate)	D0, D1, D2 active
1	1		Reserved	Reserved

8.4.1.1 1-Channel Mode

While LS0 and LS1 are held low, the SN65LVDS301 transmits payload data over a single SubLVDS data pair, D0. The PLL locks to PCLK and internally multiplies the clock by a factor of 30. The internal high-speed clock is used to serialize (shift out) the data payload on D0. Two reserved bits and the parity bit are added to the data frame. Figure 8-4 illustrates the timing and the mapping of the data payload into the 30-bit frame. The internal high-speed clock is divided by a factor of 30 to recreate the pixel clock, and presented on the SubLVDS CLK output. While in this mode, the PLL can lock to a clock that is in the range of 4 MHz through 15 MHz. This mode is intended for smaller video display formats (e.g. QVGA to HVGA) that do not require the full bandwidth capabilities of the SN65LVDS301.

Figure 8-4. Data and Clock Output in 1-Channel Mode (LS0 and LS1 = low).

8.4.1.2 2-Channel Mode

While LS0 is held high and LS1 is held low, the SN65LVDS301 transmits payload data over two SubLVDS data pairs, D0 and D1. The PLL locks to PCLK and internally multiplies it by a factor of 15. The internal high-speed clock is used to serialize the data payload on D0, and D1. Two reserved bits and the parity bit are added to the data frame. Figure 8-5 illustrates the timing and the mapping of the data payload into the 30-bit frame and how the frame becomes split into the two output channels. The internal high-speed clock is divided by 15 to recreate the pixel clock, and presented on SubLVDS CLK. The PLL can lock to a clock that is in the range of 8 MHz through 30 MHz in this mode. Typical applications for using the 2-channel mode are HVGA and VGA displays.

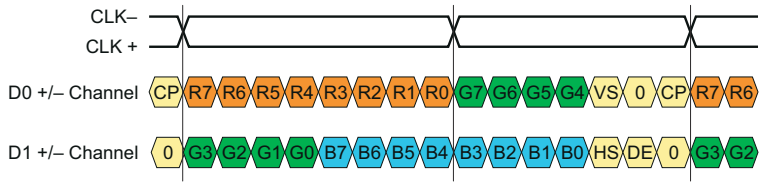


Figure 8-5. Data and Clock Output in 2-Channel Mode (LS0 = high; LS1 = low).

8.4.1.3 3-Channel Mode

While LS0 is held low and LS1 is held high, the SN65LVDS301 transmits payload data over three SubLVDS data pairs D0, D1, and D2. The PLL locks to PCLK, and internally multiplies it by 10. The internal high-speed clock is used to serialize the data payload on D0, D1, and D2. Two reserved bits and the parity bit are added to the data frame. Figure 8-6 illustrates the timing and the mapping of the data payload into the 30-bit frame and how the frame becomes split over the three output channels. The internal high speed clock is divided back down by a factor of 10 to recreate the pixel clock and presented on SubLVDS CLK output. While in this mode, the PLL can lock to a clock in the range of 20 MHz through 65 MHz. The 3-channel mode supports applications with very large display resolutions such as VGA or XGA.

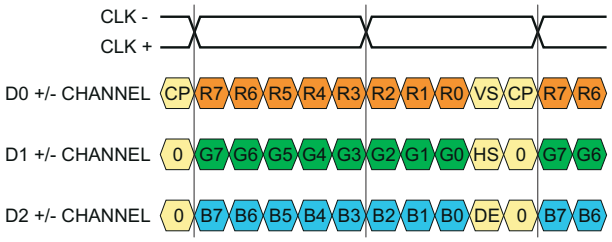


Figure 8-6. Data and Clock Output in 3-Channel Mode (LS0 = low; LS1 = high).

8.4.2 Powerdown Modes

The SN65LVDS301 Transmitter has two powerdown modes to facilitate efficient power management.

8.4.3 Shutdown Mode

The SN65LVDS301 enters Shutdown mode when the TXEN pin is asserted low. This turns off all transmitter circuitry, including the CMOS input, PLL, serializer, and SubLVDS transmitter output stage. All outputs are high-impedance. Current consumption in Shutdown mode is nearly zero.

8.4.4 Standby Mode

The SN65LVDS301 enters the Standby mode if TXEN is high and the PCLK input signal frequency is less than 500kHz. All circuitry except the PCLK input monitor is shut down, and all outputs enter high-impedance mode. The current consumption in Standby mode is very low. When the PCLK input signal is completely stopped, the I_{DD} current consumption is less than 10 µA. The PCLK input must not be left floating.

Note

A floating (left open) CMOS input allows leakage currents to flow from V_{DD} to GND. To prevent large leakage current, a CMOS gate must be kept at a valid logic level, either V_{IH} or V_{IL}. This can be achieved by applying an external voltage of V_{IH} or V_{IL} to all SN65LVDS301 inputs.

8.4.5 Active Modes

When TXEN is high and the PCLK input clock signal is faster than 3 MHz, the SN65LVDS301 enters Active mode. Current consumption in Active mode depends on operating frequency and the number of data transitions in the data payload.

8.4.6 Acquire Mode (PLL approaches lock)

The PLL is enabled and attempts to lock to the input Clock. All outputs remain in high-impedance mode. When the PLL monitor detects stable PLL operation, the device switches from Acquire to Transmit mode. For proper device operation, the pixel clock frequency must fall within the valid f_{PCLK} range specified under recommended operating conditions. If the pixel clock frequency is larger than 3 MHz but smaller than f_{PCLK}(min), the SN65LVDS301 PLL is enabled. Under such conditions, it is possible for the PLL to lock temporarily to the pixel clock, causing the PLL monitor to release the device into transmit mode. If this happens, the PLL may or may not be properly locked to the pixel clock input, potentially causing data errors, frequency oscillation, and PLL deadlock (loss of VCO oscillation).

8.4.7 Transmit Mode

After the PLL achieves lock, the device enters the normal transmit mode. The CLK pin outputs a copy of PCLK. Based on the selected mode of operation, the D0, D1, and D2 outputs carry the serialized data. In 1-channel mode, outputs D1 and D2 remain high-impedance. In the 2-channel mode, output D2 remains high-impedance.

8.4.8 Status Detect and Operating Modes Flow diagram

The SN65LVDS301 switches between the power saving and active modes in the following way:

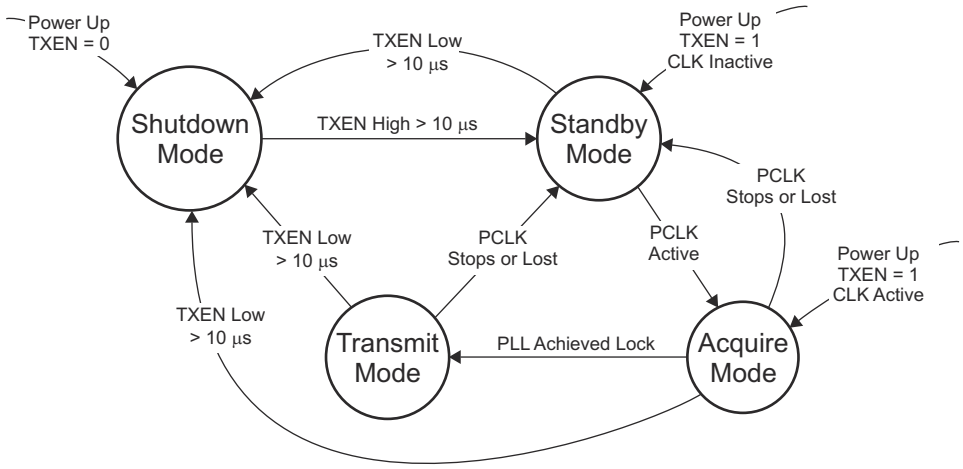


Figure 8-7. Status Detect and Operating Modes Flow Diagram

Table 8-3. Status Detect and Operating Modes Descriptions

Mode	Characteristics	Conditions
Shutdown Mode	Least amount of power consumption(1) (most circuitry turned off); All outputs are high-impedance	TXEN is low(1) (2)
Standby Mode	Low power consumption (only clock activity circuit active; PLL is disabled to conserve power); All outputs are high-impedance	TXEN is high; PCLK input signal is missing or inactive(2)
Acquire Mode	PLL tries to achieve lock; All outputs are high-impedance	TXEN is high; PCLK input monitor detected input activity
Transmit Mode	Data transfer (normal operation); Transmitter serializes data and transmits data on serial output; unused outputs remain high-impedance	TXEN is high and PLL is locked to incoming clock

(1) In Shutdown Mode, all SN65LVDS301 internal switching circuits (e.g., PLL, serializer, etc.) are turned off to minimize power consumption. The input stage of any input pin remains active.

(2) Leaving inputs unconnected can cause random noise to toggle the input stage and potentially harm the device. All inputs must be tied to a valid logic level V_{IL} or V_{IH} during Shutdown or Standby Mode.

Table 8-4. Operating Mode Transitions

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Shutdown → Standby	Drive TXEN high to enable transmitter	1. TXEN high > 10 µs 2. Transmitter enters standby mode a. All outputs are high-impedance b. Transmitter turns on clock input monitor
Standby → Acquire	Transmitter activity detected	1. PCLK input monitor detects clock input activity; 2. Outputs remain high-impedance; 3. PLL circuit is enabled
Acquire → Transmit	Link is ready to transfer data	1. PLL is active and approaches lock 2. PLL achieved lock within 2 ms 3. Parallel Data input latches into shift register 4. CLK output turns on 5. selected Data outputs turn on and send out first serial data bit
Transmit → Standby	Request Transmitter to enter Standby mode by stopping PCLK	1. PCLK Input monitor detects missing PCLK 2. Transmitter indicates standby, putting all outputs into high-impedance; 3. PLL shuts down; 4. PCLK activity input monitor remains active
Transmit/Standby → Shutdown	Turn off Transmitter	1. TXEN pulled low for longer than 10us 2. Transmitter indicates standby, putting output CLK+ and CLK– into high-impedance state; 3. Transmitter puts all other outputs into high-impedance state 4. Most IC circuitry is shut down for least power consumption

9 Application information

9.1 Application Information

General application guidelines and hints for LVDS drivers and receivers may be found in the LVDS application notes and design guides.

9.2 Preventing Increased Leakage Currents in Control Inputs

A floating (left open) CMOS input allows leakage currents to flow from V_{DD} to GND. Do not leave any CMOS Input unconnected or floating. Every input must be connected to a valid logic level V_{IH} or V_{OL} while power is supplied to V_{DD}. This also minimizes the power consumption of standby and power down mode.

9.3 VGA Application

Figure 9-1 shows a possible implementation of a VGA display. The LVDS301 interfaces to the SN65LVDS302, which is the corresponding receiver device to deserialize the data and drive the display driver. The pixel clock rate of 22 MHz assumes ~10% blanking overhead and 60 Hz display refresh rate. The application assumes 24-bit color resolution. It is also shown, how the application processor provides a powerdown (reset) signal for both serializer and the display driver. The signal count over the FPC could be further decreased by using the standby option on the SN65LVDS302 and pulling RXEN high with a 30 kΩ resistor to V_{DD}.

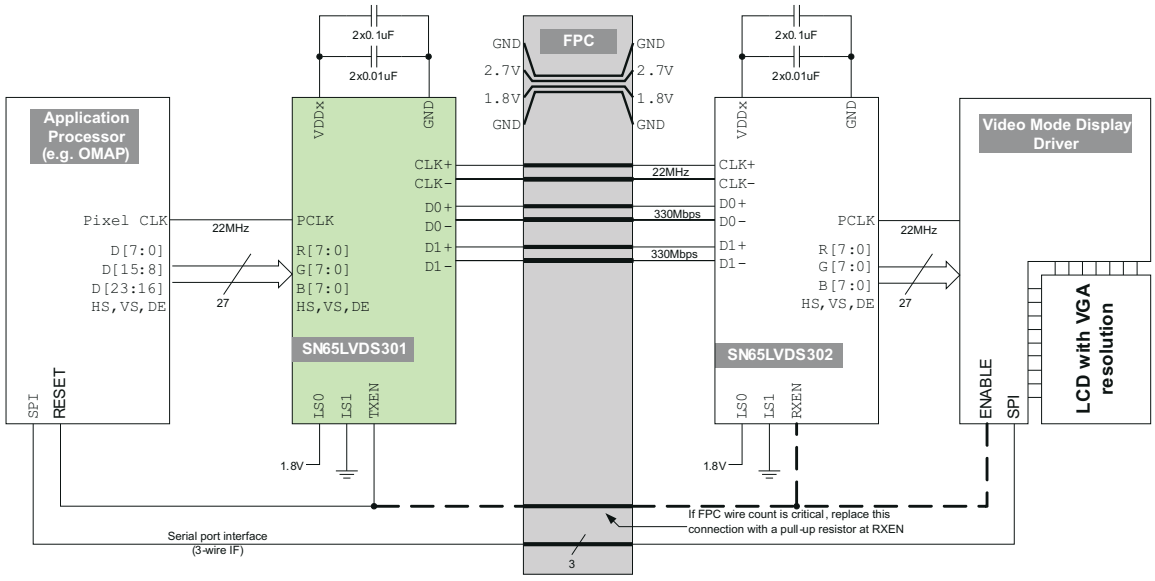


Figure 9-1. Typical VGA Display Application

9.4 Dual LCD-Display Application

The example in Figure 9-2 shows a possible application setup driving two video mode displays from one application processor. The data rate of 330 Mbps at a pixel clock rate of 5.5 MHz corresponds to QVGA resolution at 60 Hz refresh rate and 10% blanking overhead.

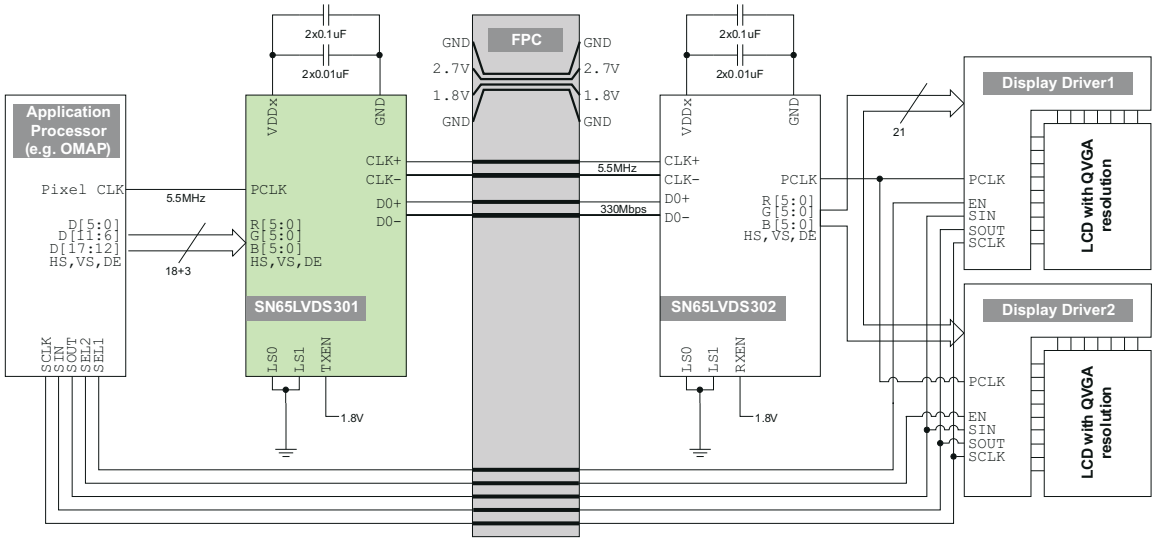


Figure 9-2. Example Dual-QVGA Display Application

9.5 Typical Application Frequencies

The SN65LVDS301 supports pixel clock frequencies from 4 MHz to 65 MHz over 1, 2, or 3 data lanes. Table 9-1 provides a few typical display resolution examples and shows the number of data lanes necessary to connect the LVDS301 with the display. The blanking overhead is assumed to be 20%. Often, blanking overhead is smaller, resulting in a lower data rate. Furthermore, the examples in the table assumes a display frame refresh rate of 60 Hz or 90 Hz. The actual refresh rate may differ depending on the application-processor clock implementation.

Table 9-1. Typical Application Data Rates & Serial Lane Usage

Display Screen Resolution	Visible Pixel Count	Blanking Overhead	Display Refresh Rate	Pixel Clock Frequency [MHz]	Serial Data Rate Per Lane		
					1-ChM	2-ChM	3-ChM
176x220 (QCIF+)	38,720	20%	90 Hz	4.2 MHz	125 Mbps		
240x320 (QVGA)	76,800		60 Hz	5.5 MHz	166 Mbps		
640x200	128,000			9.2 MHz	276 Mbps	138 Mbps	
352x416 (CIF+)	146,432			10.5 MHz	316 Mbps	158 Mbps	
352x440	154,880			11.2 MHz	335 Mbps	167 Mbps	
320x480 (HVGA)	153,600			11.1 MHz	332 Mbps	166 Mbps	
800x250	200,000			14.4 MHz	432 Mbps	216 Mbps	
640x320	204,800			14.7 MHz	442 Mbps	221 Mbps	
640x480 (VGA)	307,200			22.1 MHz		332 Mbps	221 Mbps
1024x320	327,680			23.6 MHz		354 Mbps	236 Mbps
854x480 (WVGA)	409,920			29.5 MHz		443 Mbps	295 Mbps
800x600 (SVGA)	480,000			34.6 MHz			346 Mbps
1024x768 (XGA)	786,432			56.6 MHz			566 Mbps

9.5.1 Calculation Example: HVGA Display

This example calculation shows a typical Half-VGA display with these parameters:

Display Resolution:	480 x 320
Frame Refresh Rate:	58.4 Hz
Horizontal Visible Pixel:	480 columns
Horizontal Front Porch:	20 columns
Horizontal Sync:	5 columns
Horizontal Back Porch:	3 columns
Vertical Visible Pixel:	320 lines
Vertical Front Porch:	10 lines
Vertical Sync:	5 lines
Vertical Back Porch:	3 lines

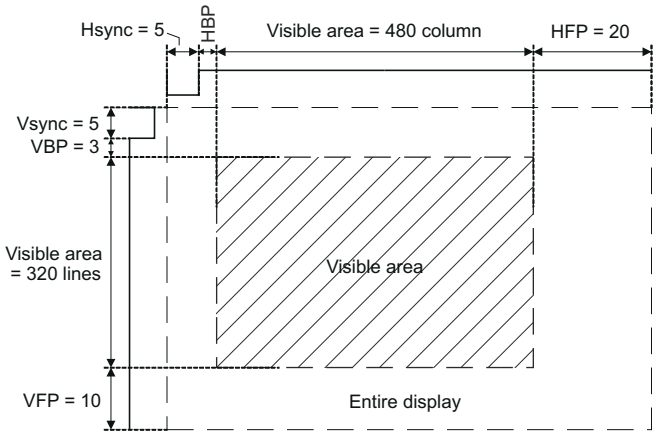


Figure 9-3. HVGA Display Parameters

Calculation of the total number of pixel and Blanking overhead:

Visible Area Pixel Count:	480 × 320 = 153600 pixel
Total Frame Pixel Count:	(480+20+5+3) × (320+10+5+3) = 171704 pixel
Blanking Overhead:	(171704-153600) ÷ 153600 = 11.8 %

The application requires following serial-link parameters:

Pixel Clk Frequency:	171704 × 58.4 Hz = 10.0 MHz
Serial Data Rate:	1-channel mode: 10.0 MHz × 30 bit/channel = 300 Mbps
	2-channel mode: 10.0 MHz × 15 bit/channel = 150 Mbps

10 Power Supply Design Recommendation

For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

10.1 Decoupling Recommendation

The SN65LVDS301 was designed to operate reliably in a constricted environment with other digital switching ICs. In many designs, the SN65LVDS301 often shares a power supply with the application processor. The SN65LVDS301 can operate with power supply noise as specified in *Recommend Device Operating Conditions*. To minimize the power supply noise floor, provide good decoupling near the SN65LVDS301 power pins. The use of four ceramic capacitors (2×0.01 µF and 2×0.1 µF) provides good performance. At the very least, it is recommended to install one 0.1 µF and one 0.01 µF capacitor near the SN65LVDS301. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and IC power inputs pins must be minimized. Placing the capacitor underneath the SN65LVDS301 on the bottom of the pcb is often a good choice.

11 Layout

11.1 Layout Guidelines

Use chamfered corners (45° bends) instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45° bend is seen as a smaller discontinuity.

When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.

Avoid metal layers and traces underneath or between the pads of the LVDS connectors for better impedance matching. Otherwise they cause the differential impedance to drop below 75 Ω and fail the board during TDR testing.

Use solid power and ground planes for 100 Ω impedance control and minimum power noise.

For a multilayer PCB, TI recommends keeping one common GND layer underneath the device and connect all ground terminals directly to this plane. For 100 Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.

Keep the trace length as short as possible to minimize attenuation.

Place bulk capacitors (10 µF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.

12 Device and Documentation Support

12.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS301ZXH	ACTIVE	NFBGA	ZXH	80	576	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	LVDS301	Samples
SN65LVDS301ZXHR	ACTIVE	NFBGA	ZXH	80	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	LVDS301	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

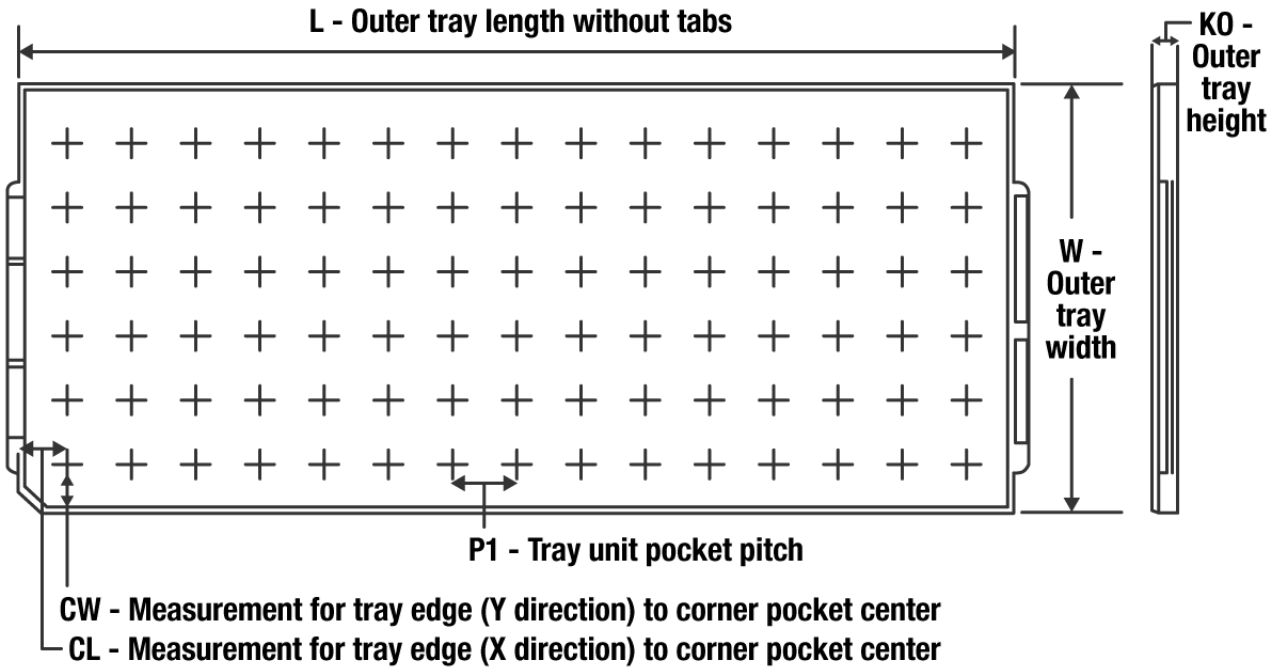
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

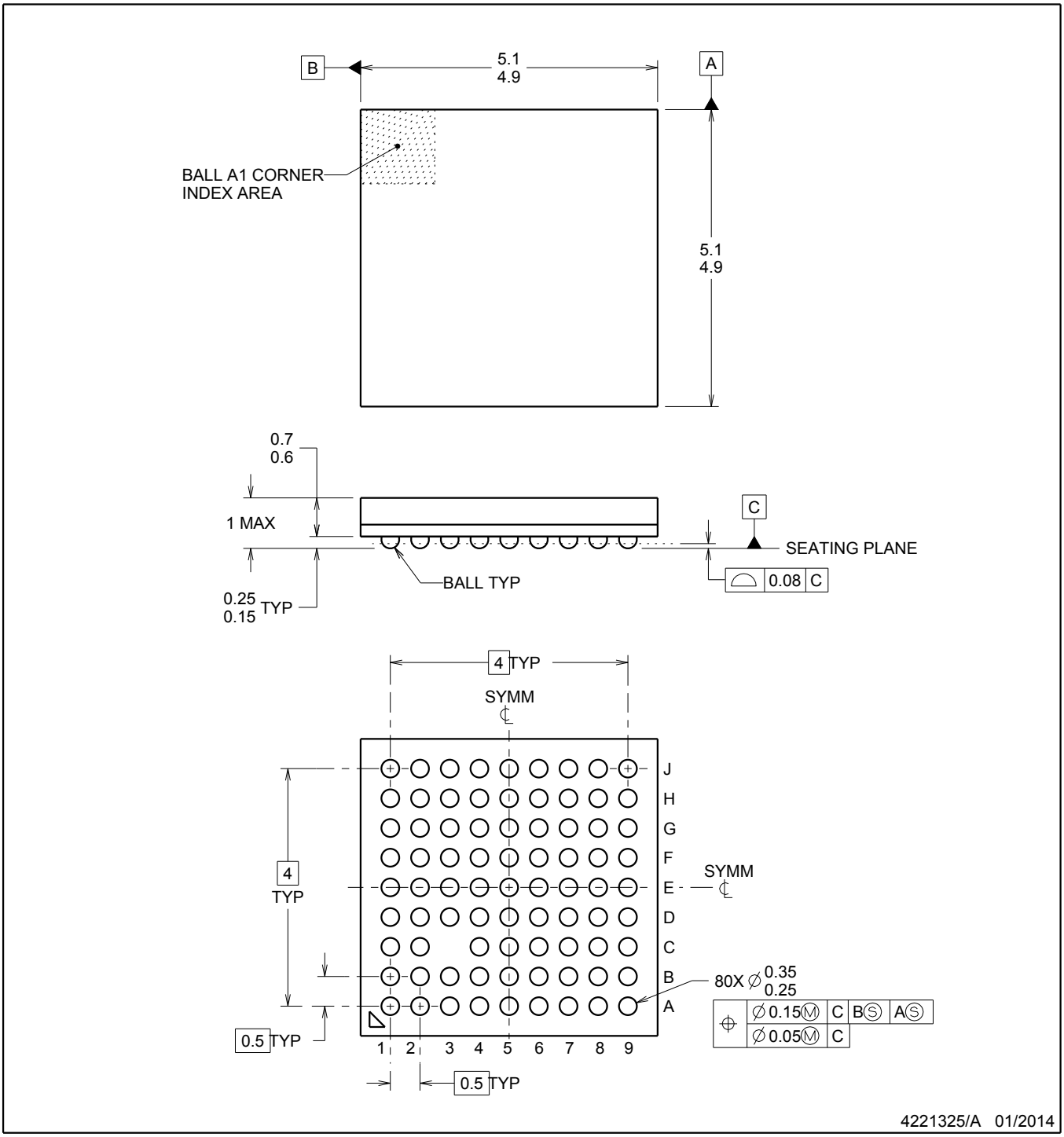
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

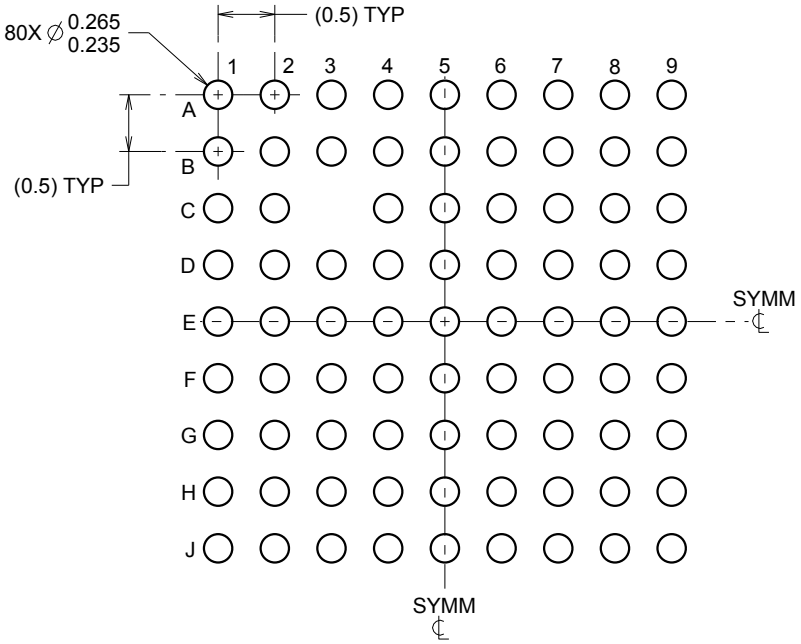
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SN65LVDS301ZXH	ZXH	NFBGA	80	576	16 x 36	150	315	135.9	7620	8.5	8.75	8.7

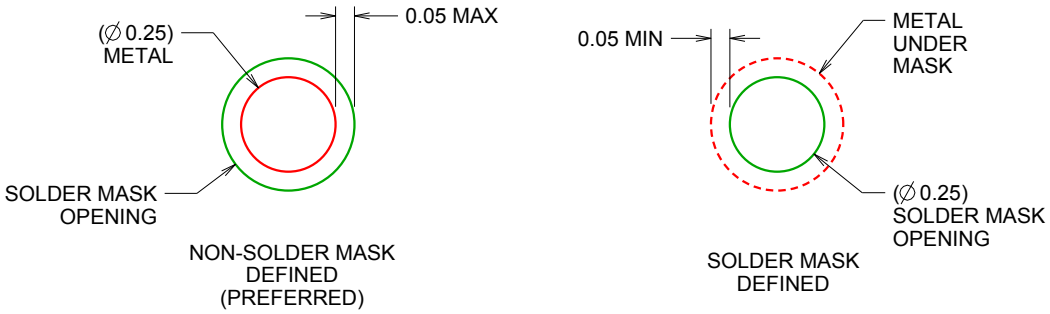


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis is for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

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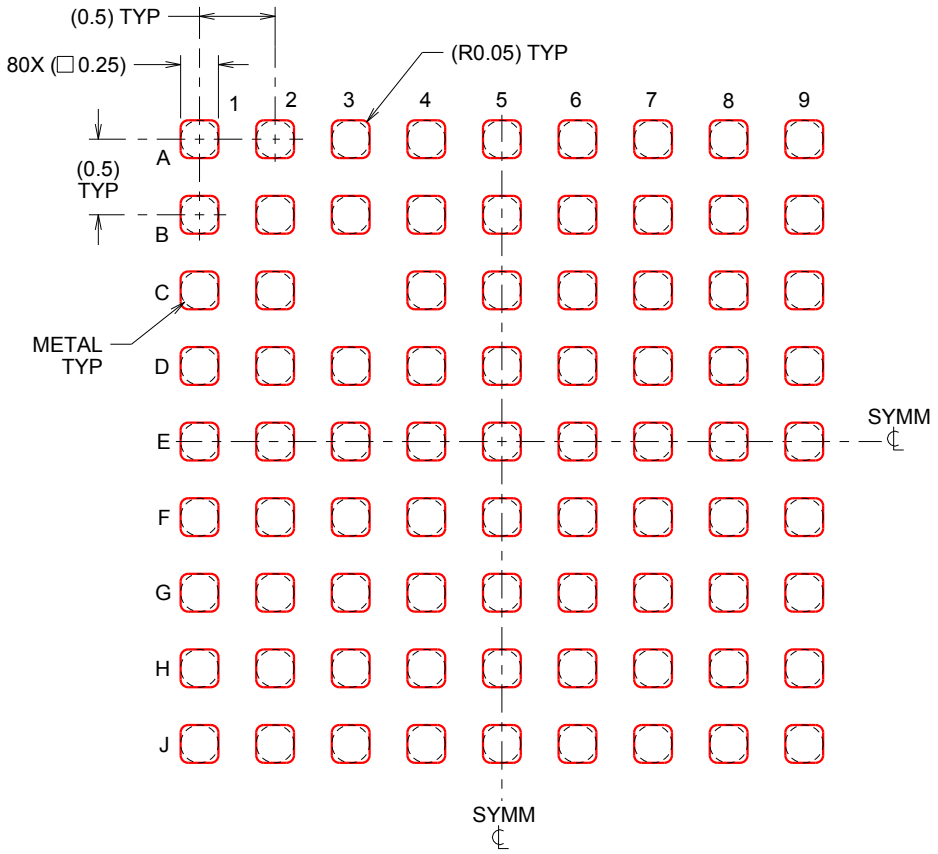
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

4221325/A 01/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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