Freescale Semiconductor
Technical Data

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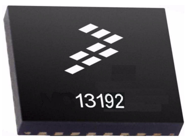
MC13192

2.4 GHz Low Power Transceiver for the IEEE® 802.15.4 Standard

MC13192



Package Information
Plastic Package
Case 1311-03
(QFN-32)

Ordering Information

Device	Device Marking	Package
MC13192FC	13192	QFN-32
MC13192FCR2 (Tape and reel)	13192	QFN-32

1 Introduction

The MC13192 is a short range, low power, 2.4 GHz Industrial, Scientific, and Medical (ISM) band transceivers. The MC13192 contains a complete 802.15.4 physical layer (PHY) modem designed for the IEEE® 802.15.4 Standard which supports peer-to-peer, star, and mesh networking.

The MC13192 includes the 802.15.4 PHY/MAC for use with the HCS08 Family of MCUs. The MC13192 can be used with Freescale's IEEE 802.15.4 MAC and BeeStack, which is Freescale's ZigBee 2006 compliant protocol stack.

When combined with an appropriate microcontroller (MCU), the MC13192 provide a cost-effective solution for short-range data links and networks. Interface with the MCU is accomplished using a four wire serial peripheral interface (SPI) connection and an interrupt request output which allows for the use of a variety of processors. The software and processor can be scaled to fit applications ranging from simple point-to-point systems, through complete ZigBee™ networking.

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For more detailed information about MC13192 operation, refer to the *MC13192 Reference Manual*, (MC13192RM).

Applications include, but are not limited to, the following:

- Remote control and wire replacement in industrial systems such as wireless sensor networks
- Factory automation and motor control
- Energy Management (lighting, HVAC, etc.)
- Asset tracking and monitoring

Potential consumer applications include:

- Home automation and control (lighting, thermostats, etc.)
- Human interface devices (keyboard, mice, etc.)
- Remote control
- Wireless toys

The transceiver includes a low noise amplifier, 1.0 mW power amplifier (PA), PLL with internal voltage controlled oscillator (VCO), on-board power supply regulation, and full spread-spectrum encoding and decoding. The device supports 250 kbps Offset-Quadrature Phase Shift Keying (O-QPSK) data in 2.0 MHz channels with 5.0 MHz channel spacing per the 802.15.4 Standard. The SPI port and interrupt request output are used for receive (RX) and transmit (TX) data transfer and control.

2 Features

- Supports 250 kbps O-QPSK data in 5.0 MHz channels and full spread-spectrum encode and decode (compatible with the 802.15.4 Standard)
- Operates on one of 16 selectable channels in the 2.4 GHz band
- RX sensitivity of <-92 dBm (typical) at 1.0% packet error rate
- 0 dBm nominal, programmable from -27 dBm to 4 dBm typical maximum output power
- Recommended power supply range: 2.0 to 3.4 V
- Buffered transmit and receive data packets for simplified use with low cost MCUs
- Three power down modes for power conservation:
  - — < 1 µA Off current
  - — 1 µA Typical Hibernate current
  - — 35 µA Typical Doze current (no CLKO)
- Four internal timer comparators available to supplement MCU resource
- Programmable frequency clock output (CLKO) for use by MCU
- Onboard trim capability for 16 MHz crystal reference oscillator eliminates need for external variable capacitors and allows for automated production frequency calibration.
- Seven general purpose input/output (GPIO) signals
- Operating temperature range: -40 °C to 85 °C
- Small form factor QFN-32 Package

- — RoHS compliant
- — Meets moisture sensitivity level (MSL) 3
- — 260 °C peak reflow temperature
- — Meets lead-free requirements

2.1 Software Features

Freescale provides a wide range of software functionality to complement the MC13192 hardware. There are three levels of application solutions:

1. Simple proprietary wireless connectivity.
2. User networks built on the 802.15.4 MAC standard.
3. ZigBee-compliant network stack.

2.1.1 Simple MAC (SMAC)

- Small memory footprint (about 3 Kbytes typical)
- Supports point-to-point and star network configurations
- Proprietary networks
- Source code and application examples provided

2.1.2 802.15.4 Standard-Compliant MAC

- Supports star, mesh and cluster tree topologies
- Supports beaconed networks
- Supports GTS for low latency
- Multiple power saving modes (idle doze, hibernate)

2.1.3 ZigBee-Compliant Network Stack

- Supports ZigBee 1.0 specification
- Supports star, mesh and tree networks
- Advanced Encryption Standard (AES) 128-bit security

3 Block Diagrams

Figure 1 shows a simplified block diagram of the MC13192 which is an 802.15.4 Standard compatible transceiver that provides the functions required in the physical layer (PHY) specification.

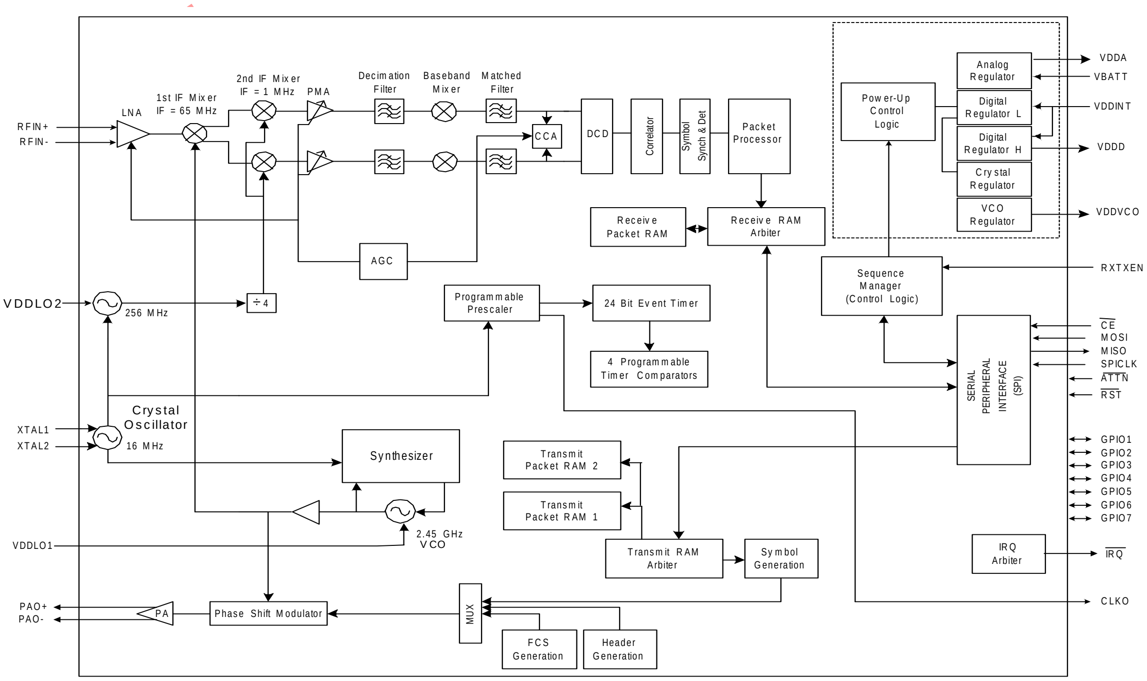
RFIN+
RFIN-
LNA
1st IF Mixer
IF = 65 MHz
2nd IF Mixer
IF = 1 MHz
PMA
Decimation Filter
Baseband Mixer
Matched Filter
CCA
DCD
Correlator
Symbol Synch & Det
Packet Processor
Power-Up Control Logic
Analog Regulator
Digital Regulator L
Digital Regulator H
Crystal Regulator
VCO Regulator
VDDA
VBATT
VDDINT
VDDD
VDDVCO
AGC
Receive Packet RAM
Receive RAM Arbiter
Sequence Manager (Control Logic)
RXTXEN
VDDLO2
256 MHz
÷ 4
Programmable Prescaler
24 Bit Event Timer
4 Programmable Timer Comparators
SERIAL PERIPHERAL INTERFACE (SPI)
$\overline{CE}$
MOSI
MISO
SPICLK
$\overline{ATTN}$
$\overline{RST}$
XTAL1
XTAL2
Crystal Oscillator
16 MHz
Synthesizer
Transmit Packet RAM 2
Transmit Packet RAM 1
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
2.45 GHz VCO
VDDLO1
Transmit RAM Arbiter
Symbol Generation
IRQ Arbiter
$\overline{IRQ}$
PAO+
PAO-
PA
Phase Shift Modulator
MUX
FCS Generation
Header Generation
CLKO

Figure 1. MC13192 Simplified Block Diagram

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Figure 2 shows the basic system block diagram for the MC13192 in an application. Interface with the transceiver is accomplished through a 4-wire SPI port and interrupt request line. The media access control (MAC), drivers, and network and application software (as required) reside on the host processor. The host can vary from a simple 8-bit device up to a sophisticated 32-bit processor depending on application requirements.

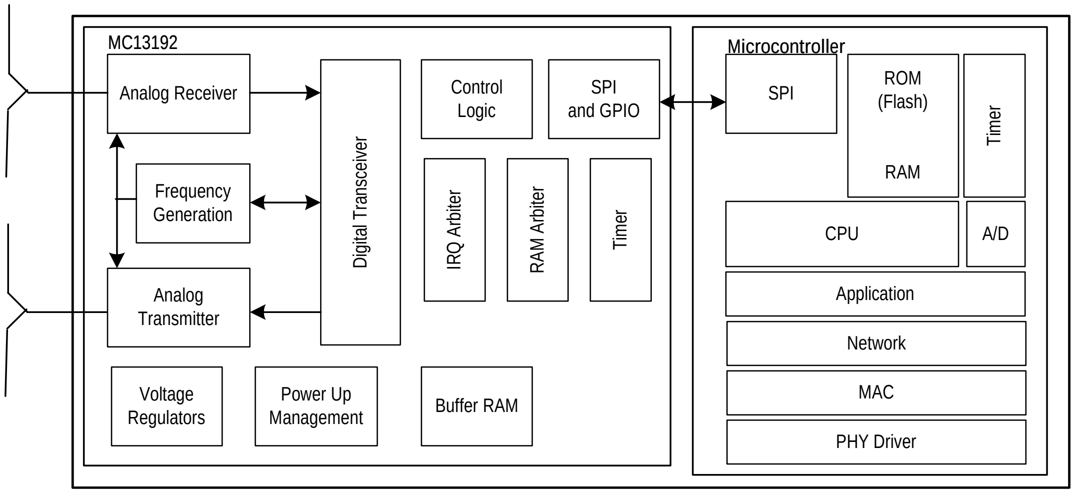
MC13192
Analog Receiver
Frequency Generation
Analog Transmitter
Digital Transceiver
Control Logic
SPI and GPIO
IRQ Arbiter
RAM Arbiter
Timer
Voltage Regulators
Power Up Management
Buffer RAM
Microcontroller
SPI
ROM (Flash)
RAM
Timer
CPU
A/D
Application
Network
MAC
PHY Driver

Figure 2. System Level Block Diagram

4 Data Transfer Modes

The MC13192 has two data transfer modes:

1. Packet Mode — Data is buffered in on-chip RAM
2. Streaming Mode — Data is processed word-by-word

The Freescale 802.15.4 MAC software only supports the streaming mode of data transfer. For proprietary applications, packet mode can be used to conserve MCU resources.

4.1 Packet Structure

Figure 3 shows the packet structure of the MC13192. Payloads of up to 125 bytes are supported. The MC13192 adds a four-byte preamble, a one-byte Start of Frame Delimiter (SFD), and a one-byte Frame Length Indicator (FLI) before the data. A two-byte Frame Check Sequence (FCS) is calculated and appended to the end of the data.

4 bytes	1 byte	1 byte	125 bytes maximum	2 bytes
Preamble	SFD	FLI	Payload Data	FCS

Figure 3. MC13192 Packet Structure

4.2 Receive Path Description

In the receive signal path, the RF input is converted to low IF In-phase and Quadrature (I & Q) signals through two down-conversion stages. A Clear Channel Assessment (CCA) can be performed based upon the baseband energy integrated over a specific time interval. The digital back end performs Differential Chip Detection (DCD), the correlator “de-spreads” the Direct Sequence Spread Spectrum (DSSS) Offset QPSK (O-QPSK) signal, determines the symbols and packets, and detects the data.

The preamble, SFD, and FLI are parsed and used to detect the payload data and FCS which are stored in RAM. A two-byte FCS is calculated on the received data and compared to the FCS value appended to the transmitted data, which generates a Cyclical Redundancy Check (CRC) result. Link Quality is measured over a 64 µs period after the packet preamble and stored in RAM.

If the MC13192 is in packet mode, the data is processed as an entire packet. The MCU is notified that an entire packet has been received via an interrupt.

If the MC13192 is in streaming mode, the MCU is notified by an interrupt on a word-by-word basis.

Figure 4 shows CCA reported power level versus input power. Note that CCA reported power saturates at about -57 dBm input power which is well above 802.15.4 Standard requirements.

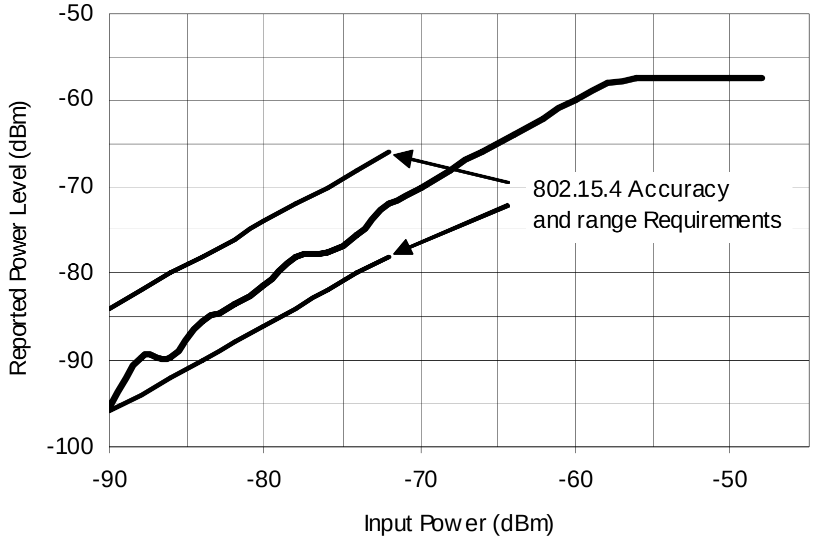

Figure 4. Reported Power Level versus Input Power in Clear Channel Assessment Mode

Figure 5 shows energy detection/LQI reported level versus input power.

NOTE

For both graphs the required 802.15.4 Standard accuracy and range limits are shown.

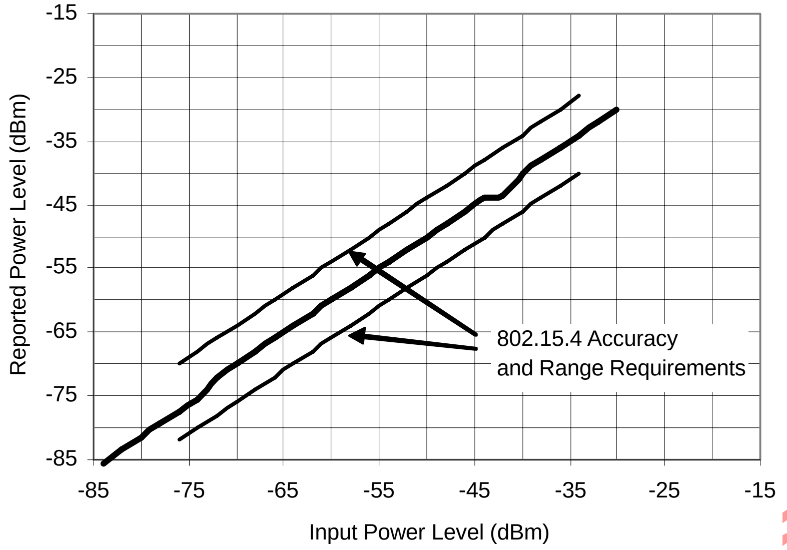

Figure 5. Reported Power Level Versus Input Power for Energy Detect or Link Quality Indicator

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4.3 Transmit Path Description

For the transmit path, the TX data that was previously stored in RAM is retrieved (packet mode) or the TX data is clocked in via the SPI (stream mode), formed into packets per the 802.15.4 PHY, spread, and then up-converted to the transmit frequency.

If the MC13192 is in packet mode, data is processed as an entire packet. The data is first loaded into the TX buffer. The MCU then requests that the MC13192 transmit the data. The MCU is notified via an interrupt when the whole packet has successfully been transmitted.

In streaming mode, the data is fed to the MC13192 on a word-by-word basis with an interrupt serving as a notification that the MC13192 is ready for more data. This continues until the whole packet is transmitted.

5 Electrical Characteristics

5.1 Maximum Ratings

Table 1. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{BATT}, V_{DDINT}	-0.3 to 3.6	Vdc
Digital Input Voltage	Vin	-0.3 to (V_{DDINT} + 0.3)	
RF Input Power	P_{max}	10	dBm
Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	-55 to 125	°C

Note: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics or Recommended Operating Conditions tables.

Note: ESD protection meets Human Body Model (HBM) = 2 kV. RF input/output pins have no ESD protection.

5.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (V_{BATT} = V_{DDINT})[1]	$V_{BATT,}$ V_{DDINT}	2.0	2.7	3.4	Vdc
Input Frequency	f_{in}	2.405	-	2.480	GHz
Ambient Temperature Range	T_A	-40	25	85	°C
Logic Input Voltage Low	V_{IL}	0	-	30% V_{DDINT}	V
Logic Input Voltage High	V_{IH}	70% V_{DDINT}	-	V_{DDINT}	V
SPI Clock Rate	f_{SPI}	-	-	8.0	MHz
RF Input Power	P_{max}	-	-	10	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	f_{ref}	16 MHz Only			

[1] If the supply voltage is produced by a switching DC-DC converter, ripple should be less than 100 mV peak-to-peak.

5.3 DC Electrical Characteristics

Table 3. DC Electrical Characteristics
(V_{BATT}, V_{DDINT} = 2.7 V, T_A = 25 °C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current (V_{BATT} + V_{DDINT}) Off[1] Hibernate[1] Doze (No CLKO)[1,2] Idle Transmit Mode (0 dBm nominal output power) Receive Mode	 $I_{leakage}$ I_{CCH} I_{CCD} I_{CCI} I_{CCT} I_{CCR}	 - - - - - -	 0.2 1.0 35 500 30 37	 1.0 6.0 102 800 35 42	 µA µA µA µA mA mA
Input Current (V_{IN} = 0 V or V_{DDINT}) (All digital inputs)	I_{IN}	-	-	±1	µA
Input Low Voltage (All digital inputs)	V_{IL}	0	-	30% V_{DDINT}	V
Input High Voltage (all digital inputs)	V_{IH}	70% V_{DDINT}	-	V_{DDINT}	V
Output High Voltage (I_{OH} = -1 mA) (All digital outputs)	V_{OH}	80% V_{DDINT}	-	V_{DDINT}	V
Output Low Voltage (I_{OL} = 1 mA) (All digital outputs)	V_{OL}	0	-	20% V_{DDINT}	V

[1] To attain specified low power current, all GPIO and other digital IO must be handled properly. See Section 8.4, "Low Power Considerations.

[2] CLKO frequency at default value of 32.786 kHz.

5.4 AC Electrical Characteristics

NOTE

All AC parameters measured with SPI Registers at default settings except where noted and the following registers over-programmed:

Register 08 = 0xFFF7 and Register 11 = 0x20FF

Not Recommended for New Designs. Use MC1320x.

Table 4. Receiver AC Electrical Characteristics

(V_{BATT}, V_{DDINT} = 2.7 V, T_A = 25 °C, f_{ref} = 16 MHz, unless otherwise noted. Parameters measured at connector J6 of evaluation circuit.)

Characteristic	Symbol	Min	Typ	Max	Unit
Sensitivity for 1% Packet Error Rate (PER) (-40 to +85 °C)	$SENS_{per}$	-	-92	-	dBm
Sensitivity for 1% Packet Error Rate (PER) (+25 °C)		-	-92	-87	dBm
Saturation (maximum input level)	$SENS_{max}$	-	10	-	dBm
Channel Rejection for 1% PER (desired signal -82 dBm) +5 MHz (adjacent channel) -5 MHz (adjacent channel) +10 MHz (alternate channel) -10 MHz (alternate channel) >= 15 MHz		 - - - - -	 25 31 42 41 49	 - - - - -	 dB dB dB dB dB
Frequency Error Tolerance		-	-	200	kHz
Symbol Rate Error Tolerance		-	-	80	ppm

Table 5. Transmitter AC Electrical Characteristics

(V_{BATT}, V_{DDINT} = 2.7 V, T_A = 25 °C, f_{ref} = 16 MHz, unless otherwise noted. Parameters measured at connector J5 of evaluation circuit.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Spectral Density (-40 to +85 °C) Absolute limit		-	-47	-	dBm
Power Spectral Density (-40 to +85 °C) Relative limit		-	47	-	
Nominal Output Power[1]	P_{out}	-3	0	3	dBm
Maximum Output Power[2]			4		dBm
Error Vector Magnitude	EVM	-	20	35	%
Output Power Control Range (-27 dBm to +4 dBm typical)		-	31	-	dB
Over the Air Data Rate		-	250	-	kbps
2nd Harmonic		-	-42	-	dBc
3rd Harmonic		-	-44	-	dBc

[1] SPI Register 12 programmed to 0x00BC which sets output power to nominal (0 dBm typical).

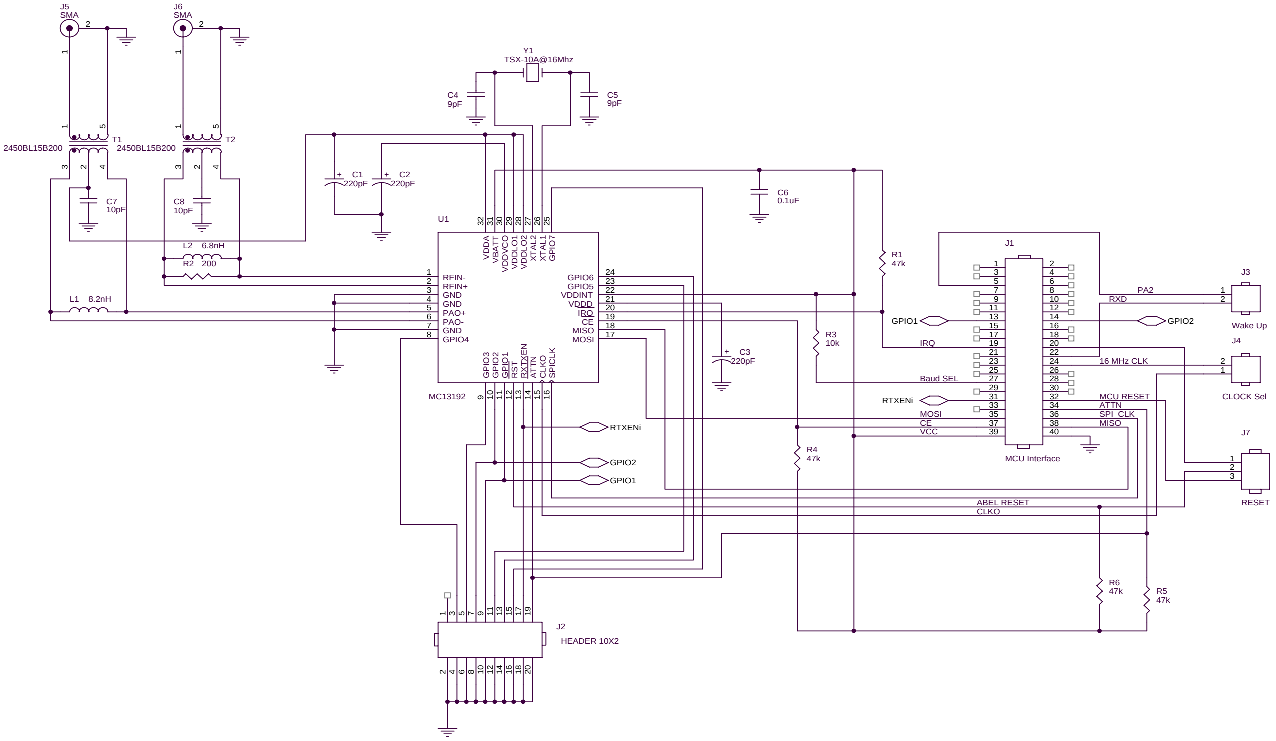
[2] SPI Register 12 programmed to 0x00FF which sets output power to maximum.

Table 6. Digital Timing Specifications

(VBATT, VDDINT = 2.7 V, TA = 25 °C, frequency = 16 MHz, unless otherwise noted.
SPI timing parameters are referenced to Figure 8.

Symbol	Parameter	Min	Typ	Max	Unit
T0	SPICLK period	125			nS
T1	Pulse width, SPICLK low	50			nS
T2	Pulse width, SPICLK high	50			nS
T3	Delay time, MISO data valid from falling SPICLK		15		nS
T4	Setup time, $\overline{\text{CE}}$ low to rising SPICLK		15		nS
T5	Delay time, MISO valid from $\overline{\text{CE}}$ low		15		nS
T6	Setup time, MOSI valid to rising SPICLK		15		nS
T7	Hold time, MOSI valid from rising SPICLK		15		nS
	$\overline{\text{RST}}$ minimum pulse width low (asserted)	250			nS

Figure 6 shows a typical AC parameter evaluation circuit.



J5
SMA
J6
SMA
T1
T2
2450BL15B200
C7
10pF
C8
10pF
L2 6.8nH
R2 200
L1 8.2nH
Y1
TSX-10A@16Mhz
C4
9pF
C5
9pF
C1
220pF
C2
220pF
C6
0.1uF
U1
MC13192
VDDA
VBATT
VDDVCO
VDDLO1
VDDLO2
XTAL2
XTAL1
GPIO7
RFIN-
RFIN+
GND
PAO+
PAO-
GPIO4
GPIO6
GPIO5
VDDINT
VDDD
IRQ
CE
MISO
MOSI
GPIO3
GPIO2
GPIO1
RST
RXTXEN
ATTN
CLKO
SPICLK
C3
220pF
R1
47k
R3
10k
R4
47k
R5
47k
R6
47k
J1
GPIO1
GPIO2
IRQ
Baud SEL
RTXENi
MOSI
CE
VCC
RXD
PA2
16 MHz CLK
MCU RESET
ATTN
SPI_CLK
MISO
MCU Interface
J3
Wake Up
J4
CLOCK Sel
J7
RESET
ABEL RESET
CLKO
RTXENi
GPIO2
GPIO1
J2
HEADER 10X2

Figure 6. Parameter Evaluation Circuit

6 Functional Description

6.1 MC13192 Operational Modes

The MC13192 has a number of operational modes that allow for low-current operation. Transition from the Off to Idle mode occurs when $\overline{\text{RST}}$ is negated. Once in Idle, the SPI is active and is used to control the IC. Transition to Hibernate and Doze modes is enabled via the SPI. These modes are summarized, along with the transition times, in Table 7. Current drain in the various modes is listed in Table 3, DC Electrical Characteristics.

Not Re
Use
for New Designs

Table 7. MC13192 Mode Definitions and Transition Times

Mode	Definition	Transition Time To or From Idle
Off	All IC functions Off, Leakage only. $\overline{\text{RST}}$ asserted. Digital outputs are tri-stated including $\overline{\text{IRQ}}$	10 - 25 ms to Idle
Hibernate	Crystal Reference Oscillator Off. (SPI not functional.) IC Responds to $\overline{\text{ATTN}}$. Data is retained.	7 - 20 ms to Idle
Doze	Crystal Reference Oscillator On but CLKO output available only if Register 7, Bit 9 = 1 for frequencies of 1 MHz or less. (SPI not functional.) Responds to ATTN and can be programmed to enter Idle Mode through an internal timer comparator.	(300 + 1/CLKO) µs to Idle
Idle	Crystal Reference Oscillator On with CLKO output available. SPI active.	
Receive	Crystal Reference Oscillator On. Receiver On.	144 µs from Idle
Transmit	Crystal Reference Oscillator On. Transmitter On.	144 µs from Idle

6.2 Serial Peripheral Interface (SPI)

The host microcontroller directs the MC13192, checks its status, and reads/writes data to the device through the 4-wire SPI port. The transceiver operates as a SPI slave device only. A transaction between the host and the MC13192 occurs as multiple 8-bit bursts on the SPI. The SPI signals are:

1. Chip Enable ($\overline{\text{CE}}$) - A transaction on the SPI port is framed by the active low $\overline{\text{CE}}$ input signal. A transaction is a minimum of 3 SPI bursts and can extend to a greater number of bursts.
2. SPI Clock (SPICLK) - The host drives the SPICLK input to the MC13192. Data is clocked into the master or slave on the leading (rising) edge of the return-to-zero SPICLK and data out changes state on the trailing (falling) edge of SPICLK.

NOTE

> For Freescale microcontrollers, the SPI clock format is the clock phase control bit CPHA = 0 and the clock polarity control bit CPOL = 0.

3. Master Out/Slave In (MOSI) - Incoming data from the host is presented on the MOSI input.
4. Master In/Slave Out (MISO) - The MC13192 presents data to the master on the MISO output.

A typical interconnection to a microcontroller is shown in Figure 7.

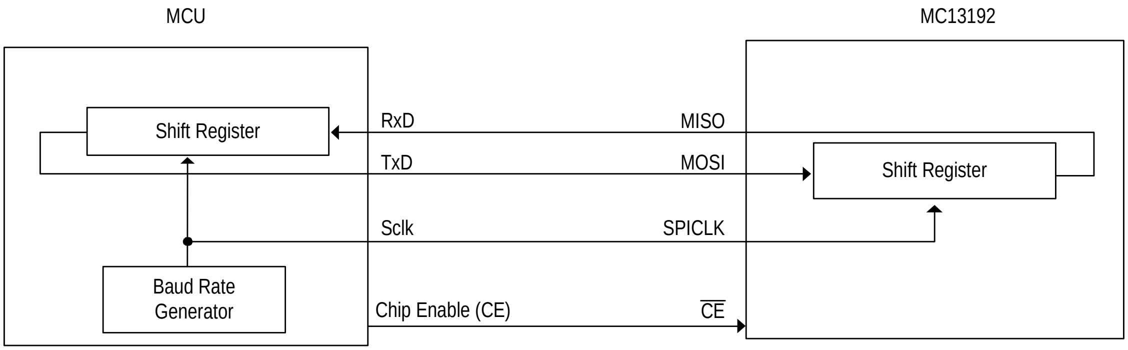

MCU
MC13192
Shift Register
RxD
MISO
TxD
MOSI
Shift Register
Sclk
SPICLK
Baud Rate Generator
Chip Enable (CE)
$\overline{\text{CE}}$

Figure 7. SPI Interface

Although the SPI port is fully static, internal memory, timer and interrupt arbiters require an internal clock (CLK_{core}), derived from the crystal reference oscillator, to communicate from the SPI registers to internal registers and memory.

6.2.1 SPI Burst Operation

The SPI port of an MCU transfers data in bursts of 8 bits with most significant bit (MSB) first. The master (MCU) can send a byte to the slave (transceiver) on the MOSI line and the slave can send a byte to the master on the MISO line. Although an MC13192 transaction is three or more SPI bursts long, the timing of a single SPI burst is shown in Figure 8.

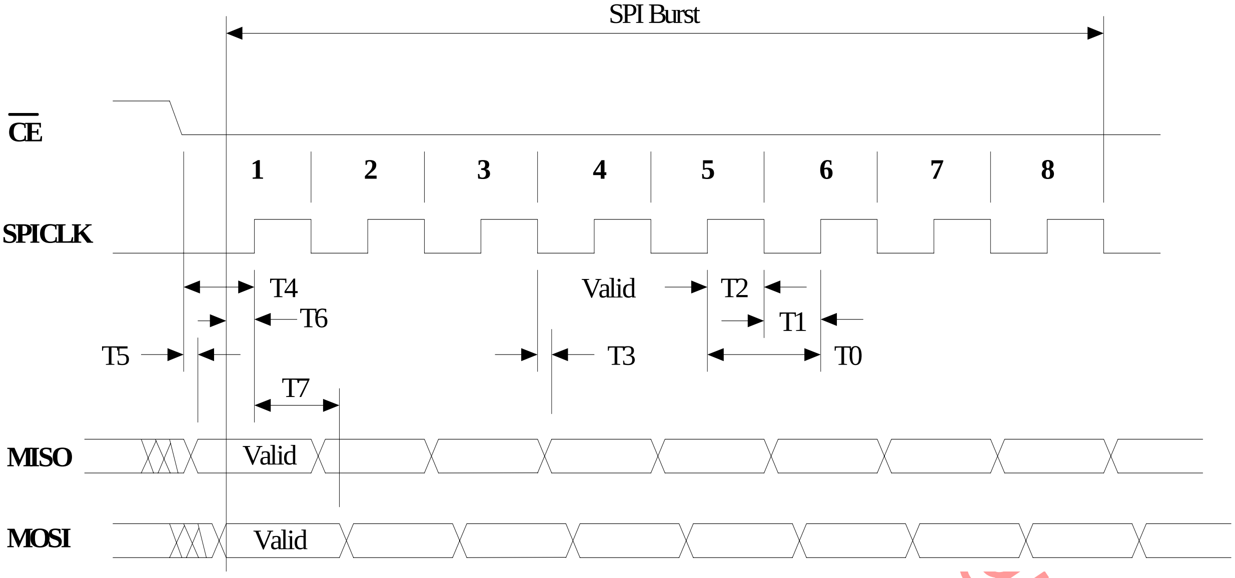

SPI Burst
$\overline{\text{CE}}$
1
2
3
4
5
6
7
8
SPICLK
T4
T6
T5
T7
Valid
T2
T1
T3
T0
MISO
Valid
MOSI
Valid

Figure 8. SPI Single Burst Timing Diagram

SPI digital timing specifications are shown in Table 6.

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6.2.2 SPI Transaction Operation

Although the SPI port of an MCU transfers data in bursts of 8 bits, the MC13192 requires that a complete SPI transaction be framed by $\overline{\text{CE}}$, and there will be three (3) or more bursts per transaction. The assertion of $\overline{\text{CE}}$ to low signals the start of a transaction. The first SPI burst is a write of an 8-bit header to the transceiver (MOSI is valid) that defines a 6-bit address of the internal resource being accessed and identifies the access as being a read or write operation. In this context, a write is data written to the MC13192 and a read is data written to the SPI master. The following SPI bursts will be either the write data (MOSI is valid) to the transceiver or read data from the transceiver (MISO is valid).

Although the SPI bus is capable of sending data simultaneously between master and slave, the MC13192 never uses this mode. The number of data bytes (payload) will be a minimum of 2 bytes and can extend to a larger number depending on the type of access. After the final SPI burst, $\overline{\text{CE}}$ is negated to high to signal the end of the transaction. Refer to the *MC13192 Reference Manual*, (MC13192RM) for more details on SPI registers and transaction types.

An example SPI read transaction with a 2-byte payload is shown in Figure 9.

Not Recomm Use MC13 r New Designs.

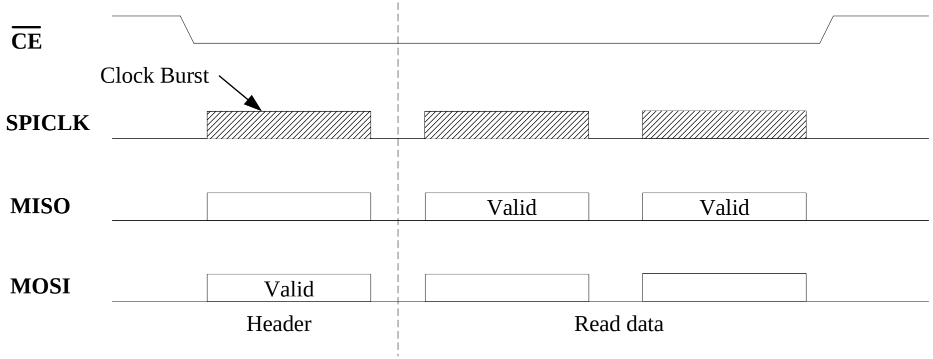


Figure 9. SPI Read Transaction Diagram

7 Pin Connections

Table 8. Pin Function Description

Pin #	Pin Name	Type	Description	Functionality
1	RFIN-	RF Input	LNA negative differential input.	
2	RFIN+	RF Input	LNA positive differential input.	
3	Not Used		Tie to Ground.	
4	Not Used		Tie to Ground.	
5	PAO+	RF Output /DC Input	Power Amplifier Positive Output. Open drain. Connect to V_{DDA}.	
6	PAO-	RF Output/DC Input	Power Amplifier Negative Output. Open drain. Connect to V_{DDA}.	
7	SM		Test mode pin. Tie to Ground	Tie to Ground for normal operation
8	GPIO4[1]	Digital Input/ Output	General Purpose Input/Output 4.	See Footnote 1
9	GPIO3[1]	Digital Input/ Output	General Purpose Input/Output 3.	See Footnote 1
10	GPIO2[1]	Digital Input/ Output	General Purpose Input/Output 2. When gpio_alt_en, Register 9, Bit 7 = 1, GPIO2 functions as a “CRC Valid” indicator.	See Footnote 1
11	GPIO1[1]	Digital Input/ Output	General Purpose Input/Output 1. When gpio_alt_en, Register 9, Bit 7 = 1, GPIO1 functions as an “Out of Idle” indicator.	See Footnote 1
12	$\overline{\text{RST}}$	Digital Input	Active Low Reset. While held low, the IC is in Off Mode and all internal information is lost from RAM and SPI registers. When high, IC goes to IDLE Mode, with SPI in default state.	
13	RXTXEN[2]	Digital Input	Active High. Low to high transition initiates RX or TX sequence depending on SPI setting. Should be taken high after SPI programming to start RX or TX sequence and should be held high through the sequence. After sequence is complete, return RXTXEN to low. When held low, forces Idle Mode.	See Footnote 2
14	$\overline{\text{ATTN}}$[2]	Digital Input	Active Low Attention. Transitions IC from either Hibernate or Doze Modes to Idle.	See Footnote 2
15	CLKO	Digital Output	Clock output to host MCU. Programmable frequencies of: 16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, 62.5 kHz, 32.786+ kHz (default), and 16.393+ kHz.	
16	SPICLK[2]	Digital Clock Input	External clock input for the SPI interface.	See Footnote 2
17	MOSI[2]	Digital Input	Master Out/Slave In. Dedicated SPI data input.	See Footnote 2
18	MISO[3]	Digital Output	Master In/Slave Out. Dedicated SPI data output.	See Footnote 3
19	$\overline{\text{CE}}$[2]	Digital Input	Active Low Chip Enable. Enables SPI transfers.	See Footnote 2

Table 8. Pin Function Description (continued)

Pin #	Pin Name	Type	Description	Functionality
20	$\overline{\text{IRQ}}$	Digital Output	Active Low Interrupt Request.	Open drain device. Programmable 40 kΩ internal pull-up. Interrupt can be serviced every 6 µs with <20 pF load. Optional external pull-up must be >4 kΩ.
21	VDDD	Power Output	Digital regulated supply bypass.	Decouple to ground.
22	VDDINT	Power Input	Digital interface supply & digital regulator input. Connect to Battery.	2.0 to 3.4 V. Decouple to ground.
23	GPIO5[1]	Digital Input/Output	General Purpose Input/Output 5.	See Footnote 1
24	GPIO6[1]	Digital Input/Output	General Purpose Input/Output 6.	See Footnote 1
25	GPIO7[1]	Digital Input/Output	General Purpose Input/Output 7.	See Footnote 1
26	XTAL1	Input	Crystal Reference oscillator input.	Connect to 16 MHz crystal and load capacitor.
27	XTAL2	Input/Output	Crystal Reference oscillator output **Note:** Do not load this pin by using it as a 16 MHz source. Measure 16 MHz output at Pin 15, CLKO, programmed for 16 MHz. See the *MC13192 Reference Manual* for details.	Connect to 16 MHz crystal and load capacitor.
28	VDDLO2	Power Input	LO2 VDD supply. Connect to VDDA externally.	
29	VDDLO1	Power Input	LO1 VDD supply. Connect to VDDA externally.	
30	VDDVCO	Power Output	VCO regulated supply bypass.	Decouple to ground.
31	VBATT	Power Input	Analog voltage regulators Input. Connect to Battery.	Decouple to ground.
32	VDDA	Power Output	Analog regulated supply Output. Connect to directly VDDLO1 and VDDLO2 externally and to PAO± through a frequency trap. **Note**: Do not use this pin to supply circuitry external to the chip.	Decouple to ground.
EP	Ground		External paddle / flag ground.	Connect to ground.

---

[1] The transceiver GPIO pins default to inputs at reset. There are no programmable pullups on these pins. Unused GPIO pins should be tied to ground if left as inputs, or if left unconnected, they should be programmed as outputs set to the low state.

[2] During low power modes, input must remain driven by MCU.

[3] By default MISO is tri-stated when $\overline{\text{CE}}$ is negated. For low power operation, miso_hiz_en (Bit 11, Register 07) should be set to zero so that MISO is driven low when $\overline{\text{CE}}$ is negated.

igns.

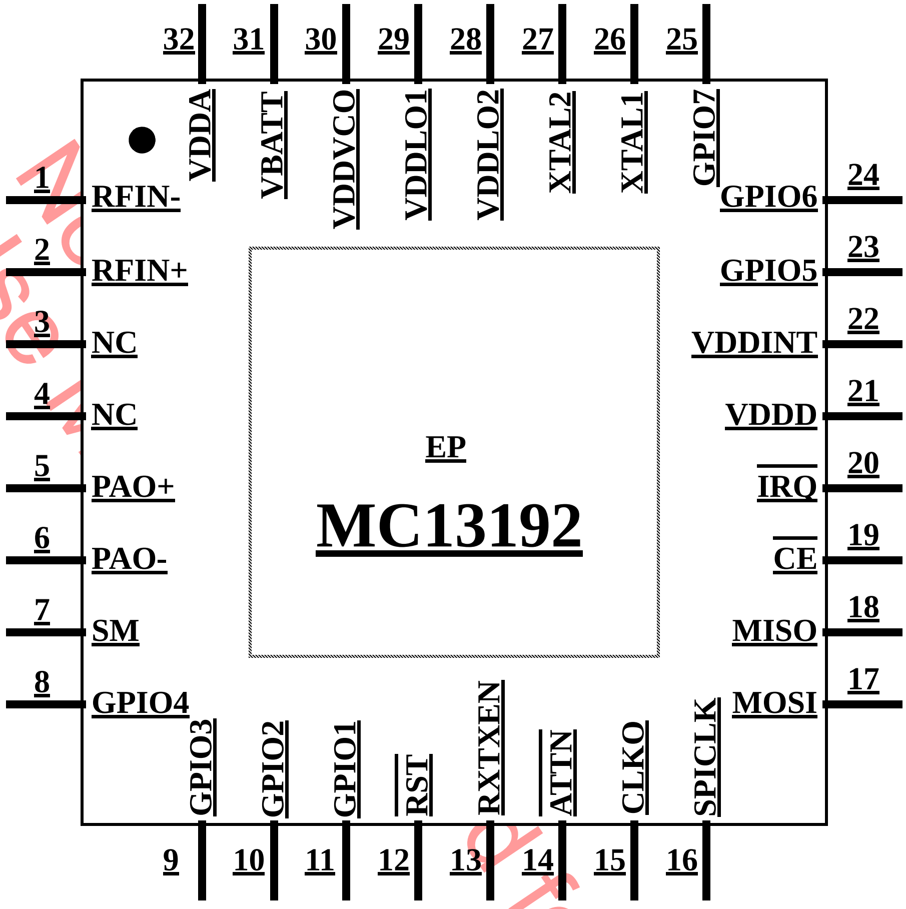

32
31
30
29
28
27
26
25
VDDA
VBATT
VDDVCO
VDDLO1
VDDLO2
XTAL2
XTAL1
GPIO7
1 RFIN-
2 RFIN+
3 NC
4 NC
5 PAO+
6 PAO-
7 SM
8 GPIO4
24 GPIO6
23 GPIO5
22 VDDINT
21 VDDD
20 IRQ
19 CE
18 MISO
17 MOSI
EP
MC13192
GPIO3
GPIO2
GPIO1
RST
RXTXEN
ATTN
CLKO
SPICLK
9
10
11
12
13
14
15
16

Figure 10. Pin Connections (Top View)

8 Applications Information

This section provides application specific information regarding crystal oscillator reference frequency, a basic design example for interfacing the MC13192 to an MCU and recommended crystal usage.

8.1 Crystal Oscillator Reference Frequency

Not Recommended for New Designs. Use MC1320x

The 802.15.4 Standard requires that several frequency tolerances be kept within ± 40 ppm accuracy. This means that a total offset up to 80 ppm between transmitter and receiver will still result in acceptable performance. The MC13192 transceiver provides onboard crystal trim capacitors to assist in meeting this performance.

The primary determining factor in meeting this specification is the tolerance of the crystal oscillator reference frequency. A number of factors can contribute to this tolerance and a crystal specification will quantify each of them:

1. The initial (or make) tolerance of the crystal resonant frequency itself.
2. The variation of the crystal resonant frequency with temperature.
3. The variation of the crystal resonant frequency with time, also commonly known as aging.
4. The variation of the crystal resonant frequency with load capacitance, also commonly known as pulling. This is affected by:
    a) The external load capacitor values - initial tolerance and variation with temperature.
    b) The internal trim capacitor values - initial tolerance and variation with temperature.
    c) Stray capacitance on the crystal pin nodes - including stray on-chip capacitance, stray package capacitance and stray board capacitance; and its initial tolerance and variation with temperature.

Freescale requires the use of a 16 MHz crystal with a <9 pF load capacitance. The MC13192 does not contain a reference divider, so 16 MHz is the only frequency that can be used. A crystal requiring higher load capacitance is prohibited because a higher load on the amplifier circuit may compromise its performance. The crystal manufacturer defines the load capacitance as that total external capacitance seen across the two terminals of the crystal. The oscillator amplifier configuration used in the MC13192 requires two balanced load capacitors from each terminal of the crystal to ground. As such, the capacitors are seen to be in series by the crystal, so each must be <18 pF for proper loading.

In the reference schematic, the external load capacitors are shown as 6.8 pF each, used in conjunction with a crystal that requires an 8 pF load capacitance. The default internal trim capacitor value (2.4 pF) and stray capacitance total value (6.8 pF) sum up to 9.2 pF giving a total of 16 pF. The value for the stray capacitance was determined empirically assuming the default internal trim capacitor value and for a specific board layout. A different board layout may require a different external load capacitor value. The on-chip trim capability may be used to determine the closest standard value by adjusting the trim value via the SPI and observing the frequency at CLKO. Each internal trim load capacitor has a trim range of approximately 5 pF in 20 fF steps.

Initial tolerance for the internal trim capacitance is approximately ±15%.

Since the MC13192 contains an on-chip reference frequency trim capability, it is possible to trim out virtually all of the initial tolerance factors and put the frequency within 0.12 ppm on a board-by-board basis.

A tolerance analysis budget may be created using all the previously stated factors. It is an engineering judgment whether the worst case tolerance will assume that all factors will vary in the same direction or if the various factors can be statistically rationalized using RSS (Root-Sum-Square) analysis. The aging factor is usually specified in ppm/year and the product designer can determine how many years are to be assumed for the product lifetime. Taking all of the factors into account, the product designer can determine the needed specifications for the crystal and external load capacitors to meet the 802.15.4 Standard.

8.2 Design Example

Figure 11 shows a basic application schematic for interfacing the MC13192 with an MCU. Table 9 lists the Bill of Materials (BOM).

The MC13192 has differential RF inputs and outputs that are well suited to balanced printed wire antenna structures. Alternatively, as in the application circuit, a printed wire antenna, a chip antenna, or other single-ended structures can be used with commercially available chip baluns or microstrip equivalents. PAO+ and PAO- require a DC connection to VDDA (the analog regulator output) through AC blocking elements. This is accomplished through the baluns in the referenced design.

The 16 MHz crystal should be mounted close to the MC13192 because the crystal trim default assumes that the listed KDS Daishinku crystal (see Table 10) and the 6.8 pF load capacitors shown are used. If a different crystal is used, it should have a specified load capacitance (stray capacitance, etc.) of 9 pF or less. Other crystals are listed in Section 8.3, “Crystal Requirements.

VDDA is an analog regulator output used to supply only the onboard PA (PAO+ and PAO-) and VDDLO1 and VDDLO2 pins. VDDA should not be used to power devices external to the transceiver chip. Bypassing capacitors are critical and should be placed close to the device. Unused pins should be grounded as shown.

The SPI connections to the MCU include $\overline{\mathrm{CE}}$, MOSI, MISO, and SPICLK. The SPI can run at a frequency of 8 MHz or less. Optionally, CLKO can provide a clock to the MCU. The CLKO frequency is programmable via the SPI and has a default of 32.786+ kHz (16 MHz / 488). The $\overline{\mathrm{ATTN}}$ line can be driven by a GPIO from the MCU (as shown) or can also be controlled by a switch or other hardware. The latter approach allows the MCU to be put into a sleep mode and then awakened by CLKO when the $\overline{\mathrm{ATTN}}$ line wakes up the MC13192. RXTXEN is used to initiate receive, transmit or CCA/ED sequences under MCU control. RXTXEN must be controlled by an MCU GPIO with the connection shown. Device reset ($\overline{\mathrm{RST}}$) is controlled through a connection to an MCU GPIO.

When the MC13192 is used in Stream Mode, as with 802.15.4 MAC/PHY software, the MC13192 GPIO1 functions as an “Out of Idle” indicator and GPIO2 functions as a “CRC Valid” / Clear Channel Assessment (CCA) result indicator and are not available for general purpose use.

Not Recommended for New Designs. Use MC1320x

Use
rns.

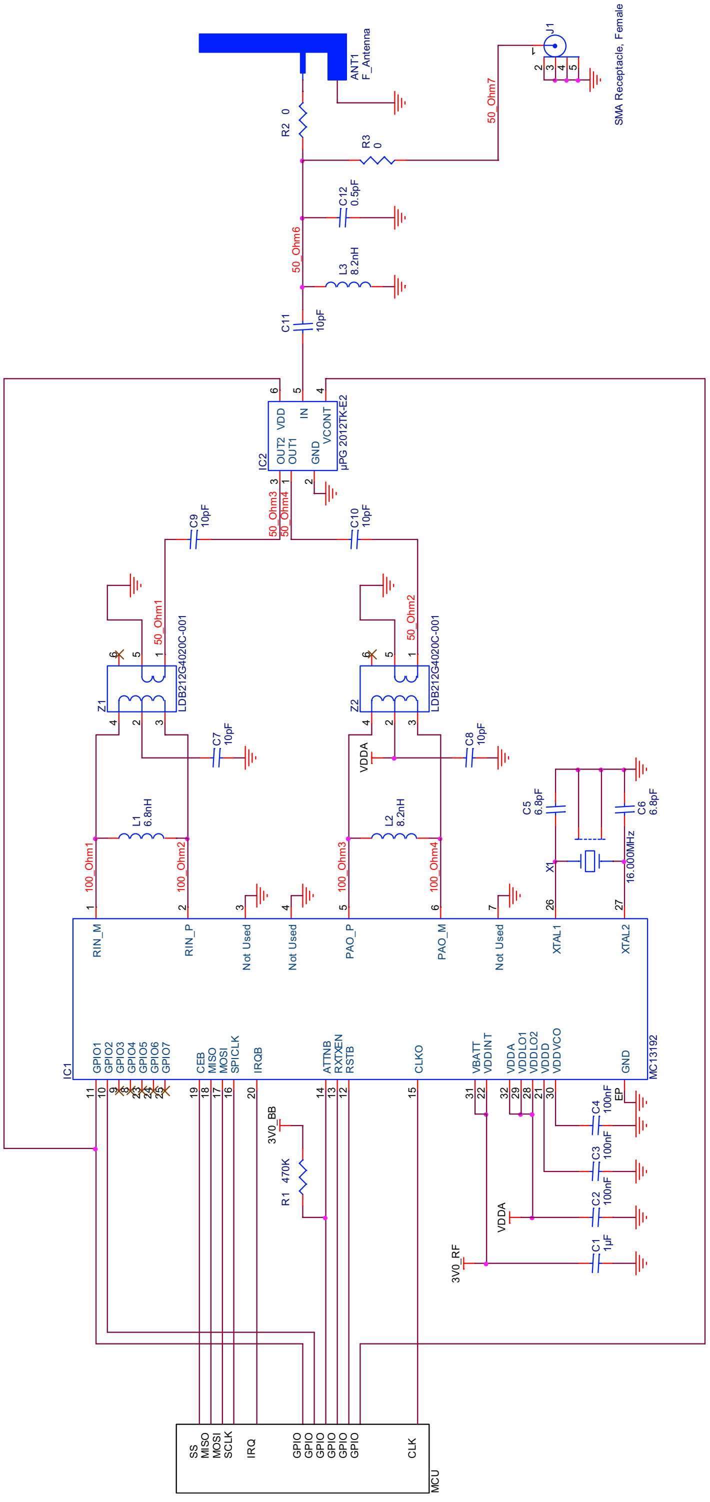

ANT1
F_Antenna
J1
SMA Receptacle, Female
R2 0
R3 0
50_Ohm7
C12 0.5pF
50_Ohm6
L3 8.2nH
C11 10pF
IC2
μPG 2012TK-E2
OUT2
OUT1
GND
VDD
IN
VCONT
50_Ohm3
50_Ohm4
C9 10pF
C10 10pF
Z1
Z2
LDB212G4020C-001
50_Ohm1
50_Ohm2
C7 10pF
C8 10pF
VDDA
L1 6.8nH
L2 8.2nH
100_Ohm1
100_Ohm2
100_Ohm3
100_Ohm4
C5 6.8pF
C6 6.8pF
X1
16.000MHz
RIN_M
RIN_P
Not Used
Not Used
PAO_P
PAO_M
Not Used
XTAL1
XTAL2
IC1
MC13192
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
CEB
MISO
MOSI
SPICLK
IRQB
ATTNB
RXTXEN
RSTB
CLKO
VBATT
VDDINT
VDDA
VDDLO1
VDDLO2
VDDD
VDDVCO
GND
EP
3V0_BB
R1 470K
C4 100nF
C3 100nF
C2 100nF
C1 1μF
VDDA
3V0_RF
SS
MISO
MOSI
SCLK
IRQ
GPIO
GPIO
GPIO
GPIO
GPIO
CLK
MCU

Figure 11. MC13192 Configured With a MCU

Not Recommended for New Designs. Use MC1320x.

Table 9. MC13192 to MCU Bill of Materials (BOM)

Item	Quantity	Reference	Part	Manufacturer
1	1	ANT1	F_Antenna	Printed wire
2	1	C1	1 µF	
3	3	C2, C3, C4	100 nF	
4	2	C5, C6	6.8 pF	
5	5	C7, C8, C9, C10, C11	10 pF	
6	1	C12	0.5 pF	
7	1	IC1	MC13192	Freescale Semiconductor
8	1	IC2	µPG2012TK-E2	NEC
9	1	J1	SMA Receptacle, Female	
10	1	L1	6.8 nH	
11	2	L2, L3	8.2 nH	
12	1	R1	470 kΩ	
13	2	R2, R3	0 Ω	
14	1	X1	16.000 MHz, Type DSX321G, ZD00882	KDS, Daishinku Corp
15	2	Z1, Z2	LDB212G4020C-001	Murata

8.3 Crystal Requirements

The suggested crystal specification for the MC13192 is shown in Table 10. A number of the stated parameters are related to desired package, desired temperature range and use of crystal capacitive load trimming. For more design details and suggested crystals, see application note *AN3251, Reference Oscillator Crystal Requirements for MC1319x, MC1320x, and MC1321x.*

Table 10. MC13192 Crystal Specifications[1]

Parameter	Value	Unit	Condition
Frequency	16.000000	MHz	
Frequency tolerance (cut tolerance)[2]	± 10	ppm	at 25 °C
Frequency stability (temperature drift)[3]	± 15	ppm	Over desired temperature range
Aging[4]	± 2	ppm	max
Equivalent series resistance[5]	43	Ω	max
Load capacitance[6]	5 - 9	pF	

Table 10. MC13192 Crystal Specifications[1] (continued)

Parameter	Value	Unit	Condition
Shunt capacitance	<2	pF	max
Mode of oscillation			fundamental

[1] User must be sure manufacturer specifications apply to the desired package.
[2] A wider frequency tolerance may acceptable if application uses trimming at production final test.
[3] A wider frequency stability may be acceptable if application uses trimming at production final test.
[4] A wider aging tolerance may be acceptable if application uses trimming at production final test.
[5] Higher ESR may be acceptable with lower load capacitance.
[6] Lower load capacitance can allow higher ESR and is better for low temperature operation in Doze mode.

Not Recommended for New Designs. Use MC1320x.

8.4 Low Power Considerations

- Program and use the modem IO pins properly for low power operation
  - All unused modem GPIOx signals must be used one of 2 ways:
    - If the Off mode is to be used as a long term low power mode, unused GPIO should be tied to ground. The default GPIO mode is an input and there will be no conflict.
    - If only Hibernate and/or Doze modes are used as long term low power modes, the GPIO should programmed as outputs in the low state.
  - When modem GPIO are used as outputs:
    - Pullup resistors should be provided (can be provided by the MCU IO pin if tied to the MCU) if the modem Off condition is to be used as a long term low power mode.
    - During Hibernate and/or Doze modes, the GPIO will retain its programmed output state.
  - If the modem GPIO is used as an input, the GPIO should be driven by its source during all low power modes or a pullup resistor should be provided.
  - Digital outputs $\overline{\text{IRQ}}$, MISO, and CLKO:
    - MISO - is always an output. During Hibernate, Doze, and active modes, the default condition is for the MISO output to go to tristate when $\overline{\text{CE}}$ is de-asserted, and this can cause a problem with the MCU because one of its inputs can float. Program Control_B Register 07, Bit 11, miso_hiz_en = 0 so that MISO is driven low when $\overline{\text{CE}}$ is de-asserted. As a result, MISO will not float when Doze or Hibernate Mode is enabled.
    - $\overline{\text{IRQ}}$ - is an open drain output (OD) and should always have a pullup resistor (typically provided by the MCU IO). $\overline{\text{IRQ}}$ acts as the interrupt request output.

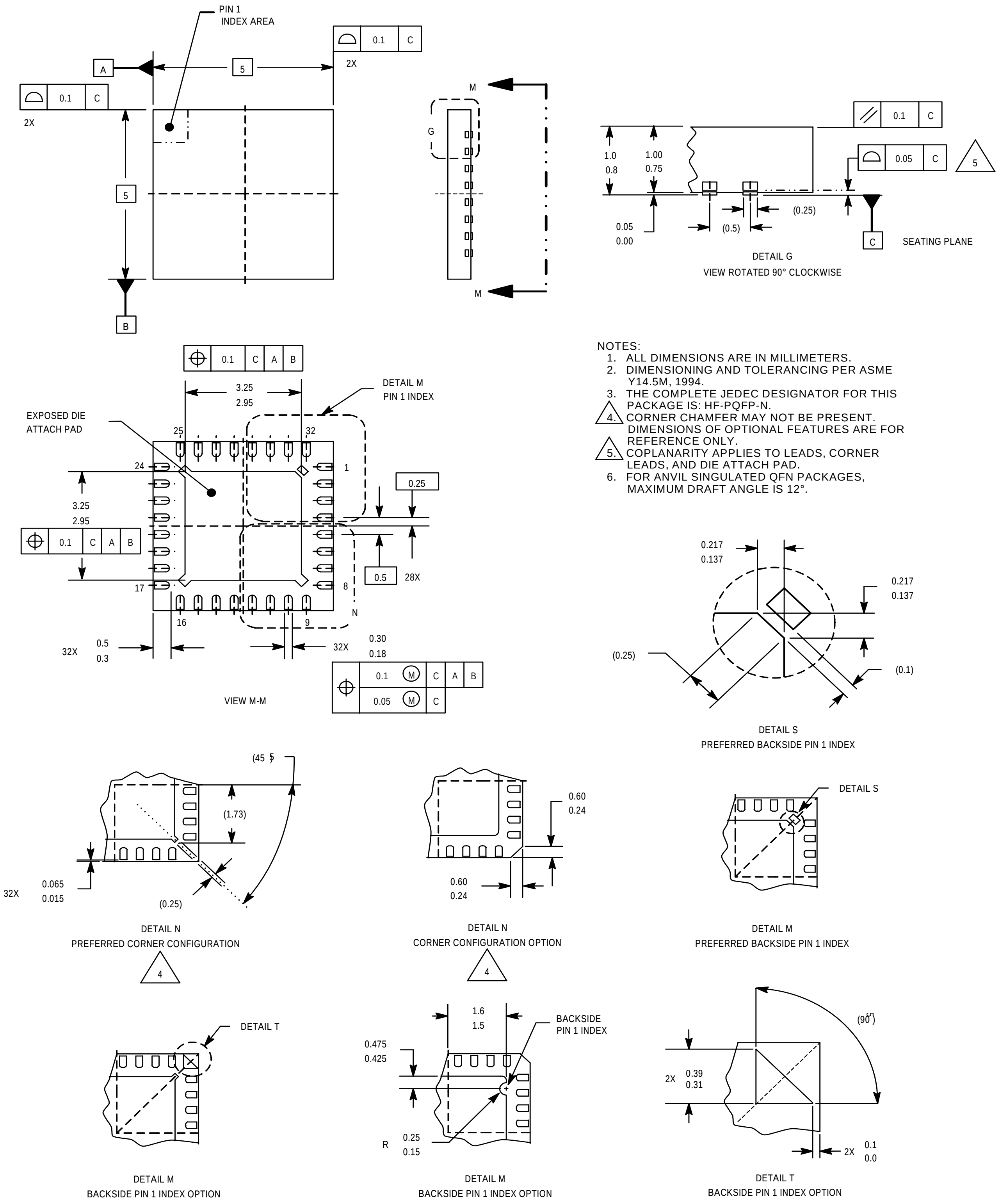
NOTE

It is good practice to have the $\overline{\text{IRQ}}$ interrupt input to the MCU disabled during the hardware reset to the modem. After releasing the modem hardware reset, the interrupt request input to the MCU can then be enabled to await the $\overline{\text{IRQ}}$ that signifies the modem is ready and in Idle mode; this can prevent a possible extraneous false interrupt request.

    - CLKO - is always an output. During Hibernate CLKO retains its output state, but does not toggle. During Doze, CLKO may toggle depending on whether it is being used.

- If the MCU is also going to be used in low power modes, be sure that all unused IO are programmed properly for low power operation (typically best case is as outputs in the low state). The MC13192 is commonly used with the Freescale MC9S08GT/GB 8-bit devices. For these MCUs:
  - — Use only STOP2 and STOP3 modes (not STOP1) with these devices where the GPIO states are retained. The MCU must retain control of the MC13192 IO during low power operation.
  - — As stated above all unused GPIO should be programmed as outputs low for lowest power and no floating inputs.
  - — MC9S08GT devices have IO signals that are not pinned-out on the package. These signals must also be initialized (even though they cannot be used) to prevent floating inputs.

9 Packaging Information


PIN 1
INDEX AREA
A
5
0.1 C
2X
5
B
M
G
M
1.0
0.8
1.00
0.75
0.05
0.00
(0.5)
(0.25)
0.1 C
0.05 C
5
C
SEATING PLANE
DETAIL G
VIEW ROTATED 90° CLOCKWISE
0.1 C A B
3.25
2.95
DETAIL M
PIN 1 INDEX
EXPOSED DIE
ATTACH PAD
25
32
24
1
0.25
3.25
2.95
17
8
0.5
28X
16
9
N
32X
0.5
0.3
32X
0.30
0.18
0.1 M C A B
0.05 M C
VIEW M-M
0.217
0.137
0.217
0.137
(0.25)
(0.1)
DETAIL S
PREFERRED BACKSIDE PIN 1 INDEX
(45°)
(1.73)
32X
0.065
0.015
(0.25)
DETAIL N
PREFERRED CORNER CONFIGURATION
4
0.60
0.24
0.60
0.24
DETAIL N
CORNER CONFIGURATION OPTION
4
DETAIL S
DETAIL M
PREFERRED BACKSIDE PIN 1 INDEX
DETAIL T
DETAIL M
BACKSIDE PIN 1 INDEX OPTION
1.6
1.5
BACKSIDE
PIN 1 INDEX
0.475
0.425
R
0.25
0.15
DETAIL M
BACKSIDE PIN 1 INDEX OPTION
(90°)
2X
0.39
0.31
2X
0.1
0.0
DETAIL T
BACKSIDE PIN 1 INDEX OPTION

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
4. CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
5. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
6. FOR ANVIL SINGULATED QFN PACKAGES, MAXIMUM DRAFT ANGLE IS 12°.

Figure 12. Outline Dimensions for QFN-32, 5x5 mm (Case 1311-03, Issue E)

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