High-Voltage Current Mode PWM Controller for ISDN Power Supplies

FEATURES

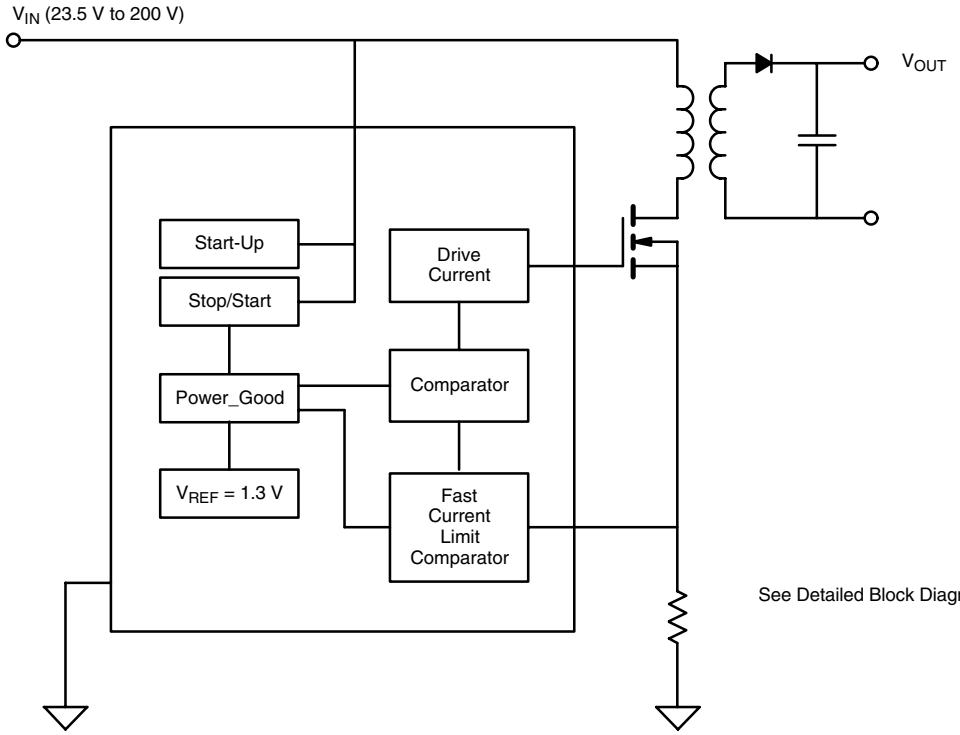
- BiC/DMOS Technology
- Current Mode Control
- Max 50% Duty Cycle Operation
- 1.3-MHz Error Amp
- Up to 500-kHz Internal Oscillator
- Soft-Start
- 0.6-V Fast Over-Current Protection
- <5-µA Supply Current for $+V_{IN}$ <18 V
- 23.5-V to 200-V Input Voltage Range
- Programmable Start/Stop Capability
- Internal Start-Up Circuit
- Power_Good Output

DESCRIPTION

Si9113 is a current mode PWM controller for ISDN power supplies. In a 14-pin SOIC package, it provides all necessary functions to implement a single-switch PWM with a minimum of external parts. To maximize the circuit integration, the Si9113 is designed with a 200-V depletion mode MOSFET capable of powering directly off the high input bus without an external start-up circuit. The Start and Stop input voltage thresholds can be programmed within the operating input voltage range by means of a resistor divider, provided $+V_{IN}$ (Start) > $+V_{IN}$ (Stop). The internal clock frequency is set with a single external resistor and is capable of capacitor-coupled external synchronization. In order to satisfy the stringent ambient temperature requirements, the Si9113 is rated to handle the industrial range of –40°C to 85°C.

The Si9113 is available in both standard and lead (Pb)-free packages.

FUNCTIONAL BLOCK DIAGRAM



See Detailed Block Diagram, page 7.

Applications information see AN728.

A Demonstration Borad data sheet is available for this product.

ABSOLUTE MAXIMUM RATINGS

V_{IN} . . . . . 220 V
V_{CC} . . . . . 18 V
Logic Inputs (OSC IN, OSC OUT, PWR_GOOD) . . . −0.3 V to V_{CC} + 0.3 V or ±10 mA
Linear Inputs (FB, V_{REF}, SENSE, SS) . . . . . −0.3 V to V_{CC} + 0.3 V
Storage Temperature . . . . . −65 to 150°C
Operating Temperature . . . . . −40 to 85°C
Junction Temperature . . . . . 150°C
Power Dissipation (Package)[a]
14-Pin SOIC (Y Suffix)[b] . . . . . 900 mW
Thermal Impedance (Θ_{JA})
14-Pin SOIC . . . . . 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C above 25°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

V_{IN} . . . . . 23.5 V to 200 V
V_{CC} . . . . . 10 V to 14 V
Digital Inputs . . . . . 0 V to V_{CC}
Linear Outputs . . . . . 0 V to V_{CC} − 3 V
F_{OSC} . . . . . 30 kHz to 500 kHz

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{OSC} = 390 kΩ	Temp[b]	Limits −40 to 85°C Min[c]	Typ[d]	Max[c]	Unit
Reference							
Output Voltage	V_{REF}	OSC_{IN} = − V_{IN} (OSC Disabled) R_L = 10 MΩ	Room Full	1.275 1.26	1.3 1.3	1.325 1.34	V
Short Circuit Current	I_{SREF}	V_{REF} = −V_{IN}	Room		−25	−10	mA
Load Regulation	ΔV_{REF}	I_{REF} = 0 to −0.5 mA	Full		±10	40	mV
Line Regulation		V_{CC} = 10 to 14 V	Full		±2	5	
UVLO							
Under Voltage Lockout	$V_{UVSTART}$	Turn-On	Full	8.10	8.8	9.50	V
	V_{UVSTOP}	Turn-Off	Full	8.10	8.8	9.50	
Input Bias Current	I_{START}	V_{STOP} = 8 V, V_{START} = 8 V	Room			0.05	µA
	I_{STOP}		Room			0.05	
Pre-Regulated V_{CC}	V_{REG}		Room	8.5	9.0	9.5	V
UVLO for V_{CC}	V_{CCUV}		Room	7.9	8.4	8.9	
V_{REG} − V_{CCUV}	VΔ		Room	0.3	0.6		
PWR_Good Comparator							
Rise Time	t_{rpg}	C_{PWR_Good} = 100 nF	Room		35		mS
Fall Time	t_{fpg}		Room		25		µS
Output Logic Low		I_{SINK} = 2.5 mA	Room		0.4	0.8	V
Soft-Start							
SS Current	I_{SS}		Room		11		µA
Output Inhibit Voltage	V_{SS}		Room		3.3		V
Oscillator							
Maximum Frequency[e]	f_{MAX}	R_{OSC} = 0	Room	500			kHz
Initial Accuracy	f_{OSC}	R_{OSC} = 390 k (Note f)	Room	80	100	120	
		R_{OSC} = 180 k (Note f)	Room	160	200	240	
Voltage Stability	Δf/f	Δf/f = (f [14 V] − f [10 V]) / f [10 V]	Room		10	15	%
Temperature Coefficient[e]	T_{OSC}		Full		450	650	ppm/°C
Maximum Duty Cycle	D_{MAX}	f_{OSC} = 100 kHz	Room		50		%

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{OSC} = 390 kΩ	Temp[b]	Limits −40 to 85°C Min[c]	Typ[d]	Max[c]	Unit
Error Amplifier							
Open Loop Voltage Gain[e]	A_{VOL}	OSC IN = – V_{IN}	Room	50	60		dB
Input BIAS Current	I_{BIAS}	V_{FB} = 1.3 V	Room	−1		1	µA
Feedback Input Voltage	V_{FB}	FB Tied to COMP, OSC IN = – V_{IN}	Full	1.28		1.32	V
Dynamic Output Impedance[e]	Z_{OUT}		Room		1	2	kΩ
Unity Gain Bandwidth[e]	BW		Room	1	1.3		MHz
Output Current	I_{OUT}	Source V_{FB} = 0.8 V	Room		−5	−1	mA
		Sink V_{FB} = 1.8 V	Room	0.12	0.15		
Power Supply Rejection[e]	PSRR		Room	50	70		dB
Current Limit Comparator							
Threshold Voltage	V_{SOURCE}	V_{FB} = 0 V	Full	0.5	0.6	0.7	V
Delay to Output[e]	t_d	V_{SENSE} = 0.85 V, See Figure 1	Full		100	150	ns
Output Drive							
Output High Voltage	V_{OH}	I_{OUT} = −10 mA	Room Full	9.7 9.5			V
Output Low Voltage	V_{OL}	I_{OUT} = 10 mA	Room Full			0.3 0.5	
Rise Time	t_r	C_L = 500 pF (10% to 90%)	Room		40	75	ns
Fall Time	t_f		Room		40	75	
Supply							
Supply Current	I_{CC}	V_{CC} = 10 V, R_{OSC} = 390 kΩ $V_{UVUP} \leq V_{IN} \leq$ 200 V	Full		1	1.4	mA
	I_{VIN}	Excluding I From Resistive Divider of Stop and Start Pins	Room		75	100	µA
Supply Current UVLO Mode	I_{VIN}	$+V_{IN} \leq$ 18 V, V_{START} (Pin 14) < 8.8 V	Room		2	5	

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Room = 25°C, Full = −40 to 85°C.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. C_{STRAY} Pin 8 = ≤ 5 pF.

TIMING WAVEFORMS

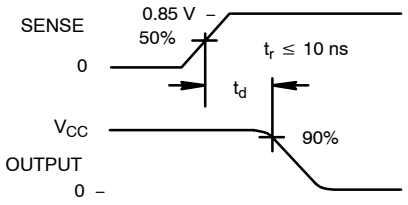
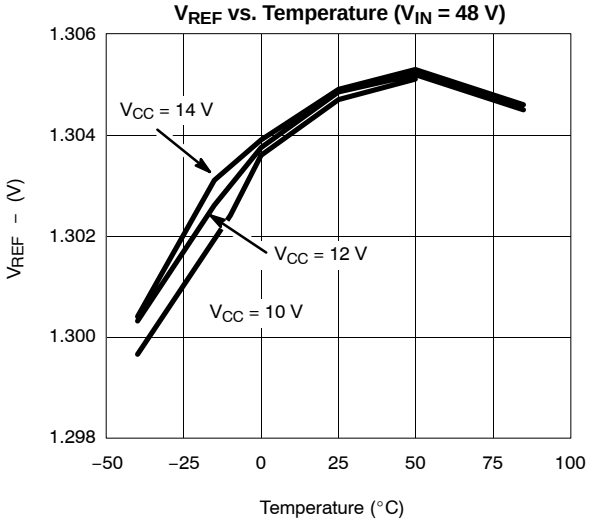


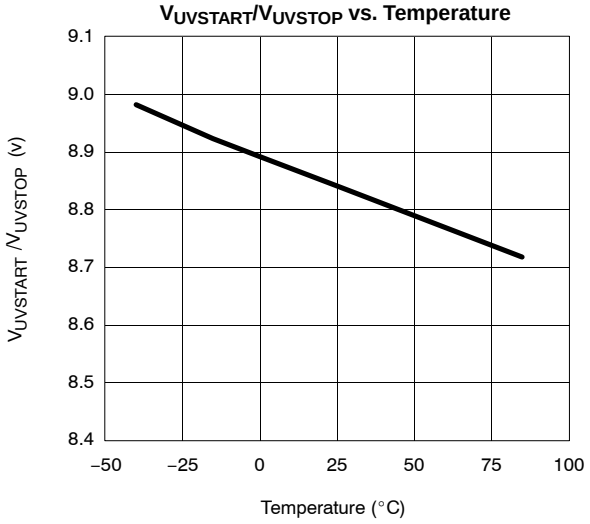
FIGURE 1. Delay Time for Current Sense

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

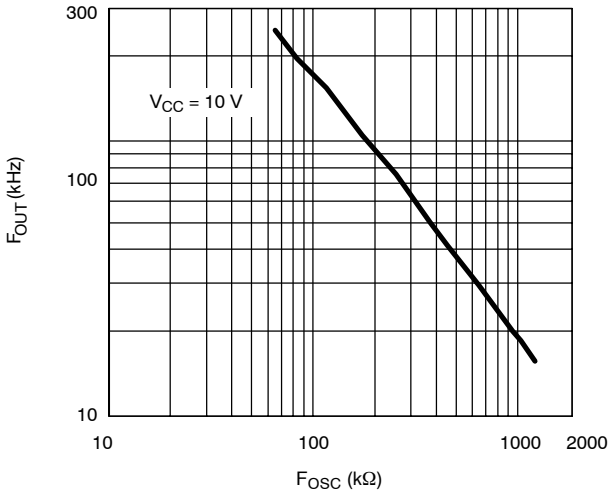
V_{REF} vs. Temperature (V_{IN} = 48 V)



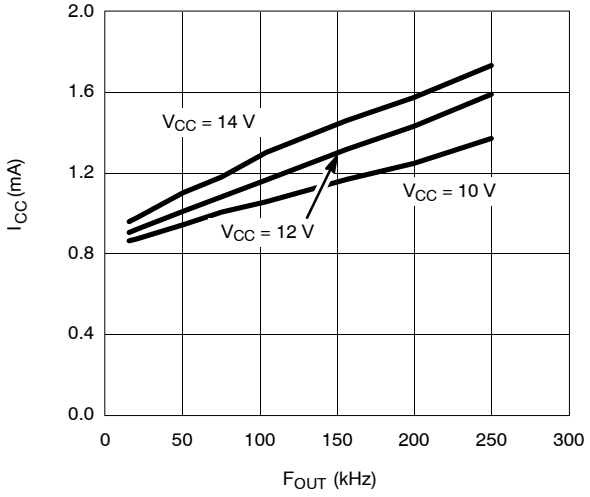
$V_{UVSTART}$/V_{UVSTOP} vs. Temperature



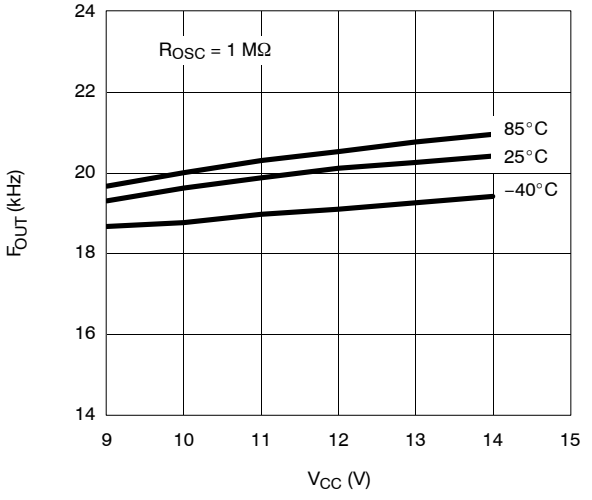
Output Frequency vs. Oscillator Resistance



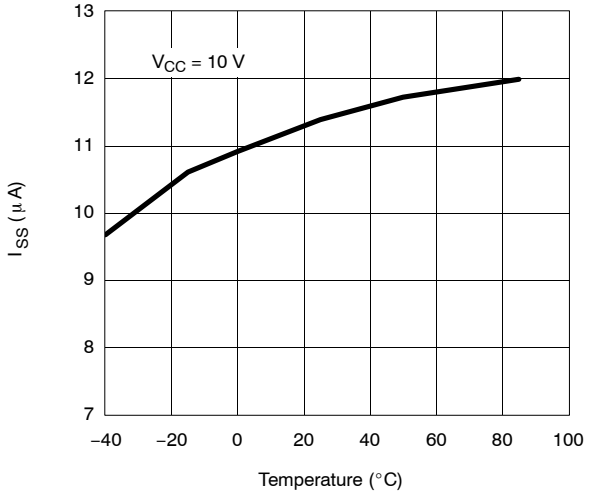
Supply Current vs. Output Frequency



Output Frequency vs. Supply Voltage

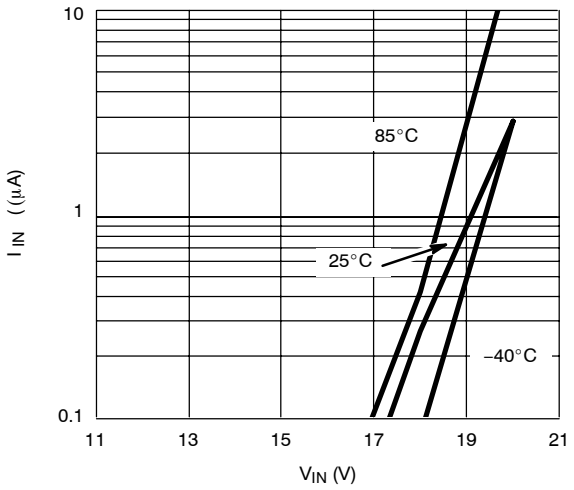


Soft-Start Current vs. Temperature

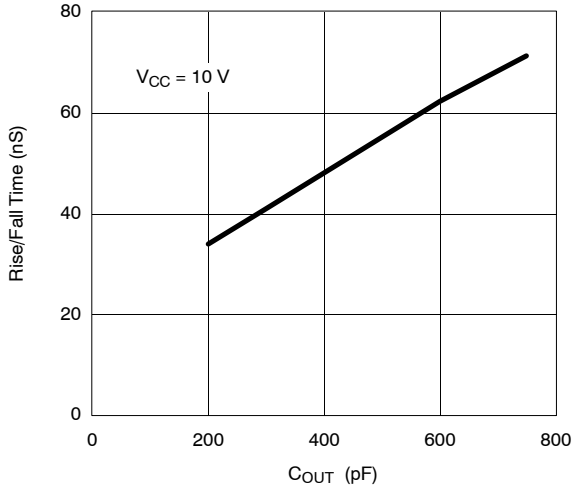


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

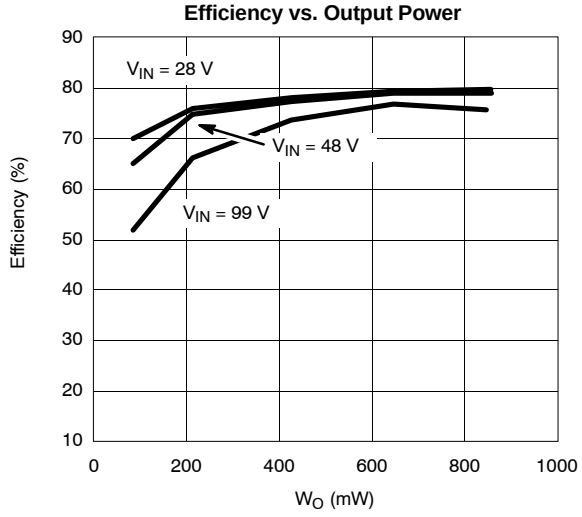
UVLO Supply Current vs. V_{IN}



Output Rise Time vs. Load

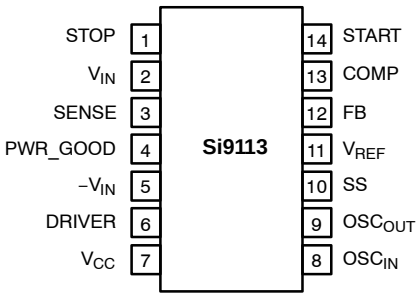


Efficiency vs. Output Power



PIN CONFIGURATION

SOIC-14



Top View

ORDERING INFORMATION

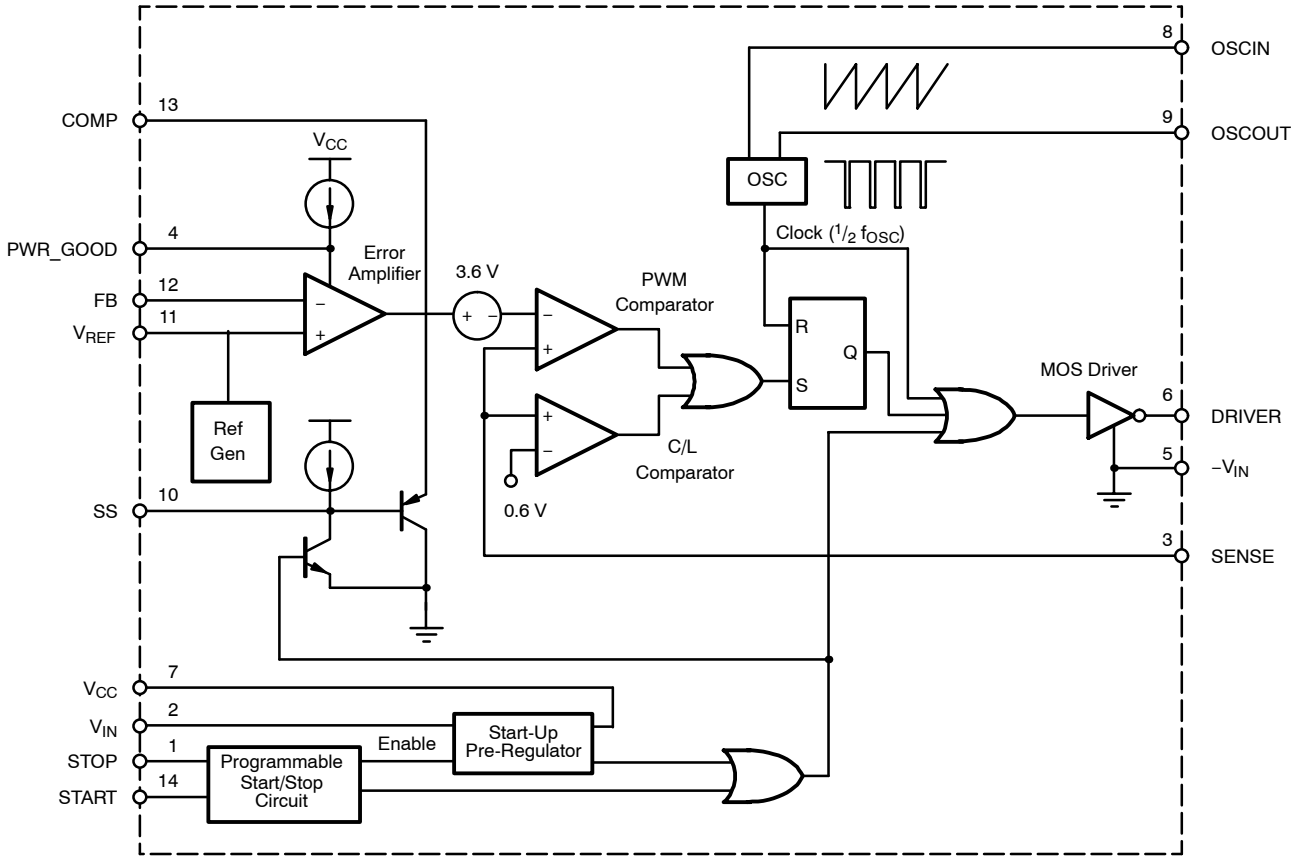
Part Number	Temperature Range	Package
Si9113DY	–40 to 85°C	Bulk
Si9113DY-T1		Tape and Reel
Si9113DY-T1—E3		

Eval Kit	Temperature Range	Board Type
Si9113D1	–10 to 70°C	Surface Mount and Thru-Hole
Si9113D2		

PIN DESCRIPTION

Pin Number	Name	Function
1	STOP	Set up the stop threshold of $+V_{IN}$ for V_{CC} via resistive dividers
2	$+V_{IN}$	Input voltage to UVLO and Start-Up circuitry
3	SENSE	Current sense amplifier input for current mode control and OCP.
4	PWR_GOOD	Logic high PWR_Good signal indicates FB voltage is within regulation.
5	$-V_{IN}$	Ground pin
6	DRIVER	MOSFET gate drive signal.
7	V_{CC}	Supply voltage to internal circuitry and MOSFET gate drive.
8	OSC_{IN}	R_{OSC} terminal
9	OSC_{OUT}	R_{OSC} terminal, square waveform output
10	SS	Soft-Start, time programmed by capacitor value.
11	V_{REF}	1.3-V reference. Decoupled with 0.1-μF capacitor.
12	FB	Inverting input of an error amplifier.
13	COMP	Error amplifier output for external compensation network.
14	START	Set up the start threshold of $+V_{IN}$ for V_{CC} via resistive dividers

DETAILED BLOCK DIAGRAM



DETAILED DESCRIPTION

Start-Up

The Si9113 start-up circuit prevents the internal circuits from turning on until the voltage on the $+V_{IN}$ pin, via the resistor divider R_3, R_4, R_5, is sufficiently positive such that the voltage across R_3 (V_{START}) is >8.8 V (typical value for the internal reference $V_{UVSTART}$ [see Figure 2]). When this occurs, the internal 1.3-V reference, soft-start and oscillator circuits are enabled. A constant current source provides the current to the external soft-start capacitor, which allows the output voltage to rise gradually without overshoot. The output drive circuit is disabled until the soft-start voltage reaches 3.3 V. The controller is continuously powered in the state until the V_{IN} voltage falls and V_{STOP} drops below 8.8 V (the typical value for the internal reference V_{UVSTOP}). The user can program the $+V_{IN}$ START and $+V_{IN}$ STOP voltage with the external resistor divider R_3–R_5 (see Figure 2) as follows:

$$V_{IN(START)} = \left(\frac{R_3 + R_4 + R_5}{R_5}\right) \times V_{UVSTART} \quad (1)$$

$$V_{IN(STOP)} = \left(\frac{R_3 + R_5}{R_5}\right) \times V_{UVSTOP} \quad (2)$$

Since $V_{UVSTART} = V_{UVSTOP} = 8.8$ V (typical) the hysteresis voltage can be expressed as:

$$\Delta V_{IN} = \left(\frac{R_4}{R_5}\right) \times V_{UVSTART} \quad (3)$$

V_{CC} Circuit

The depletion MOSFET process allows the Si9113 controller to power directly from the high input bus voltage. Once $V_{UVSTART}$ is met, the pre-regulator start-up circuit generates the 9.0-V V_{CC} voltage. The V_{CC} voltage is used internally to power the IC as well as providing the drive current for the external MOSFET. An internal V_{CC} circuit is disabled once a higher external voltage (~10 V) is applied to this pin. If V_{CC} is below V_{CCUV}, the Si9113 will inhibit the driver output switching.

REF

The reference voltage of Si9113 is set at 1.3 V. The reference voltage is internally connected to the non-inverting input of error amplifier. The reference is decoupled with 0.1-μF capacitor.

Soft-Start

The soft-start circuit provides a constant 10-μA current to external capacitor attached to SS pin. A constant soft-start current forces a gradual increase in duty cycle which in turn ensures gradual output voltage rise without overshooting. The soft-start time is programmed by the capacitance value.

Oscillator

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. An external resistor, R_{OSC}, between the OSC_{IN} and OSC_{OUT} pins sets the frequency. The maximum frequency is obtained when R_{OSC} = 0 Ω. A frequency divider in the logic section limits the switch duty cycle to 50% by locking the switching frequency to one-half of the oscillator frequency.

PWM Mode

As the load and line voltage vary, the switching frequency remains constant. The switching frequency is programmed by the R_{OSC} value as shown by the oscillator curve. In the PWM mode, a duty cycle pulse is generated for each switching period eliminating any chance of undesirable noise frequency. When the output load current decreases to 0 A, the controller is forced to enter the pulse skipping mode. This is a natural phenomenal for all controllers since the duty cycle cannot decrease linearly to 0%.

Error Amplifier

The error amplifier gain-bandwidth product and slew rate are critical parameters which determine the transient response of converter. The transient response is the function of both small and large signal responses. The small signal response is determined by the converter closed loop bandwidth and phase margin while the large signal is determined by the error amplifier dv/dt and the inductor di/dt slew rate. Besides the inductance value, the error amplifier determines the converter response time. In order to minimize the response time, the Si9113 is designed with 1.3-MHz error amplifier gain-bandwidth product to generate the widest converter bandwidth.

Current Limit

Over current protection circuit is provided by monitoring the voltage on the Sense pin. Once the current sense voltage reaches 0.6V peak, the output drive stage is disabled for the remainder of the clock cycle.

Power_Good Comparator

The PWR_Good signal indicates the status of output voltage. If the output voltage and V_{CC} are within regulation, the PWR_Good signal generates a logic high output by monitoring the voltage on COMP and V_{CC} pins. If either one is out of regulation, a logic low PWR_Good signal is generated. The capacitor at the PWR_Good pin determines the rise time of the power good signal, once all the conditions are met for power good. The PWR_Good signal is an open collector output capable of sinking 2.5 mA.

MOSFET Gate Drive

The DRIVER pin is designed to drive the low-side n-channel MOSFET. Typically, the driver stage is sized to sink and source 200-mA of peak current when V_{CC} = 12 V.

TYPICAL APPLICATION CIRCUITS

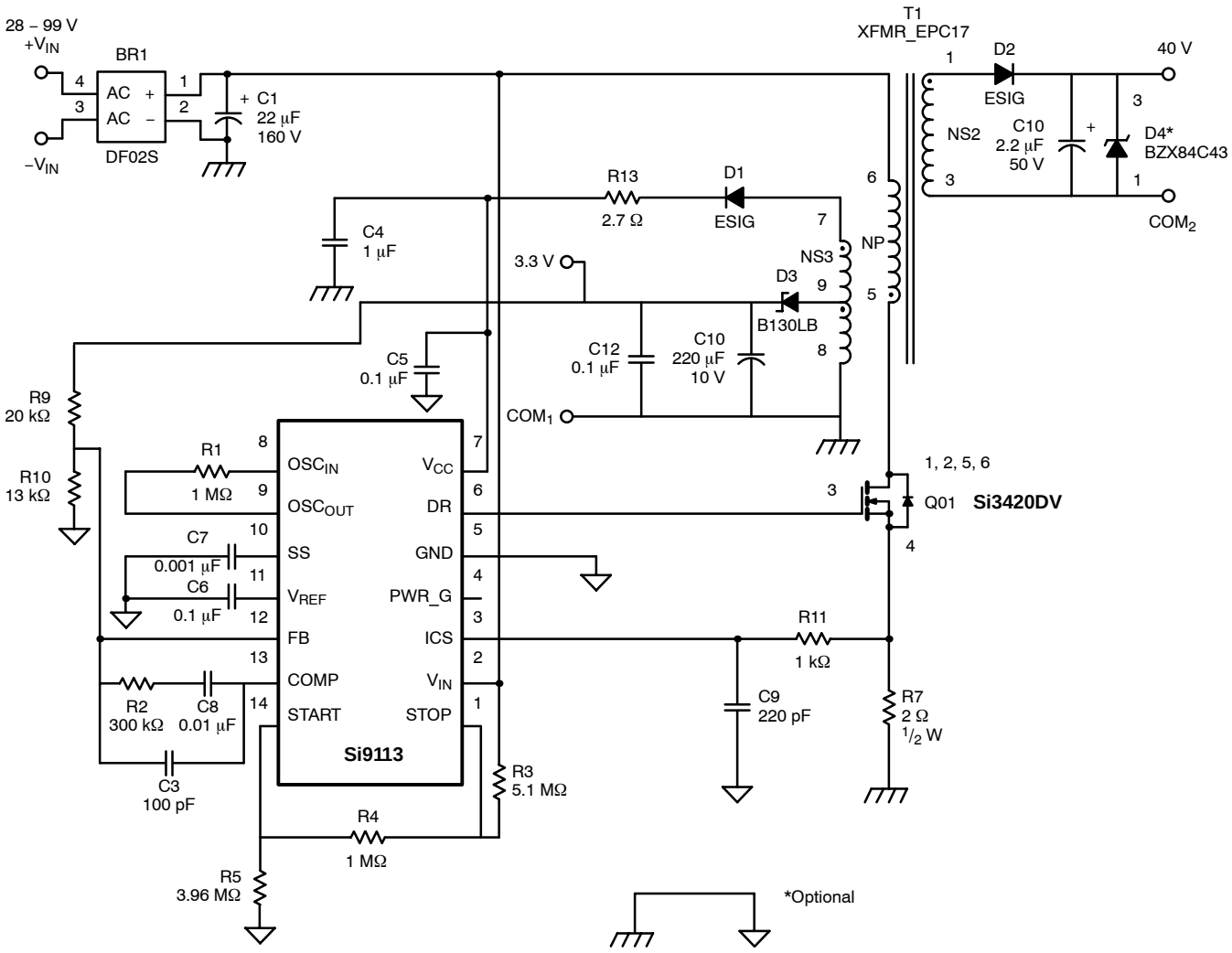


FIGURE 2. Dual Output Flyback Converter with 2% Regulation for 3.3 V
(As used on Demo Board—DB1)

TYPICAL APPLICATION CIRCUITS

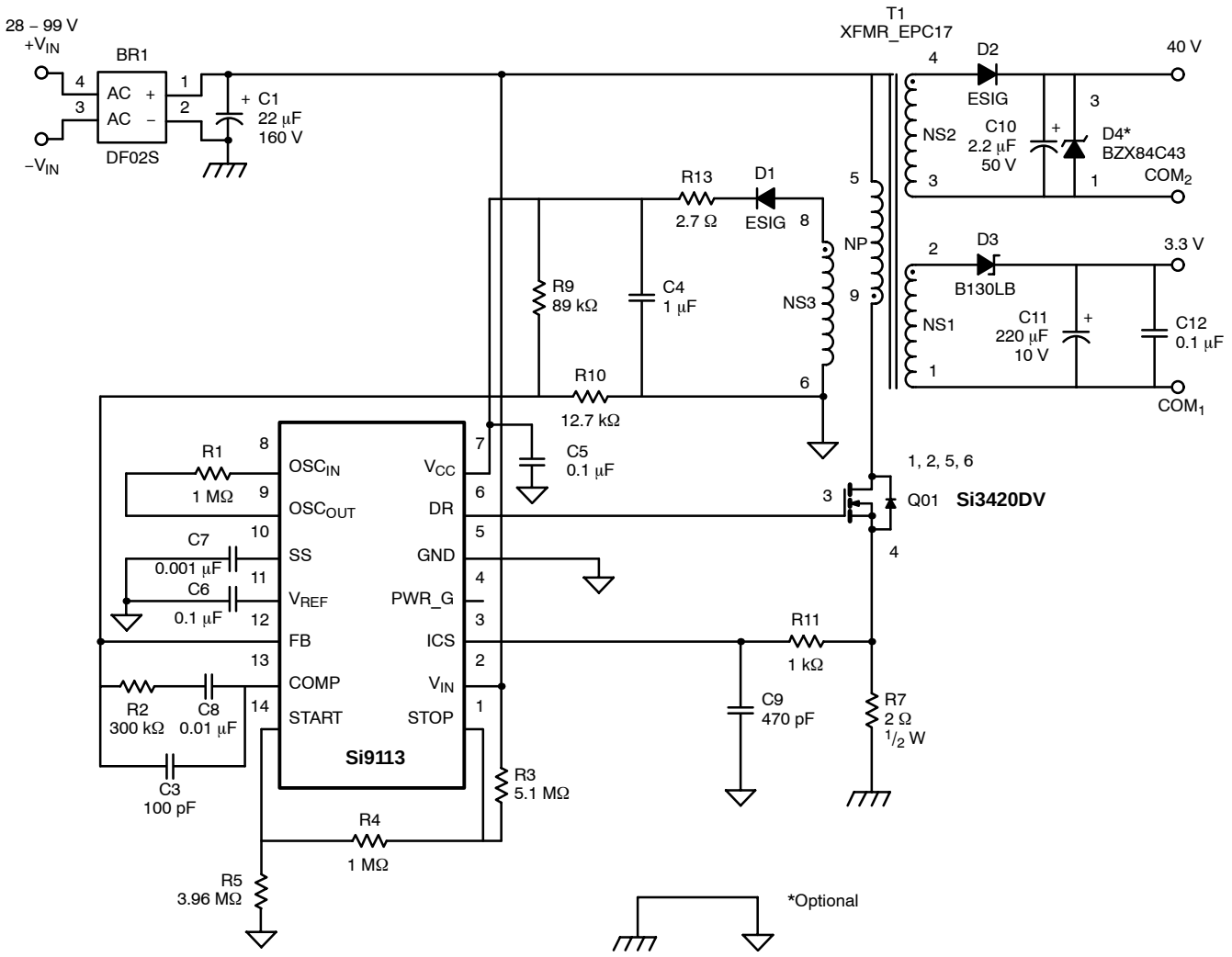
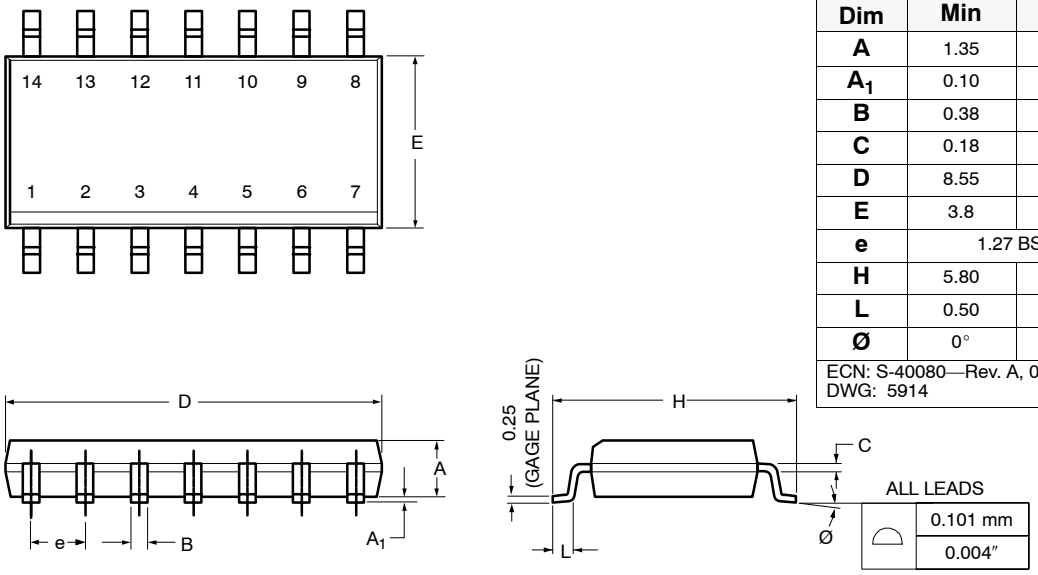


FIGURE 3. Dual Output Flyback Converter with Moderately Regulated Outputs
(As used on Demo Board DB-2)

SOIC (NARROW): 14-LEAD (POWER IC ONLY)



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	8.55	8.75	0.336	0.344
E	3.8	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
Ø	0°	8°	0°	8°

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DWG: 5914

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