# MLX90288

Datasheet

## 1. Features and Benefits

- Surface mounted device
- Analog ratiometric output
- Measurement range from ±6mT to ±650mT bipolar full scale
- Digital IIR filtering for accurate bandwidth
- Offset trimming possible outside output range
- 1st and 2nd order magnet TC compensation
- Reverse polarity and overvoltage protection
- Extensive diagnostic features

## 2. Application Examples

- Rotary position sensor
- Linear position sensor
- Proximity sensor

## 3. Description

The MLX90288 is a cost-effective monolithic programmable linear Hall sensor which provides an analog ratiometric output signal proportional to the magnetic flux density that is applied perpendicular to the die surface. The MLX90288 is fully programmable (offset, sensitivity, clamping levels, magnet temperature drift, digital IIR filtering …) through the connector, using the PTC-04 programming tool. It supports both linear and quadratic magnet Thermal Compensation.

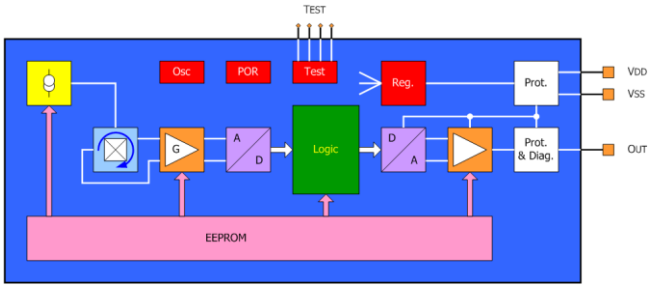



*Figure 1 gives the block diagram*

## Contents

## 4. Ordering Information

| Product | Temperature | Package | Option Code | Packing Form | Definition |
|---|---|---|---|---|---|
| MLX90288 | L | DC | CAA-000 | TU | |
| MLX90288 | L | DC | CAA-000 | RE | |
| MLX90288 | K | DC | CAA-000 | TU | |
| MLX90288 | K | DC | CAA-000 | RE | |

| | |
|---|---|
| **Temperature Code:** | **L: from -40°C to 150°C**<br>**K:from -40°C to 125°C** |
| Package Code: | "DC" for SOIC-8 package, 150Mil |
| Option Code: | CAA-000 |
| Packing Form: | "RE for Reel", "TU for Tube" |
| Ordering Example: | "MLX90288LDC-CAA-000-RE" |

*Table 1*

## 5. Glossary of Terms

| Gauss (G), Tesla (T) | Units for the magnetic flux density – 1 mT = 10 G |
|---|---|
| TC | Temperature Coefficient (in ppm/Deg.C.) |
| NC | Not Connected |
| ADC | Analog-to-Digital Converter |
| DAC | Digital-to-Analog Converter |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| DNL | Differential Non-Linearity |
| INL | Integral Non-Linearity |
| ASP | Analog Signal Processing |

| Gauss (G), Tesla (T) | Units for the magnetic flux density – 1 mT = 10 G |
|---|---|
| DSP | Digital Signal Processing |
| EMC | Electro-Magnetic Compatibility |
| FSM | Finite State Machine |

*Table 2*

## 6. Pin Definitions and Descriptions

| Pin # | Name | Description |
|---|---|---|
| 1 | VDD | Supply |
| 2 | VSS | Ground |
| 3 | N/C | Not connected |
| 4 | OUT | Analog + PTC communication |
| 5 | IDDQ | Test |
| 6 | TESTOUT | Test |
| 7 | MUST0 | Test |
| 8 | MUST1 | Test |

*Table 3 gives the pinout*

The pinout of the MLX90288 of the global pins is identical to that of the MLX90291 (PWM output), making drop-in replacements possible for multi-protocol applications. Both ICs have differences in architecture, apart from the protocol only.

## 7. Absolute Maximum Ratings

| Item | Symbol | Rating |
|---|---|---|
| Supply Forward-Voltage | $V_{DDFWD}$ | + 30 V (continuous)<br>(Breakdown at + 40 V) |
| Supply Forward-Current | $I_{DDFWD}$ | + 20 mA |

| Item | Symbol | Rating |
|---|---|---|
| Supply Reverse-Voltage | $V_{DDREV}$ | – 14.5 V (continuous)<br>(Breakdown at – 19 V) |
| Supply Reverse-Current | $I_{DDREV}$ | – 2 mA |
| Output Forward-Voltage | $V_{OUTFWD}$ | + 18 V |
| Output Forward-Current | $I_{OUTFWD}$ | – 60 mA |
| Output Reverse-Voltage | $V_{OUTREV}$ | – 14 V |
| Output Reverse-Current | $I_{OUTREV}$ | + 20 mA |
| Storage Temperature Range (Non Operating) | $T_S$ | -55°C to +165°C |
| Operating Ambient Temperature Range | $T_A$ | -40°C to +150°C |
| Junction Temperature | $T_J$ | +165°C |
| Package Thermal Resistance | $R_{TH}$ | 100 K/W |
| Maximum Flux Density | $B_{MAX}$ | 2T |

*Table 4 gives the maximum ratings.*

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

## 8. General Electrical Specifications

| Parameter | Symbol | Remark | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | Guaranteed spec operation | 4.5 | 5 | 5.5 | V |
| Supply Current | $I_{DD}$ | Worst case (min $R_{PD}$, max VDD) | - | 8.8 | 10 | mA |
| Regulated Voltage | $V_{REG}$ | Internal voltage | 3.0 | 3.3 | 3.6 | V |
| Reset Voltage | $V_{PORRISE}$ | Output is high impedant for $V_{POR} < V_{DD} < V_{UNDER}$ | 2.5 | | 3.4 | V |
| | $V_{PORFALL}$ | | 2.4 | | 3.3 | V |
| Undervoltage Threshold | $V_{UNDERRISE}$ | Operating if $V_{DD} > V_{UNDER}$ | 3.4 | | 4.4 | V |
| | $V_{UNDERFALL}$ | | 3.3 | | 4.3 | V |

| Parameter | Symbol | Remark | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Programming Voltage(1) | $V_{PROGRISE}$ | | 6.2 | | 7.2 | V |
| | $V_{PROGFALL}$ | Device not locked | 6.1 | | 7.1 | V |
| Overvoltage Threshold(2) | $V_{OVER}$ | Disconnect $V_{PROT}$ from $V_{DD}$ | 8.4 | | 14 | V |
| Load Resistance Range | $R_{PD}$ | Pull-down to GND | 8 | 10 | 330 | kΩ |
| Load capacitor range | $C_L$ | Between OUT and GND | 47 | | 1000 | nF |
| Output Saturation Voltage(3) | $V_{SATHI}$ | Including $R_{PD}$ | 96 | | 100 | $\%V_{DD}$ |
| | $V_{SATLO}$ | Including $R_{PD}$ | 0 | | 2 | $\%V_{DD}$ |
| Output Current Limitation(4) | $I_{OUTLIMGND}$ | Output amplifier sourcing strength | 2 | 5 | 8 | mA |
| | $I_{OUTLIMVDD}$ | Output amplifier sinking strength | 2 | 5 | 8 | mA |
| Supply Current Limitation | $I_{VDDLIM}$ | Same condition as above | 5 | | 18 | mA |
| Output Diagnostic Band Leakage Current(5) | $I_{DIAGLO}$ | Leakage current over $T_A$ $V_{DD}$=5V | | | 500 | nA |
| Output Diagnostic Level | $V_{DIAGLO}$ | Leakage current over $T_A$ and $V_{DD}$ span | | | $R_{PD}$ x $I_{DIAGLO}$ | V |

*Table 5 gives the electrical specifications*

(1) The programming voltage defines the threshold at which the ASIC goes into PTC mode, where the output pin becomes bidirectional. Write access is eventually defined by the locking bits as described in subsequent sections.
(2) The overvoltage threshold will disconnect all internal supplies (Vana, Vdig & Vprot) from $V_{DD}$; the output becomes high impedant.
(3) The saturation voltage is the rail voltage the output amplifier can reach actively with $R_{PD}$ connected.
(4) The maximum current the output stage can deliver to keep its DC value, in case the output is pulled to one of the rails by means of an external power supply, while $V_{DD}$ = 5V.
(5) The leakage current is in fact the current sourced by the output in case of an OBD detection (broken ground), where the output goes into high-Z mode. For better contacting at the connectors over lifetime and bigger rail-to-rail operation, the smaller pull-down resistors from this specification are recommended at ECU side.

## 9. Timing Specification

| Parameter | Symbol | Remark | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supply Slew Rate | $V_{DDSR}$ | External supply $V_{DD}$ | 5e-6 | | 5 | V/µs |

| Parameter | Symbol | Remark | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Startup time[1] | $t_{STARTUP}$ | | 200 | 500 | 800 | µs |
| Main Oscillator Frequency | $F_{OSC}$ | Tolerance ± 10% | 900 | 1000 | 1100 | kHz |
| Conversion Rate | $t_{CONV}$ | Acquisition of Hall and Temperature signals (no digital filtering) | 130 | 144 | 158 | µs |
| | $f_{CONV}$ | | 6.33 | 7 | 7.7 | kHz |
| Programmable Filtering[2] | BW | Tempsensor enabled | 0.004 | | 1.114 | kHz |
| Output Amplifier Rise Time (10%-90%)[3] | $t_{RISEPP}$ | $R_L$ = 8 kΩ to Ground<br>$C_L$ = 330 nF to Ground | | 300 | | µs |
| Output Amplifier Fall Time (90%-10%)[3] | $t_{FALLPP}$ | $R_L$ = 330 kΩ to Ground<br>$C_L$ = 330 nF to Ground | | 200 | | µs |
| Calibration Time[4] | $t_{CALIB}$ | EE Full Erase + Write | | | 6 | ms |
| | | EE Full Read | | 180 | | ms |
| | | RAM Write | | | 3 | ms |

*Table 6 gives the timing specifications*

(1) Startup time is defined as the time between crossing the POR level and having the first DAC output update. It includes loading of the parameters from EEPROM, checking the CRC validity, initializations and the signal latency between the first Hall plate acquisition and the DAC output update.
(2) Filtering is programmable with the FILTCODE parameter in EEPROM. The filter consists of an IIR filter in the digital. For more details about the corresponding bandwidths, see subsequent sections.
(3) Rise and fall times are measured for worst case conditions, hence the difference in Rload for both parameters. These specifications are only defined by the output amplifier and its load. The output amplifier (Gain=2) is given a step response at the input from 5%$V_{DD}$ to 45%$V_{DD}$ and the rise/fall times are measured as the time between reaching 10% and 90% of the step response DC output voltages (10%$V_{DD}$ to 90%$V_{DD}$).
(4) Calibration times measured at room temperature with PTC-04 and DB-HALL03 daughterboard, FIR090288AAMLX firmware loaded onto the PTC-04 and on a MLX90288 in the recommended application diagram from subsequent sections at 10kbit/s.

## 10. Transfer Characteristic Specification

| Parameter | Symbol | Remark | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Clamping Range | ClampLo | 9 bits[1] | 0 | | 50 | %$V_{DD}$ |
| | ClampHi | 10 bits [1] | 0 | | 100 | %$V_{DD}$ |

| Parameter | Symbol | Remark | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Quiescent (Offset) Voltage Range | $V_{OQ}$ | 14 bits (YA setting) (1) | – 200 | | 200 | $\%V_{DD}$ |
| Sensitivity Range | S | RG[2] = 1 (1)<br>For full-scale output(2) | ±0.04 | | ±0.4 | $\%V_{DD}/G$ |

*Table 7 gives the transfer characteristic specifications*

(1) Please refer to subsequent sections for more detailed information.
(2) The full-scale output corresponds to 100%Vdd output range. This corresponds to 100% of the ADC range when FINEGAIN is set to 1 (1024LSB) in a bipolar application. The DSP chain can additionally increase sensitivity by a factor 4.

## 11. Accuracy Specification

| Parameter | Symbol | Remark | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output DAC Resolution | $LSB_{DAC}$ | 12 bits | | 0.0244 | | $\%V_{DD}$ |
| Output DAC Linearity | $DNL_{DAC}$ | | – 1 | | + 1 | $LSB_{DAC}$ |
| | $INL_{DAC}$ | | – 2 | | + 2 | $LSB_{DAC}$ |
| Ratiometric Error(1) | $OUT_{ratiom}$ | with TEMPTC=0 | – 0.1 | | + 0.1 | $\%V_{DD}$ |
| | | with TEMPTC=128 | – 0.2 | | + 0.2 | $\%V_{DD}$ |
| Output Noise(2) | $OUT_{noise}$ | RG = 4, FG = 800<br>FILTCODE = 4 | | 0.12 | 0.18 | $mV_{RMS}$ |
| | | RG = 7, FG = 800<br>FILTCODE = 4 | | 0.13 | 0.2 | $mV_{RMS}$ |
| | | RG = 4, FG = 4095<br>FILTCODE = 4 | | 0.75 | 1.1 | $mV_{RMS}$ |
| | | RG = 7, FG = 4095<br>FILTCODE = 4 | | 1 | 1.5 | $mV_{RMS}$ |
| Thermal Output Quiescent (Offset) Drift | $\Delta^T V_{OQ}$ | RG = 4 | – 10 | | + 10 | $LSB_{DAC}$ |
| | | RG = 5 | – 10 | | + 10 | $LSB_{DAC}$ |
| | | RG = 6 | – 15 | | + 15 | $LSB_{DAC}$ |

| Parameter | Symbol | Remark | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Sensitivity Drift(3) | $\Delta^T S$ | RG = 7 | – 20 | | + 20 | $LSB_{DAC}$ |
| | | No magnet TC | – 150 | 0 | + 150 | ppm/°C |
| | | Using 1st and 2nd order magnet TC(4) | – 200 | | + 200 | ppm/°C |
| Sensitivity Thermal Hystersis | $\Delta^H S$ | After full thermal excursion | – 0.5 | ± 0.2 | + 0.5 | % |

*Table 8 gives the accuracy specifications*

(1) Ratiometric performance of the IC is measured as a difference in output voltage (expressed as $\%V_{DD}$) between the nominal case with $V_{DD}$ = 5V and the limits of the supply ratiometric operating range (4.5V and 5.5V). The difference between TEMPTC = 0 (or TEMPSENSOR disabled altogether) and TEMPTC = 128 originates in the fact that the on-chip temperature is also a function of the supply voltage. Since the TEMPTC changes the gain of the IC to compensate for the magnet TC, and it relies on the fact that the on-chip temperature is the same as the magnet temperature, an extra error occurs compared to TEMPTC = 0 case.

(2) The noise measurements are performed on the recommended application diagram, with a supply voltage of 5V at room temperature. Increased capacitance values compared to the recommended application diagram, contribute to lower output noise. For peak-to-peak values, the RMS value is typically multiplied by a factor of 6.

(3) The Sensitivity Thermal Drift is within these boundaries for all ICs with the default setting for gain compensation i.e. fixed to 1, which is obtained by setting TEMPTC to 0, but leaving the TEMPSENSOR bit set (see Subsequent Section). If the value is not fixed to 1, the sensitivity of the IC will exhibit a sensitivity thermal drift curve such as the one shown in the section on magnet compensation (if SECONDORDERTC is set) or with a linear temperature coefficient (if SECONDORDERTC is cleared) depending on the setting of TEMPTC, but ±150ppm/°C.

(4) This limit is an indication of what can be achieved for a typical magnet. The main assumption is that the magnet strength monotonically decreases over temperature. Then, the 2nd order implementation as described in subsequent sections has been designed to work up to ferrite magnets with a magnet TC of -2000ppm/°C. Please contact Melexis when in doubt over the achievable specification for your magnet.

## 12. Diagnostic Specification

| Parameter | Symbol | Remark | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ADC Clipping Signaling(1) | $DIAG_{CLIP}$ | DIAGINFAULT = 0 | - | - | $V_{SATLO}$ | $\%V_{DD}$ |
| | | DIAGINFAULT = 1 | $V_{SATHI}$ | - | - | $\%V_{DD}$ |
| ADC Clipping Criterion(1) | $N_{CLIP}$ | ADC clipping count before Diagnostic is set | - | 4 | - | Count |
| CRC Fail Signaling | $DIAG_{PAR}$ | DIAGINFAULT = 0 | - | - | $V_{SATLO}$ | $\%V_{DD}$ |
| | | DIAGINFAULT = 1 | $V_{SATHI}$ | - | - | $\%V_{DD}$ |
| CRC Fail Criterion | $N_{CRC}$ | CRC Fail count before | - | 3 | - | Count |

| Parameter | Symbol | Remark | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | Diagnostic is set | | | | |
| Broken $V_{SS}$ (2) | $V_{OUTbrVSS}$ | Over $R_{PD}$ range | - | - | $V_{DIAGLO}$ | $\%V_{DD}$ |
| Broken $V_{DD}$ (2) | $V_{OUTbrVDD}$ | Over $R_{PD}$ range | - | - | $V_{DIAGLO}$ | $\%V_{DD}$ |

*Table 9 gives the diagnostic level specifications*

(1) ADC clipping is only flagged if the FAULTONCLIP bit in EEPROM is set. If the bit is cleared, the ADC will clamp at either the maximum code or the minimum code, depending on the clipping condition. Reporting after 4 sequential clipping conditions is required for an EMC robust design. Clipping reporting does not apply to ADC values of the temperature signal.

(2) Diagnostics that are the result of a passive settling because the output stage becomes high impedant (such as broken wire) are governed by the RC time constant of the capacitive load on the output and the $R_{PD}$ resistor at ECU side. The OBD detection time is negligible in comparison to the settling time in case of a broken wire. The settling time should be taken as 4 times the RC time constant. E.g. with a load of 330nF and 330kOhm, the RC time constant equals 109ms. Settling time then corresponds to 4 RC time constants, i.e. 436ms.

## 13. Startup, Undervoltage, Overvoltage and Reset Specification

During power-up (supply rising from 0V upwards) the MLX90288 remains in a zone where the output is undefined (grey triangular area in the plot) because there is no active circuitry putting the output stage in a specific condition. Most likely the output remains close to the low rail because of the passive external pull-down, but it cannot be predicted what happens exactly inside the IC at this point. This is also depicted in the signal waveforms of this section.

The POR phase is the phase where the supply is still below VPORRISE, but above the undefined region. In this case the digital is in a reset state, which puts all flip-flops in a known state, and the output is high impedant. Due to the external pull-down resistive load, the output is at the low rail.

When the supply rises above the VPORRISE threshold (which has built-in hysteresis: for the falling edge, VPORFALL), an initialization occurs which includes loading all EEPROM settings into RAM. After this initialization phase, the chip will start its FSM program and provide a valid output signal, for as long as the supply voltage is above the VUNDERRISE threshold (which has built-in hysteresis: for the falling edge, VUNDERFALL). If the supply is below this threshold, the output remains in high impedant state, corresponding to an output voltage at the low rail.

Whenever the MLX90288 goes from normal operation to undervoltage or via undervoltage to reset state, and vice versa, the output has a settling time which is a function of both the output load and the driving capability. On top of this, there is a startup time ($t_{STARTUP}$) in case the chip comes out of reset.

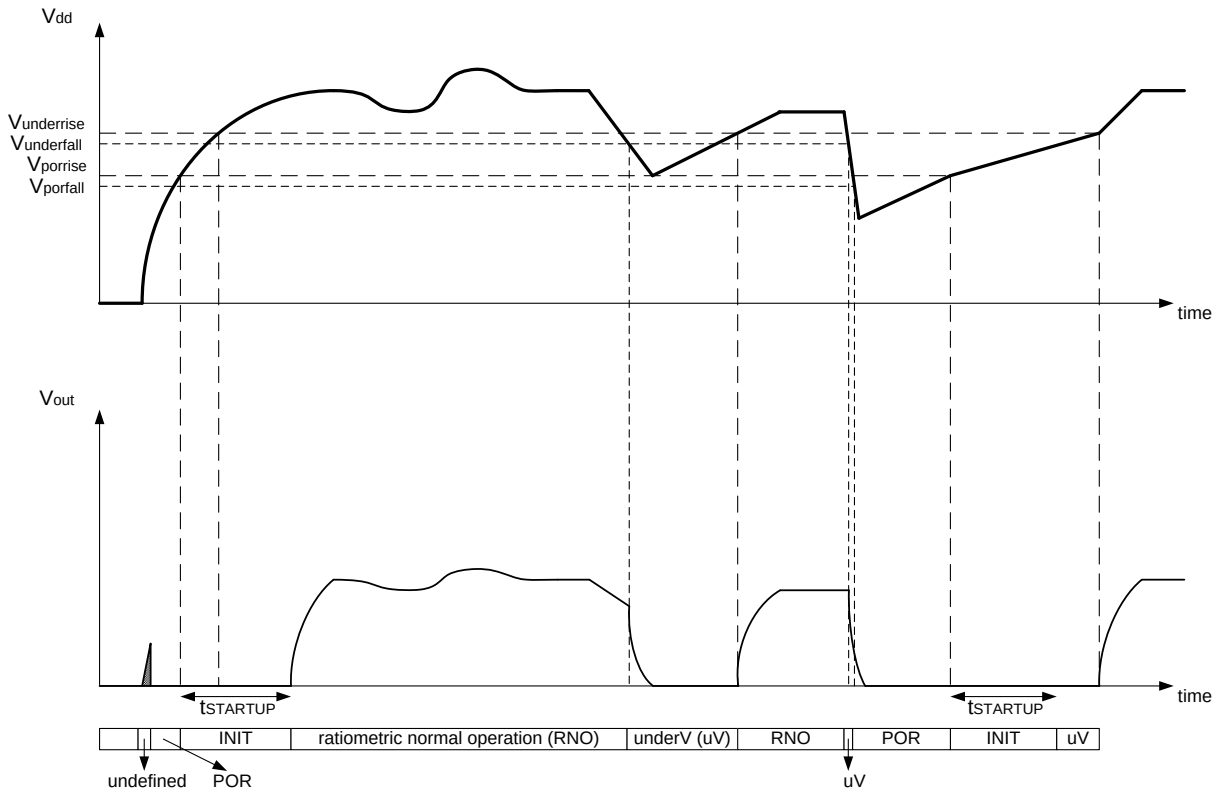



*Figure 2 Operating, undervoltage and reset functionality*

In case the supply is raised above the VPROGRISE threshold (which has built-in hysteresis: for the falling edge, VPROGFALL), but below the VOVER threshold, the IC goes in programming mode: the output becomes high impedant and after proper commands coming from the programming unit (PTC04), the IC can respond on the output pin as well. The communication protocol on the output (PTC-04 communication) is bi-directional. If the supply is higher than the VOVER threshold, the internal regulated supply is disconnected from the external supply, as are most blocks of the IC. A reset will be the result when the supply is restored.

## 14. EMC/ESD Specification

| Parameter | Symbol | Remark | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Micro-interrupt without reset(1) | µI | | - | - | 0.1 | µs |
| ESD Human Body Model(2) | $ESD_{HBM}$ | | | ± 2 | | kV |
| ESD Charged Device Model(3) | $ESD_{CDM}$ | | | ± 500 | | V |

(1) If the digital regulated voltage drops below POR level, the ASIC will reset nearly immediately; this is a necessity from a DFMEA point of view. The only way to make the ASIC immune for longer micro-interrupts is to have external components (Rseries and Csupply) filtering these micro-interrupts for the ASIC. Introducing an Rseries in the supply line will have a negative impact on ratiometricity.

(2) ESD HBM test performed on all pins according to JEDEC-22-A-114 standard.

(3) ESD CDM test performed on all pins according to AEC-Q100-011 standard.

# 15. EEPROM Mapping

## 15.1. EEPROM Description

All calibration parameters on the MLX90288 are stored in a 32 x 16bit non-volatile EEPROM.

The EEPROM parameters from the first 29 addresses are stored with triple redundancy, to correct if any EEPROM bit would loose its content, by using majority voting. Consequently, an EEPROM word in this part of EEPROM only holds the information of 5 calibration bits + 1 locking bit at index 15. The EEPROM word stored at address 0 thus looks like this:

**{LOCK0,PARAM[4:0],PARAM[4:0],PARAM[4:0]}**

If bit index 15 is set, the EEPROM word is permanently locked, making it impossible to overwrite the given address in PTC mode.

ID bits from the last 3 addresses are not stored with redundancy. The MLXID is not programmable in PTC mode, hence guaranteeing traceability of the parts.

There are no constraints on the EEPROM readout in PTC mode.

## 15.2. Melexis Programmable Parameters

### 15.2.1. OSCTRIM [4:0]

- Will be calibrated at MLX production
- Trims oscillator frequency around 1 MHz

### 15.2.2. TRIMCTAT [4:0]

- Will be calibrated at MLX production
- Trims PTAT and CTAT to have both current sources at the same level at 25°C
- This calibration is necessary to allow correct TC1 trimming with a single measurement at either hot or cold
- The calibration compensates mismatch in both PTAT and CTAT current sources

### 15.2.3. ITRIM[2:0]

- Will be calibrated at MLX production
- Trims the current reference used throughout the analog part to a predefined value

### 15.2.4. IPLATE[3:0]

- Will be calibrated at MLX production
- Defines the current through the Hall plates, impacting the total gain

### 15.2.5. TC1ST[6:0]

- Will be calibrated at MLX production
- Programming first order sensitivity temperature drift compensation
- Piecewise linear compensation between hot and cold temperatures = TC1ST

### 15.2.6. TC2ND[5:0]

- Will be calibrated at MLX production
- Programming piecewise linear sensitivity temperature drift compensation
- It is like an additional TC1 starting at 25 °C +/-30 °C
- Piecewise linear compensation for hot temperatures = TC1ST + TC2ND

### 15.2.7. TC3RD[2:0]

- Will be calibrated at MLX production
- Programming piecewise linear sensitivity temperature drift compensation
- It is like an additional TC1 starting at - 5 °C
- Piecewise linear compensation for cold temperatures = TC1ST + TC2ND + 2*TC3RD

### 15.2.8. PLATEPOL

- Will be calibrated at MLX production
- Changes the polarity of the Hall plates, inverting the sensing nodes
- Changing the plate polarity will make the MLX production calibration void
- Changing the polarity of the output signal is recommended to be achieved by changing the FINEGAIN MSB

### 15.2.9. OFFCST[4:0]

- Will be calibrated at MLX production
- Residual offset calibration (at Integrator stage) to make sure that the ADC input is at half of the ADC span when no field is applied
- Analog compensation, sign magnitude number

### 15.2.10. OFFDRIFT[5:0]

- Will be calibrated at MLX production
- Compensates linearly for residual offset temperature drift at the Integrator stage
- Analog compensation, sign magnitude number

### 15.2.11. ROUGHGAIN[2]

- Set by default to 1 by Melexis

### 15.2.12. XA[13:0]

- Will be calibrated at MLX production
- Gain-dependent offset, should not be modified after calibration
- Removes the residual offset of the ADC output when no field is applied

### 15.2.13. MLXID[31:0]

- Melexis ID bits for traceability
- Can not be overwritten in PTC mode

### 15.2.14. CRC[9:0]

- Standard CRC10 for data integrity
- Polynomial is $x^{10}+x^{9}+x^{5}+x^{4}+x^{1}+1$
- EEPROM data is fed LSB first, per address (5bits, after majority voting) sequentially

The CRC integrity will be preserved by the PSF software when using the PTC04. It could not be changed manually

## 15.3. Melexis Programmable Parameters

### 15.3.1. FAULTONCLIP

- Enable error reporting if ADC is clipping for 4 or more successive times
- The diagnostic side for this error is defined by DIAGINFAULT

### 15.3.2. DIAGINFAULT

- Defines to which side the output will go in case of an active error such as CRC fail or ADC clipping, the latter only in case FAULTONCLIP is set
- The thresholds are specified under the section on diagnostics.

### 15.3.3. FILTCODE[3:0]

- The digital IIR filter offers noise reduction and low pass filtering with programmable cut off frequency

| FILTCODE[3:0] | Cut-off frequency [Hz] |
|---|---|
| 0 | 1114 |
| 1 | 557 |
| 2 | 279 |
| 3 | 139 |
| 4 | 70 |
| 5 | 35 |
| 6 | 17 |
| 7 | 9 |
| 8 | 4 |

*Table 10: Filter cut-off frequencies*

- For Filter code from 9 to 15, the rounding error becomes too high versus the resolution so those codes are not to be used.

- This table only applies in case the temperature sensor is enabled, otherwise the cut-off frequency should be multiplied by a factor of 2 since no more temperature ADC's are performed anymore.

### 15.3.4. TEMPSENSOR

- Enables digital gain compensation over temperature (GainMag)
- Requires proper calibration of TEMPOFF and TEMPTC, as well as the SECONDORDERTC

### 15.3.5. SECONDORDERTC

- Chooses between linear gain compensation over temperature (cleared) and ROM based 2$^{nd}$ order compensation (set) as described under the section on magnet compensation

### 15.3.6. TEMPOFF[9:0]

- Will be calibrated at MLX production
- Defines the offset of the GainMag temperature compensation as described under Section **Error! Reference source ot found.**

### 15.3.7. TEMPTC[7:0]

- Will be calibrated at MLX production
- Defines the slope of the GainMag temperature compensation as described under Section **Error! Reference source ot found.**

### 15.3.8. CLPLow[8:0]

- Low clamp level programmability range from 0% to 50% of VDD
- Resolution is 1/4$^{th}$ of the outDAC resolution, i.e. 0.098% of VDD

### 15.3.9. CLPHigh[9:0]

- High clamp level programmability range from 0% to 100% of VDD
- Resolution is 1/4$^{th}$ of the outDAC resolution, i.e. 0.098% of VDD

### 15.3.10. ROUGHGAIN[1:0]

- These 2 bits control the gain of the MAIN AMPLIFIER

### 15.3.11. ATTN2P5

- Enables the attenuation in the analog chain by a factor of 4.5

### 15.3.12. FINEGAIN[12:0]

- Sign-magnitude 13bit digital fine gain (not 2's complement!)
- The code 1024 (400h) corresponds to a gain of 1
- The code 5120 (1400h) corresponds to a gain of -1
- The MSB is a sign bit
- FINEGAIN range is therefore from -4095 (1FFFh) to +4095 (FFFh), which corresponds to a gain range of -3.999 to +3.999

### 15.3.13. YA[13:0]

- Output offset programming, not gain dependent
- Defines the offset on the output in case no field is applied, inside a range of -200%Vdd to +200% Vdd with the 12-bit resolution of the output DAC, i.e. 0.0244% of VDD

### 15.3.14. CSTID[15:0]

- Customer ID bits for traceability

# 16. Thermal Sensitivity Drift Compensation

## 16.1. Introduction

The embedded temperature sensor is digitized via the main path ADC before each analog amplified Hall sensor voltage ADC in case TEMPSENSOR is enabled. This temperature information is used to generate either an address for a ROM Look-up Table in order to obtain a quadratic temperature compensation (SECONDORDERTC=1), or a value proportional to the temperature that allows a linear IC gain compensation (SECONDORDERTC=0). Both compensations rely on the TEMPOFF and TEMPTC parameters.

## 16.2. Linear Compensation (1st Order)

The conventional linear temperature compensation proves to be adequate for small application temperature ranges and/or small magnet temperature coefficients. In such cases the error induced by the linear approach are limited and prove to be good enough for the desired system sensitivity drift.

## 8.3 Quadratic Compensation (2nd Order)

This look up table is stored in ROM and contains the inverse transfer function of a specific magnetic flux density over temperature. It should be used for magnets with temperature coefficients lower than -1500 ppm/degC, as is typically the case for plastic bonded magnets. Such magnet temperature coefficients cannot optimally be compensated by the linear method. However, Melexis tooling together with the stored compensation characteristic enable improved thermal drift compensation.

The correction factor GainMag is multiplied with the measured magnetic flux density. This multiplication results in a (nearly) temperature independent sensitivity of the whole system (magnet + IC).

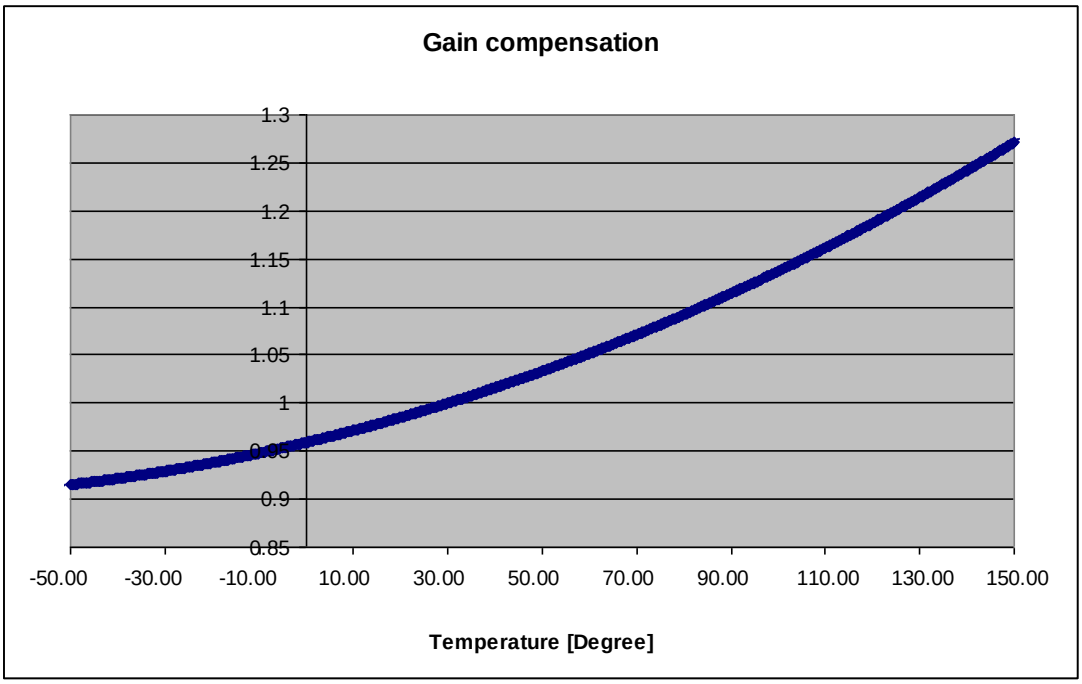



*Figure 3: ROM table - 2nd order gain compensation (for illustrative purposes only)*

The factory calibration performed by Melexis targets a specific magnet TC, which serves as accurate basis for any delta calibration that should be performed when using a magnet with a different TC. This is performed

via the solver software provided by Melexis. The solver enables customers to address different sections in the lookup table for different temperature ranges. This flexibility is to ensure a good match between magnet TC and applied compensation.

## 17. Standard Information

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to standards in place in Semiconductor industry.

For further details about test method references and for compliance verification of selected soldering method for product integration, Melexis recommends reviewing on our web site the General Guidelines soldering recommendation. For all soldering technologies deviating from the one mentioned in above document (regarding peak temperature, temperature gradient, temperature profile etc), additional classification and qualification tests have to be agreed upon with Melexis.

For package technology embedding trim and form post-delivery capability, Melexis recommends to consult the dedicated trim&form recommendation application note: lead trimming and forming recommendations

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/en/quality-environment

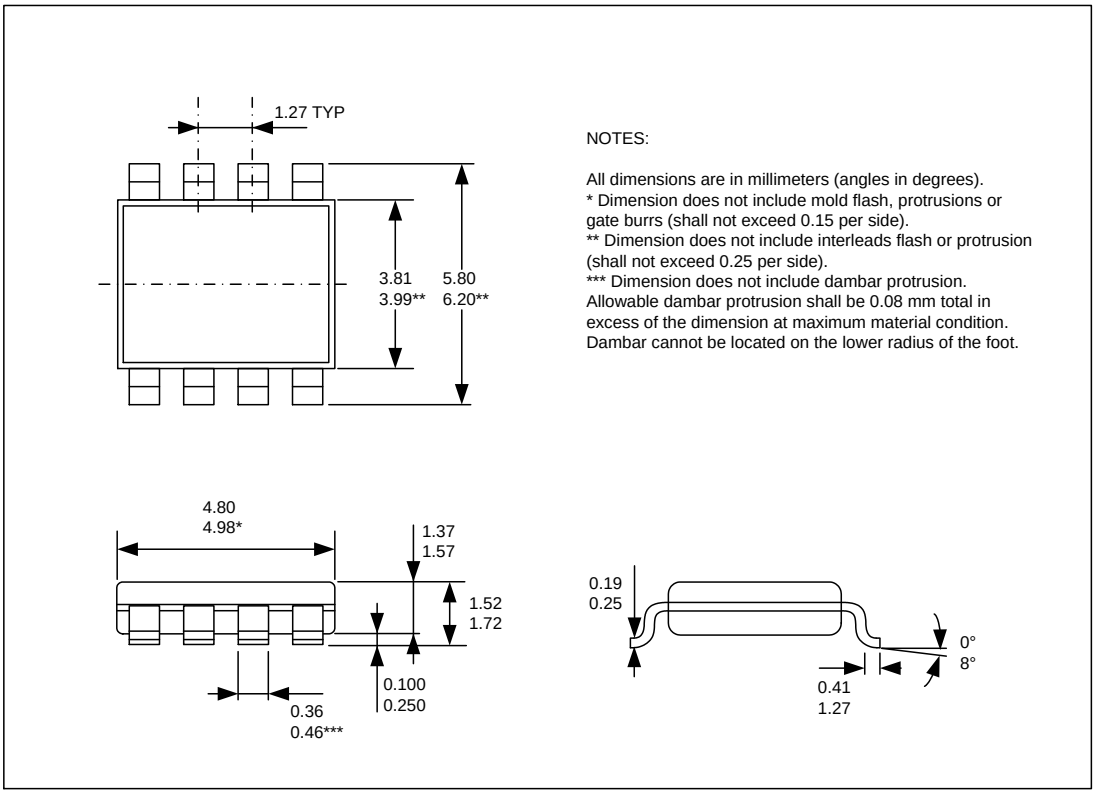
## 18. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

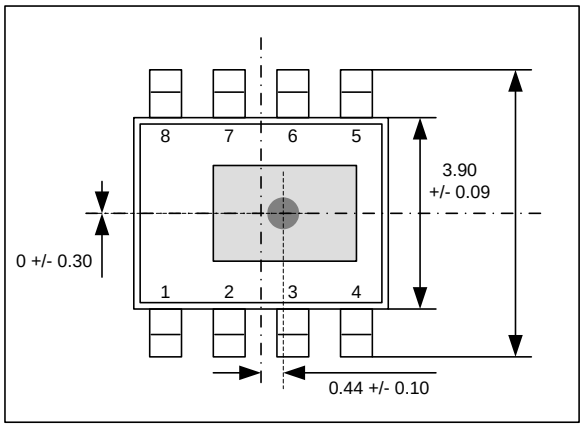
# 19. Package Specification

## 19.1. Package Dimensions

- Package Type: SOIC-8 (8-pin Small Outline Integrated Circuit Package)
- Die placement accuracy is ± 2 mils = ± 50 microns.




Dimensions




Hall Plate location

*Figure 4: Package Dimensions*

## 19.2. Package Marking

The package is labelled for traceability purposes, as depicted in this section's figure.

The first line is reserved for the project number at Melexis, 90288 followed by the ASIC silicon version. The line below refers to the wafer fab. The bottom line is the date code indicating when the bare dies were packaged at the assembly house. The black dot indicates the position of pin #1.

- MXXXXX = 5-digit lot number (M = wafer fab)
- YYWW = last 2 digits of the year, followed by the calendar week

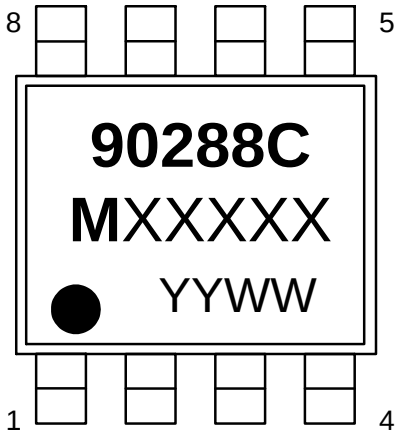



*Figure 5: Package markings*

### 19.3. Recommended Application Diagram

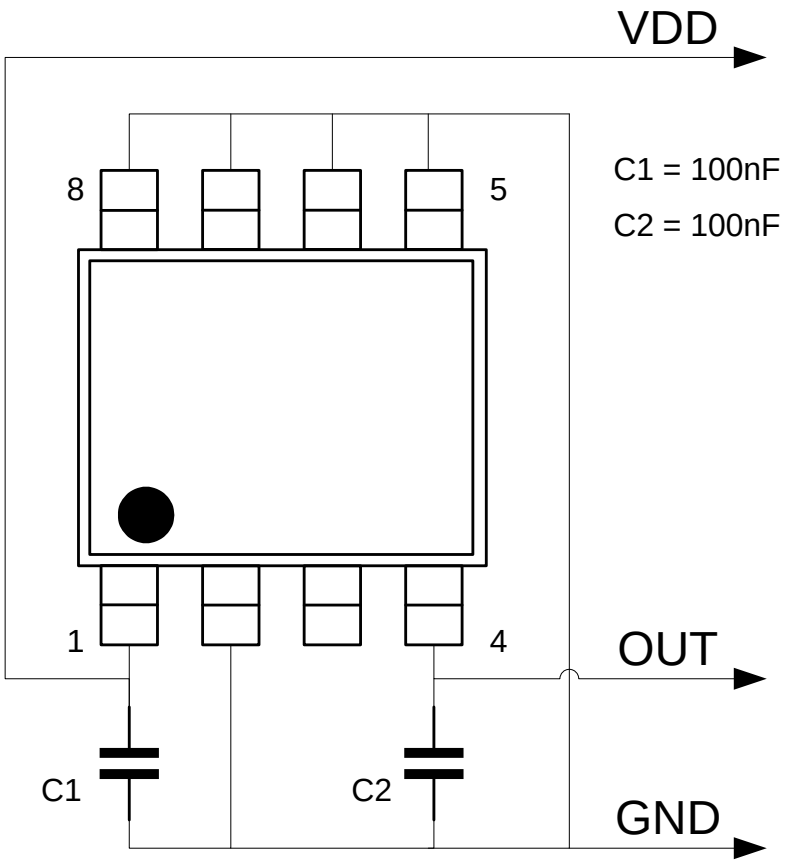



*Figure 6: Recommended Application Diagram*

The testpins (#5, #6, #7, #8) need to be grounded to avoid the risk of the chip going into testmode because of RF/noise entering the test controller on these pins. The test input pins have an internal pull-down resistor.

The recommended application diagram is not a mandatory design guide. For better ESD and EMC performance external components can be modified for as long as the electrical specifications are followed under previous sections. For good EMC performance the components should be placed as close as possible to the IC.

## 20. Revision History Table

| | |
|---|---|
| 21/07/2017 | Conversion of 90288CA datasheet to new template of datasheet |

*Table 11*

## 21. Contact

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For additional information, please contact our Direct Sales team and get help for your specific needs:

| | |
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