TPS4333x-Q1 Low-I$_Q$, Single-Boost, Dual Synchronous-Buck Controller

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C2
- Two Synchronous Buck Controllers
- One Pre-Boost Controller
- Input Range up to 40 V, (Transients up to 60 V), Operation Down to 2 V When Boost is Enabled
- Low-Power-Mode I$_Q$: 30 µA (One Buck On), 35 µA (Two Bucks On)
- Low Shutdown Current I$_{sh}$ < 4 µA
- Buck Output Range 0.9 V to 11 V
- Boost Output Selectable: 7 V, 10 V, or 11 V
- Programmable Frequency and External Synchronization Range 150 kHz to 600 kHz
- Separate Enable Inputs (ENA, ENB)
- Frequency Spread Spectrum (TPS43336-Q1)
- Selectable Forced Continuous Mode or Automatic Low-Power Mode at Light Loads
- Sense Resistor or Inductor DCR Sensing
- Out-of-Phase Switching Between Buck Channels
- Peak Gate-Drive Current 0.7 A
- Thermally Enhanced 38-Pin HTSSOP (DAP) PowerPAD™ Package

2 Applications

- Automotive Start-Stop, Infotainment, Navigation Instrument Cluster Systems
- Industrial and Automotive Multi-Rail DC Power Distribution Systems and Electronic Control Units

3 Description

The TPS43335-Q1 and TPS43336-Q1 include two current-mode synchronous buck controllers and a voltage-mode boost controller. The devices are ideally suited as a pre-regulator stage with low Iq requirements and for applications that must survive supply drops due to cranking events. The integrated boost controller allows the devices to operate down to 2 V at the input without seeing a drop on the buck regulator output stages. At light loads, one can enable the buck controllers to operate automatically in low-power mode, consuming just 30 µA of quiescent current.

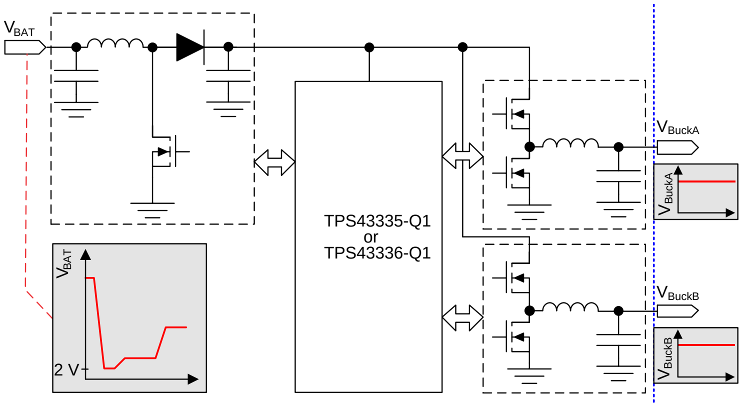
The buck controllers have independent soft-start capability and power-good indicators. Current foldback in the buck controllers and cycle-by-cycle current limitation in the boost controller provide external MOSFET protection. One can program the switching frequency over 150 kHz to 600 kHz or synchronize it to an external clock in the same range. Additionally, the TPS43336-Q1 offers frequency-hopping spread-spectrum operation.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS43335-Q1	HTSSOP (38)	6.20 mm × 12.50 mm
TPS43336-Q1		

[1] For all available packages, see the orderable addendum at the end of the data sheet.

Figure 1. Typical Application Diagram



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4 Revision History

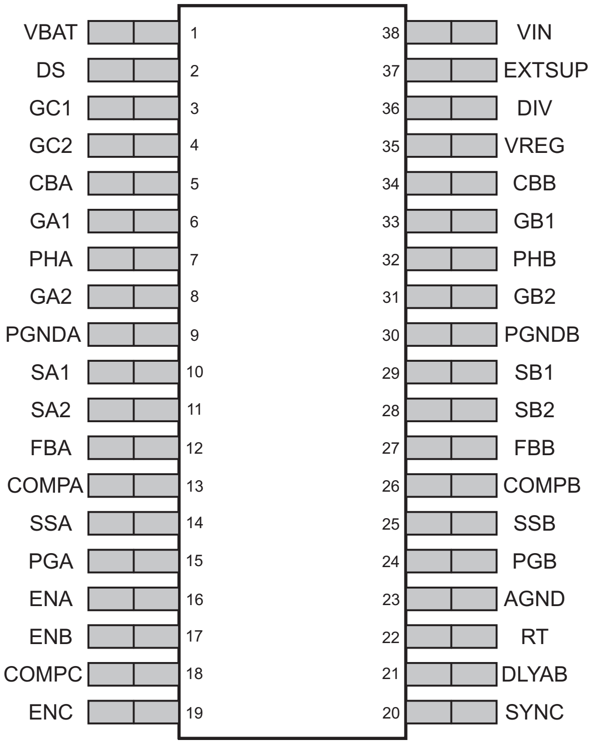
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2013) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

Changes from Revision C (June 2011) to Revision D	Page
• Corrected pinout drawing	3
• Changed descriptions for pins DIV, ENA, and ENB	3
• Revised Absolute Maximum Ratings table	6
• Changed specification names for HBM and CDM classification ratings	6
• Replaced curve in Load Step Response (Boost) graph	12
• Revised functional block diagram	16
• Revised last paragraph of Light-Load PFM Mode section	20
• Corrected R1 + R2... equation in Resistor Divider Selection... section	35

5 Pin Configuration and Functions

DAP Package
38-Pin HTSSOP With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	23	O	Analog ground reference
CBA	5	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck controller BuckA. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge.
CBB	34	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck controller BuckB. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge.
COMPA	13	O	Error amplifier output of BuckA and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the inductor of BuckA. Clamping his voltage on the upper and lower ends provides current-limit protection for the external MOSFETs.
COMPB	26	O	Error amplifier output of BuckB and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the inductor of BuckB. Clamping his voltage on the upper and lower ends provides current-limit protection for the external MOSFETs.
COMPC	18	O	Error-amplifier output and loop-compensation node of the boost regulator
DIV	36	I	The status of this pin defines the output voltage of the boost regulator. A high input regulates the boost converter at 11 V, a low input sets the value at 7 V, and a floating pin sets 10 V. NOTE: DIV = high and ENC = high inhibits low-power mode on the bucks.
DLYAB	21	O	The capacitor at the DLYAB pin sets the power-good delay interval used to de-glitch the outputs of the power-good comparators. Leaving this pin open sets the power-good delay to an internal default value of 20 µs typical.
DS	2	I	This input monitors the voltage on the external boost-converter low-side MOSFET for overcurrent protection. An alternative connection for better noise immunity is to place a sense resistor between the source of the low-side MOSFET and ground via a filter network.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	**NO.**		
ENA	16	I	Enable input for BuckA (active-high with an internal pullup current source). An input voltage higher than 1.7 V enables the controller, whereas an input voltage lower than 1.7 V disables the controller. When both ENA and ENB are low, the device shuts down and consumes less than 4 µA of current. NOTE: DIV = high and ENC = high inhibits low-power mode on the bucks.
ENB	17	I	Enable input for BuckB (active-high with an internal pullup current source). An input voltage higher than 1.7 V enables the controller, whereas an input voltage lower than 1.7 V disables the controller. When both ENA and ENB are low, the device shuts down and consumes less than 4 µA of current. NOTE: DIV = high and ENC = high inhibits low-power mode on the bucks.
ENC	19	I	This input enables and disables the boost regulator. An input voltage higher than 1.7 V enables the controller. Voltages lower than 0.7 V disable the controller. Because this pin provides an internal pulldown resistor (500 kΩ), enabling the boost function requires pulling it high. When enabled, the controller starts switching as soon as V_{BAT} falls below the boost threshold, depending on the programmed output voltage.
EXTSUP	37	I	One can use EXTSUP to supply the VREG regulator from one of the TPS43335-Q1 or TPS43336-Q1 buck regulator rails to reduce power dissipation in cases where there is an expectation of high VIN. If EXTSUP is unused, leave the pin open without a capacitor installed.
FBA	12	I	Feedback voltage pin for BuckA. The buck controller regulates the feedback voltage to the internal reference of 0.8 V. A suitable resistor divider network between the buck output and the feedback pin sets the desired output voltage.
FBB	27	I	Feedback voltage pin for BuckB. The buck controller regulates the feedback voltage to the internal reference of 0.8 V. A suitable resistor-divider network between the buck output and the feedback pin sets the desired output voltage.
GA1	6	O	This output can drive the external high-side N-channel MOSFET for buck regulator BuckA. The output provides high peak currents to drive capacitive loads. The gate drive reference is to a floating ground provided by PHA that has a voltage swing provided by CBA.
GA2	8	O	This output can drive the external low-side N-channel MOSFET for buck regulator BuckA. The output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin.
GB1	33	O	This output can drive the external high-side N-channel MOSFET for buck regulator BuckB. The output provides high peak currents to drive capacitive loads. The gate drive reference is to a floating ground provided by PHB that has a voltage swing provided by CBB.
GB2	31	O	This output can drive the external low-side N-channel MOSFET for buck regulator BuckB. The output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin.
GC1	3	O	This output can drive an external low-side N-channel MOSFET for the boost regulator. This output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin.
GC2	4	O	This pin makes a floating output drive available to control the external P-channel MOSFET. This MOSFET can bypass the boost rectifier diode or a reverse-protection diode when the boost is not switching or if boost is disabled, and thus reduce power losses.
PGA	15	O	Open-drain power-good indicator pin for BuckA. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls below 93% of the set value, or if either V_{IN} or V_{BAT} drops below its respective undervoltage threshold.
PGB	24	O	Open-drain power-good indicator pin for BuckB. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls below 93% of the set value, or if either V_{IN} or V_{BAT} drops below its respective undervoltage threshold.
PGNDA	9	O	Power ground connection to the source of the low-side N-channel MOSFET of BuckA
PGNDB	30	O	Power ground connection to the source of the low-side N-channel MOSFET of BuckB
PHA	7	O	Switching terminal of buck regulator BuckA, providing a floating ground reference for the high-side MOSFET gate-driver circuitry and used to sense current reversal in the inductor when discontinuous-mode operation is desired.
PHB	32	O	Switching terminal of buck regulator BuckB, providing a floating ground reference for the high-side MOSFET gate-driver circuitry and used to sense current reversal in the inductor when discontinuous-mode operation is desired.
RT	22	O	Connecting a resistor to ground on this pin sets the operational switching frequency of the buck and boost controllers. A short circuit to ground on this pin defaults operation to 400 kHz for the buck controllers and 200 kHz for the boost controller.
SA1	10	I	High-impedance differential-voltage inputs from the current-sense element (sense resistor or inductor DCR) for each buck controller. Choose the current-sense element to set the maximum current through the inductor based on the current-limit threshold (subject to tolerances) and considering the typical characteristics across duty cycle and V_{IN}. (SA1 positive node, SA2 negative node).
SA2	11	I	

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SB1	29	I	High-impedance differential voltage inputs from the current-sense element (sense resistor or inductor DCR) for each buck controller. Choose the current-sense element to set the maximum current through the inductor based on the current-limit threshold (subject to tolerances) and considering the typical characteristics across duty cycle and V_{IN}. (SB1 positive node, SB2 negative node).
SB2	28	I	
SSA	14	O	Soft-start or tracking input for buck controller BuckA. The buck controller regulates the FBA voltage to the lower of 0.8 V or the SSA pin voltage. An internal pullup current source of 1 µA is present at the pin, and an appropriate capacitor connected here sets the soft-start ramp interval. Alternatively, a resistor divider connected to another supply can provide a tracking input to this pin.
SSB	25	O	Soft-start or tracking input for buck controller BuckB. The buck controller regulates the FBB voltage to the lower of 0.8 V or the SSB pin voltage. An internal pullup current source of 1 µA is present at the pin, and an appropriate capacitor connected here sets the soft-start ramp interval. Alternatively, a resistor divider connected to another supply can provide a tracking input to this pin.
SYNC	20	I	If an external clock is present on this pin, the device detects it and the internal PLL locks onto the external clock, thus overriding the internal oscillator frequency. The device can synchronize to frequencies from 150 kHz to 600 kHz. A high logic level on this pin ensures forced continuous-mode operation of the buck controllers and inhibits transition to low-power mode. An open or low allows discontinuous-mode operation and entry into low-power mode at light loads. On the TPS43336-Q1, a high level enables frequency-hopping spread spectrum, whereas an open or a low level disables it.
VBAT	1	I	Battery input sense for the boost controller. If, with the boost controller enabled, the voltage at VBAT falls below the boost threshold, the device activates the boost controller and regulates the voltage at VIN to the programmed boost output voltage.
VIN	38	I	Main input pin. This is the buck controller input pin as well as the output of the boost regulator. Additionally, VIN powers the internal control circuits of the device.
VREG	35	O	The device requires an external capacitor on this pin to provide a regulated supply for the gate drivers of the buck and boost controllers. TI recommends capacitance on the order of 4.7 µF. The regulator obtains its power from either VIN or EXTSUP. This pin has current-limit protection; do not use it to drive any other loads.

6 Specifications

6.1 Absolute Maximum Ratings

See [1]

		MIN	MAX	UNIT
Voltage	Input voltage: VIN, VBAT	–0.3	60	V
Voltage (buck function: BuckA and BuckB)	Ground: PGNDA–AGND, PGNDB–AGND	–0.3	0.3	V
	Enable inputs: ENA, ENB	–0.3	60	
	Bootstrap inputs: CBA, CBB	–0.3	68	
	Bootstrap inputs: CBA–PHA, CBB–PHB	–0.3	8.8	
	Phase inputs: PHA, PHB	–0.7	60	
	Phase inputs: PHA, PHB (for 150 ns)	–1	60	
	Feedback inputs: FBA, FBB	–0.3	13	
	Error amplifier outputs: COMPA, COMPB	–0.3	13	
	High-side MOSFET driver: GA1–PHA, GB1–PHB	–0.3	8.8	
	Low-side MOSFET drivers: GA2–PGNDA, GB2–PGNDB	–0.3	8.8	
	Current-sense voltage: SA1, SA2, SB1, SB2	–0.3	13	
	Soft start: SSA, SSB	–0.3	13	
	Power-good output: PGA, PGB	–0.3	13	
	Power-good delay: DLYAB	–0.3	13	
	Switching-frequency timing resistor: RT	–0.3	13	
	SYNC, EXTSUP	–0.3	13	
Voltage (boost function)	Low-side MOSFET driver: GC1–PGNDA	–0.3	8.8	V
	Error-amplifier output: COMPC	–0.3	13	
	Enable input: ENC	–0.3	13	
	Current-limit sense: DS	–0.3	60	
	Output-voltage select: DIV	–0.3	8.8	
Voltage (PMOS driver)	P-channel MOSFET driver: GC2	–0.3	60	V
	P-channel MOSFET driver: VIN–GC2	–0.3	8.8	
Voltage	Gate-driver supply: VREG	–0.3	8.8	V
Temperature	Junction temperature, T_J	–40	150	°C
	Operating temperature, T_A	–40	125	
	Storage temperature, T_{stg}	–55	165	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 [1]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	FBA, FBB, RT, DLYAB	±400	
			VBAT, ENC, SYNC, VIN	±750	
			All other pins	±500	
		Machine model (MM)	PGA, PGB	±150	
			All other pins	±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Buck function: BuckA and BuckB voltage	Input voltage: VIN, VBAT	4	40	V
	Enable inputs: ENA, ENB	0	40	
	Boot inputs: CBA, CBB	4	48	
	Phase inputs: PHA, PHB	–0.6	40	
	Current-sense voltage: SA1, SA2, SB1, SB2	0	11	
	Power-good output: PGA, PGB	0	11	
	SYNC, EXTSUP	0	9	
Boost function	Enable input: ENC	0	9	V
	Voltage sense: DS		40	
	DIV	0	V_{REG}	
Operating temperature, T_A		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS4333x-Q1	UNIT
		DAP (HTSSOP)	
		38 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.24	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics

V_{IN} = 8 V to 18 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{BAT}	Supply voltage	Boost controller enabled, after satisfying initial start-up condition	2		40	V
V_{IN}	Input voltage required for device on initial start-up		6.5		40	V
	Buck regulator operating range after initial start-up		4		40	
$V_{IN(UV)}$	Buck undervoltage lockout	V_{IN} falling. After a reset, initial start-up conditions may apply.(1)	3.5	3.6	3.8	V
		V_{IN} rising. After a reset, initial start-up conditions may apply.(1)		3.8	4	V
V_{BOOST_UNLOCK}	Boost unlock threshold	V_{BAT} rising	8.2	8.5	8.8	V
$I_{q\_LPM\_}$	LPM quiescent current: (2)	V_{IN} = 13 V, BuckA: LPM, BuckB: off, T_A = 25°C		30	40	µA
		V_{IN} = 13 V, BuckB: LPM, BuckA: off, T_A = 25°C		30	40	
		V_{IN} = 13 V, BuckA, B: LPM, T_A = 25°C		35	45	µA
I_{q_LPM}	LPM quiescent current: (2)	V_{IN} = 13 V, BuckA: LPM, BuckB: off, T_A = 125°C		40	50	µA
		V_{IN} = 13 V, BuckB: LPM, BuckA: off, T_A = 125°C		40	50	
		V_{IN} = 13 V, BuckA, B: LPM, T_A = 125°C		45	55	µA
I_{q_NRM}	Quiescent current: normal (PWM) mode(2)	SYNC = HIGH, T_A = 25°C		4.85	5.3	mA
		V_{IN} = 13 V, BuckA: CCM, BuckB: off, T_A = 25°C		4.85	5.3	
		V_{IN} = 13 V, BuckB: CCM, BuckA: off, T_A = 25°C		4.85	5.3	
		V_{IN} = 13 V, BuckA, B: CCM, T_A = 25°C		7	7.6	
I_{q_NRM}	Quiescent current: normal (PWM) mode(2)	SYNC = HIGH, T_A = 125°C		5	5.5	mA
		V_{IN} = 13 V, BuckA: CCM, BuckB: off, T_A = 125°C		5	5.5	
		V_{IN} = 13 V, BuckB: CCM, BuckA: off, T_A = 125°C		5	5.5	
		V_{IN} = 13 V, BuckA, B: CCM, T_A = 125°C		7.5	8	
I_{bat_sh}	Shutdown current	BuckA, B: off, V_{BAT} = 13 V , T_A = 25°C		2.5	4	µA
I_{bat_sh}	Shutdown current	BuckA, B: off, V_{BAT} = 13 V, T_A = 125°C		3	5	µA
INPUT VOLTAGE V_{BAT} - UNDERVOLTAGE LOCKOUT						
$V_{BAT(UV)}$	Boost-input undervoltage	V_{BAT} falling. After a reset, initial start-up conditions may apply.(1)	1.8	1.9	2	V
		V_{BAT} rising. After a reset, initial start-up conditions may apply.(1)	2.4	2.5	2.6	V
$UVLO_{Hys}$	Hysteresis		500	600	700	mV
$UVLO_{filter}$	Filter time			5		µs
INPUT VOLTAGE V_{IN} - OVERVOLTAGE LOCKOUT						
V_{OVLO}	Overvoltage shutdown	V_{IN} rising	45	46	47	V
		V_{IN} falling	43	44	45	
$OVLO_{Hys}$	Hysteresis		1	2	3	V
$OVLO_{filter}$	Filter time			5		µs

(1) If V_{BAT} and V_{REG} remain adequate, the buck can continue to operate if V_{IN} is > 3.8 V.
(2) Quiescent current specification is non-switching current consumption without including the current in the external-feedback resistor divider.

DC Electrical Characteristics (continued)

V_{IN} = 8 V to 18 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CONTROLLER						
$V_{boost7V}$	Boost V_{OUT} = 7 V	DIV = low, V_{BAT} = 2 V to 7 V	6.8	7	7.3	V
$V_{boost7V\text{-}th}$	Boost-enable threshold	Boost V_{OUT} = 7 V, V_{BAT} falling	7.5	8	8.5	V
	Boost-disable threshold	Boost V_{OUT} = 7 V, V_{BAT} rising	8	8.5	9	
	Boost hysteresis	Boost V_{OUT} = 7 V, V_{BAT} rising or falling	0.4	0.5	0.6	
$V_{boost10V}$	Boost V_{OUT} = 10 V	DIV = open, V_{BAT} = 2 V to 10 V	9.7	10	10.4	V
$V_{boost10V\text{-}th}$	Boost-enable threshold	Boost V_{OUT} = 10 V, V_{BAT} falling	10.5	11	11.5	V
	Boost-disable threshold	Boost V_{OUT} = 10 V, V_{BAT} rising	11	11.5	12	
	Boost hysteresis	Boost V_{OUT} = 10 V, V_{BAT} rising or falling	0.4	0.5	0.6	
$V_{boost11V}$	Boost V_{OUT} = 11 V	DIV = V_{REG}, V_{BAT} = 2 V to 11 V	10.7	11	11.4	V
$V_{boost11V\text{-}th}$	Boost-enable threshold	Boost V_{OUT} = 11 V, V_{BAT} falling	11.5	12	12.5	V
	Boost-disable threshold	Boost V_{OUT} = 11 V, V_{BAT} rising	12	12.5	13	
	Boost hysteresis	Boost V_{OUT} = 11 V, V_{BAT} rising or falling	0.4	0.5	0.6	
BOOST-SWITCH CURRENT LIMIT						
V_{DS}	Current-limit sensing	DS input with respect to PGNDA	0.175	0.2	0.225	V
t_{DS}	Leading-edge blanking			200		ns
GATE DRIVER FOR BOOST CONTROLLER						
$I_{GC1\ Peak}$	Gate-driver peak current			1.5		A
$r_{DS(on)}$	Source and sink driver	V_{REG} = 5.8 V, I_{GC1} current = 200 mA			2	Ω
GATE DRIVER FOR PMOS						
$r_{DS(on)}$	PMOS OFF			10	20	Ω
I_{PMOS_ON}	Gate current	V_{IN} = 13.5 V, V_{GS} = –5 V	10			mA
t_{delay_ON}	Turnon delay	C = 10 nF		5	10	µs
BOOST-CONTROLLER SWITCHING FREQUENCY						
$f_{sw\text{-}Boost}$	Boost switching frequency				f_{SW_Buck} / 2	kHz
D_{Boost}	Boost duty cycle				90%	
ERROR AMPLIFIER (OTA) FOR BOOST CONVERTERS						
Gm_{BOOST}	Forward transconductance	V_{BAT} = 12 V	0.8		1.35	mS
		V_{BAT} = 5 V	0.35		0.65	
BUCK CONTROLLERS						
V_{BuckA} or V_{BuckB}	Adjustable output-voltage range		0.9		11	V
$V_{ref,\ NRM}$	Internal reference and tolerance voltage in normal mode	Measure FBX pin	0.792	0.800	0.808	V
			–1%		1%	
$V_{ref,\ LPM}$	Internal reference and tolerance voltage in low-power mode	Measure FBX pin	0.784	0.800	0.816	V
			–2%		2%	
V_{sense}	V sense for forward-current limit in CCM	FBx = 0.75 V (low duty cycle)	60	75	90	mV
	V sense for reverse-current limit in CCM	FBx = 1 V	–65	–37.5	–23	mV
$V_{I\text{-}Foldback}$	V sense for output short	FBx = 0 V	17	32.5	48	mV
t_{dead}	Shoot-through delay, blanking time			20		ns
DC_{NRM}	High-side minimum on-time			100		ns
	Maximum duty cycle (digitally controlled)			98.75%		
DC_{LPM}	Duty cycle, LPM				80%	
I_{LPM_Entry}	LPM entry-threshold load current as fraction of maximum set load current			1%	See[3]	
I_{LPM_Exit}	LPM exit-threshold load current as fraction of maximum set load current		See[3]	10%		

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(3) The exit threshold specification is to be always higher than the entry threshold.

DC Electrical Characteristics (continued)

V_{IN} = 8 V to 18 V, T_J = –40°C to 150°C (unless otherwise noted)

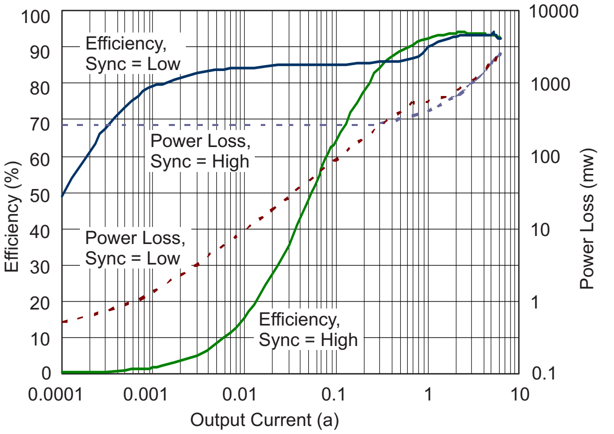
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-SIDE EXTERNAL NMOS GATE DRIVERS FOR BUCK CONTROLLER						
I_{GX1_peak}	Gate-driver peak current			0.7		A
$r_{DS(on)}$	Source and sink driver	V_{REG} = 5.8 V, I_{GX1} current = 200 mA			4	Ω
LOW-SIDE NMOS GATE DRIVERS FOR BUCK CONTROLLER						
I_{GX2_peak}	Gate driver peak current			0.7		A
$R_{DS\ ON}$	Source and sink driver	V_{REG} = 5.8 V, I_{GX2} current = 200 mA			4	Ω
ERROR AMPLIFIER (OTA) FOR BUCK CONVERTERS						
Gm_{BUCK}	Transconductance	COMPA, COMPB = 0.8 V, source/sink = 5 µA, test in feedback loop	0.72	1	1.35	mS
I_{PULLUP_FBx}	Pullup current at FBx pins	FBx = 0 V	50	100	200	nA
DIGITAL INPUTS: ENA, ENB, ENC, SYNC						
V_{IH}	Higher threshold	V_{IN}= 13 V	1.7			V
V_{IL}	Lower threshold	V_{IN} = 13 V			0.7	V
R_{IH_SYNC}	Pulldown resistance on SYNC	V_{SYNC} = 5 V		500		kΩ
R_{IL_ENC}	Pulldown resistance on ENC	V_{ENC} = 5 V		500		kΩ
I_{IL_ENx}	Pullup current source on ENA, ENB	V_{ENx} = 0 V,		0.5	2	µA
BOOST OUTPUT VOLTAGE: DIV						
V_{IH_DIV}	Higher threshold	V_{REG} = 5.8 V	V_{REG} – 0.2			V
V_{IL_DIV}	Lower threshold				0.2	V
V_{oz_DIV}	Voltage on DIV if unconnected	Voltage on DIV if unconnected		V_{REG} / 2		V
SWITCHING PARAMETER – BUCK DC-DC CONTROLLERS						
f_{SW_Buck}	Buck switching frequency	RT pin: GND	360	400	440	kHz
f_{SW_Buck}	Buck switching frequency	RT pin: 60-kΩ external resistor	360	400	440	kHz
f_{SW_adj}	Buck adjustable range with external resistor	RT pin: external resistor	150		600	kHz
f_{SYNC}	Buck synchronization range	External clock input	150		600	kHz
f_{SS}	Spread-spectrum spreading	TPS43336-Q1 only		5%		
INTERNAL GATE-DRIVER SUPPLY						
V_{REG}	Internal regulated supply	V_{IN} = 8 V to 18 V, V_{EXTSUP} = 0 V, SYNC = high	5.5	5.8	6.1	V
	Load regulation	I_{VREG} = 0 mA to 100 mA, V_{EXTSUP} = 0 V, SYNC = high		0.2%	1%	
$V_{REG(EXTSUP)}$	Internal regulated supply	V_{EXTSUP} = 8.5 V	7.2	7.5	7.8	V
	Load regulation	I_{EXTSUP} = 0 mA to 125 mA, SYNC = High V_{EXTSUP} = 8.5 V to 13 V		0.2%	1%	
$V_{EXTSUP\text{-}th}$	EXTSUP switch-over voltage threshold	I_{VREG} = 0 mA to 100 mA, V_{EXTSUP} ramping positive	4.4	4.6	4.8	V
$V_{EXTSUP\text{-}Hys}$	EXTSUP switch-over hysteresis		150		250	mV
$I_{VREG\text{-}Limit}$	Current limit on VREG	V_{EXTSUP} = 0 V, normal mode as well as LPM	100		400	mA
$I_{VREG\_EXTSUP\text{-}Limit}$	Current limit on VREG when using EXTSUP	I_{VREG} = 0 mA to 100 mA, V_{EXTSUP} = 8.5 V, SYNC = High	125		400	mA
SOFT START						
I_{SSx}	Soft-start source current	V_{SSA} and V_{SSB} = 0 V	0.75	1	1.25	µA
OSCILLATOR (RT)						
V_{RT}	Oscillator reference voltage			1.2		V

DC Electrical Characteristics (continued)

V_{IN} = 8 V to 18 V, T_J = –40°C to 150°C (unless otherwise noted)

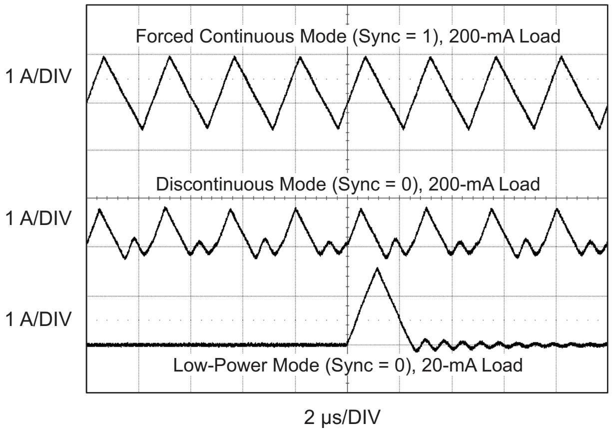
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD / DELAY						
PG_{pullup}	Pullup for A and B to Sx2			50		kΩ
PG_{th1}	Power-good threshold	FBx falling	–5%	–7%	–9%	
PG_{hys}	Hysteresis			2%		
PG_{drop}	Voltage drop	I_{PGA} = 5 mA			450	mV
		I_{PGA} = 1 mA			100	mV
PG_{leak}	Power-good leakage	V_{Sx2} = V_{PGx} = 13 V			1	µA
$t_{deglitch}$	Power-good deglitch time		2		16	µs
t_{delay}	Reset delay	External capacitor = 1 nF V_{BuckX} < PG_{th1}		1		ms
t_{delay_fix}	Fixed reset delay	No external capacitor, pin open		20	50	µs
I_{OH}	Activate current source (current to charge external capacitor)		30	40	50	µA
I_{IL}	Activate current sink (current to discharge external capacitor)		30	40	50	µA
OVERTEMPERATURE PROTECTION						
$T_{shutdown}$	Junction-temperature shutdown threshold		150	165		°C
T_{hys}	Junction-temperature hysteresis			15		°C

6.6 Typical Characteristics



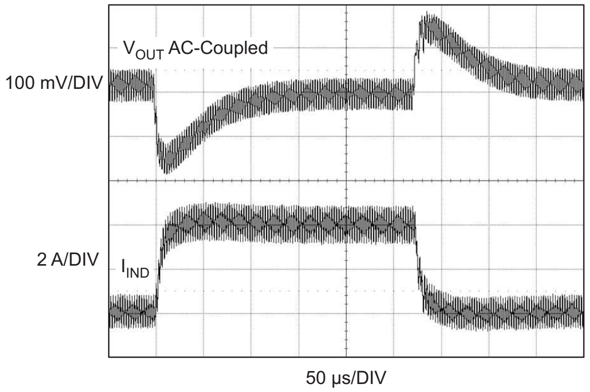
V_{IN} = 12 V   L= 4.7 µH f_{SW} = 400 kHz
V_{OUT} = 5 V R_{SENSE} = 10 Ω

Figure 2. Efficiency Across Output Currents (Bucks)



V_{IN} = 12 V   L= 4.7 µH f_{SW} = 400 kHz
V_{OUT} = 5 V R_{SENSE} = 10 Ω

Figure 3. Inductor Currents (Buck)



V_{IN} = 12 V   L= 4.7 µH f_{SW} = 400 kHz
V_{OUT} = 5 V R_{SENSE} = 10 Ω

Figure 4. Buck Load Step: Forced Continuous Mode (0 to 4 A at 2.5 A/µs)

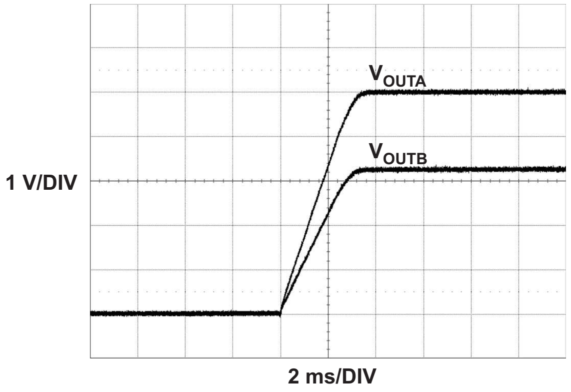
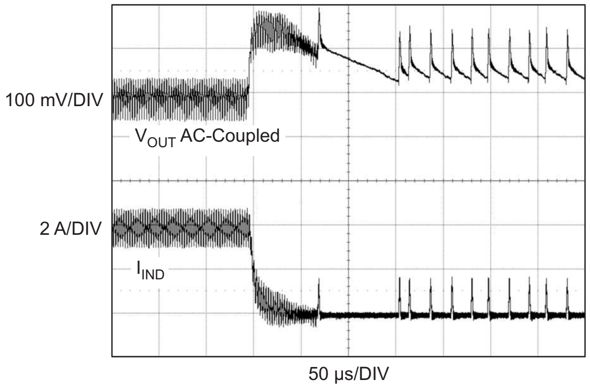
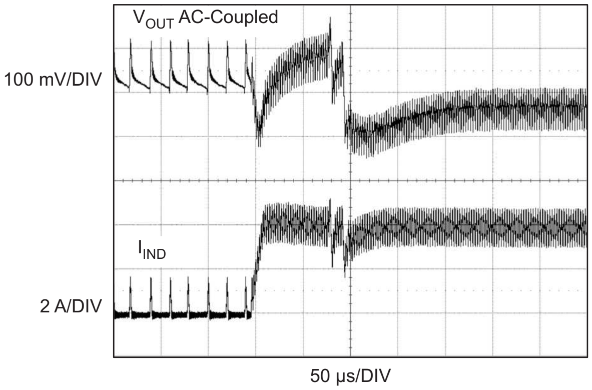


Figure 5. Soft-Start Outputs (Buck)



V_{IN} = 12 V   L= 4.7 µH f_{SW} = 400 kHz
V_{OUT} = 5 V R_{SENSE} = 10 Ω

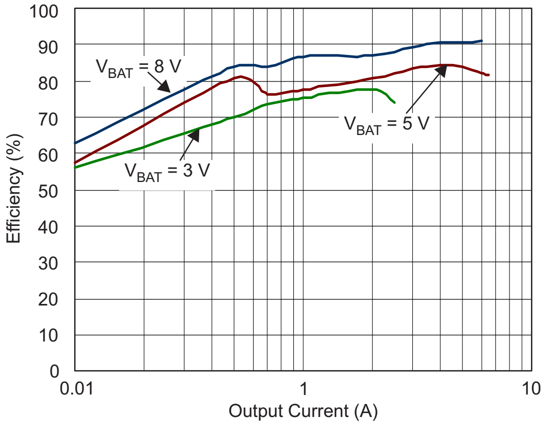
Figure 6. Buck Load Step: Low-Power-Mode Entry (4 A to 90 mA at 2.5 A/µs)



V_{IN} = 12 V   L= 4.7 µH f_{SW} = 400 kHz
V_{OUT} = 5 V R_{SENSE} = 10 Ω

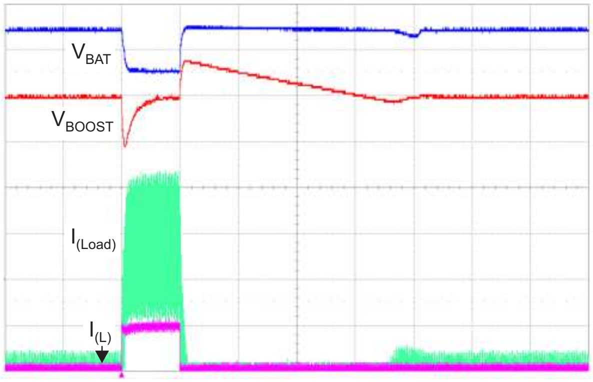
Figure 7. Buck Load Step: Low-Power-Mode Exit (90 mA to 4 A at 2.5 A/µs)

Typical Characteristics (continued)



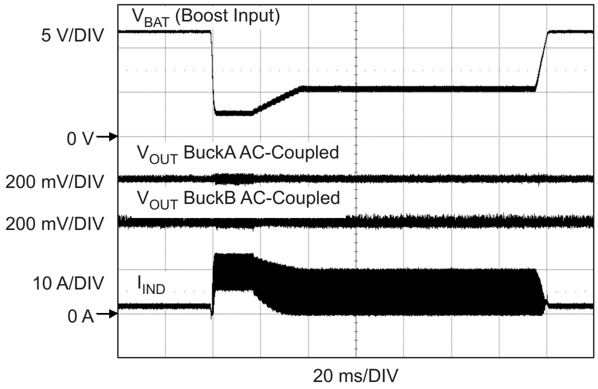
V_{IN} (BOOST OUTPUT) = 10 V f_{SW} = 200 kHz
L = 1 µH R_{SENSE} = 7.5 mΩ

Figure 8. Efficiency Across Output Currents (Boost)



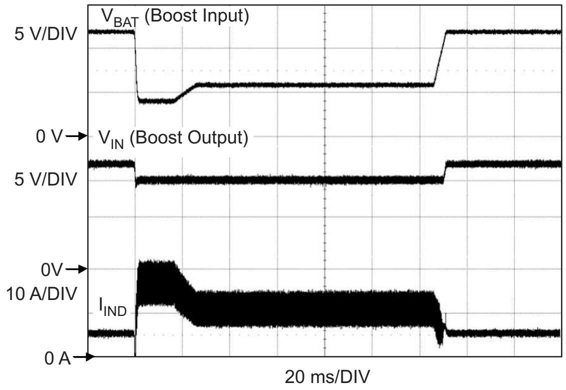
V_{BAT} (BOOST INPUT) = 5 V f_{SW} = 200 kHz
V_{IN} (BOOST OUTPUT) = 10 V L = 680 nH
C_{IN} = 440 µF C_{OUT} = 660 µF R_{SENSE} = 10 mΩ

**Figure 9. Load Step Response (Boost)
(0 to 5 A at 10 A/µs)**



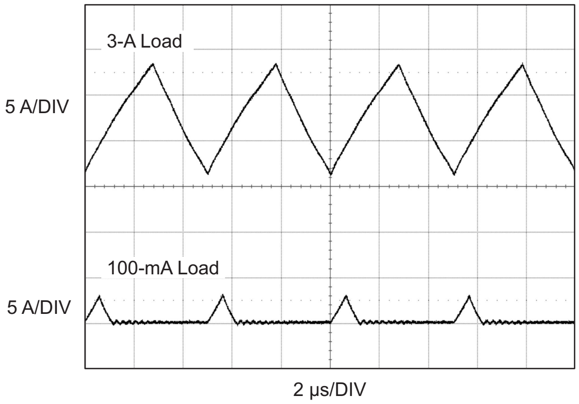
V_{IN} (BOOST OUTPUT) = 10 V f_{SW} = 200 kHz
BuckA = 5 V AT 1.5 A C_{IN} = 440 µF L = 1 µH
BuckB = 3.3 V AT 3.5 A C_{OUT} = 660 µF R_{SENSE} = 7.5 mΩ

**Figure 10. Cranking Pulse Boost Response
(12 V to 3 V in 1 ms at Buck Outputs 7.5 W / 11.5 W)**



V_{IN} (BOOST OUTPUT) = 10 V f_{SW} = 200 kHz
BuckA = 5 V AT 1.5 A C_{IN} = 440 µF L = 1 µH
BuckB = 3.3 V AT 3.5 A C_{OUT} = 660 µF R_{SENSE} = 7.5 mΩ

**Figure 11. Cranking Pulse Boost Response
(12 V to 4 V in 1 ms at Boost Direct Output 25 W)**



V_{BAT} (BOOST INPUT) = 5 V f_{SW} = 200 kHz
V_{IN} (BOOST OUTPUT) = 10 V L = 1 µH
C_{IN} = 440 µF C_{OUT} = 660 µF R_{SENSE} = 7.5 mΩ

Figure 12. Inductor Currents (Boost)

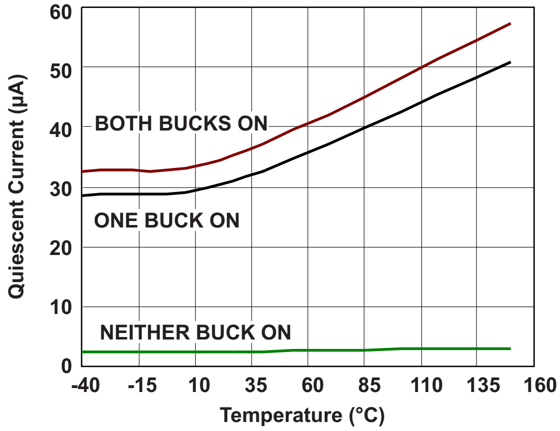


Figure 13. No-Load Quiescent Current vs Temperature

Typical Characteristics (continued)

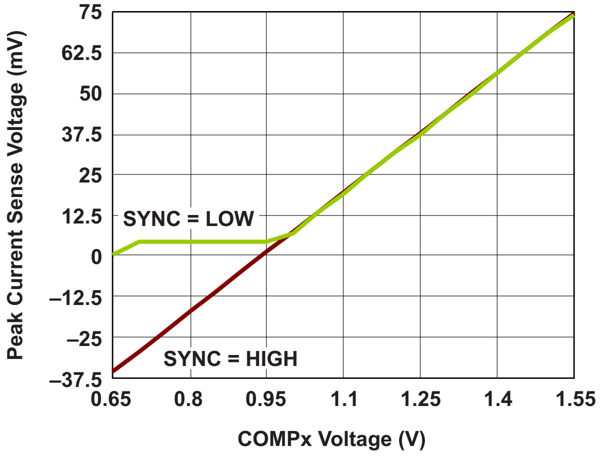


Figure 14. Buckx Peak Current Limit vs Compx Voltage

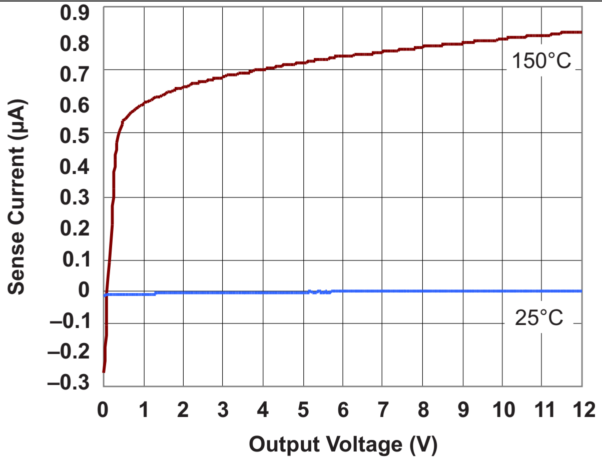


Figure 15. Current-Sense Pins Input Current (Buck)

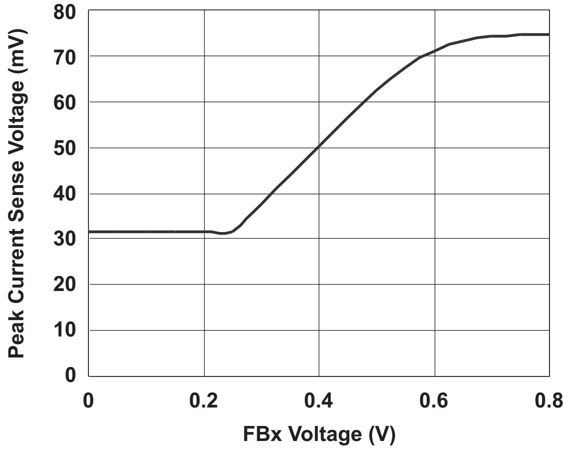


Figure 16. Foldback Current Limit (Buck)

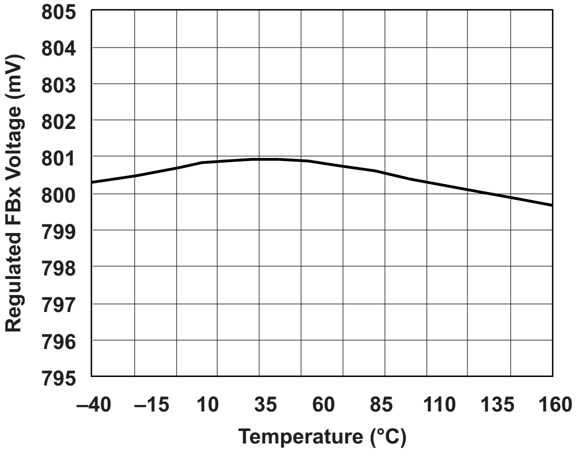


Figure 17. Regulated Fbx Voltage vs Temperature (Buck)

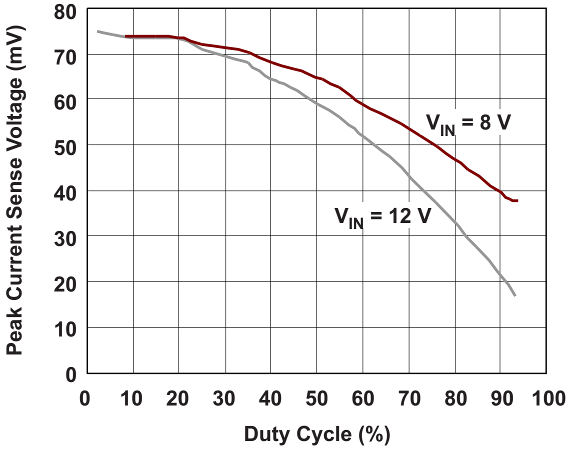


Figure 18. Current Limit vs Duty Cycle (Buck)

7 Detailed Description

7.1 Overview

The TPS43335-Q1 and TPS43336-Q1 devices include two current-mode synchronous buck controllers and a voltage mode boost controller. The integrated boost controller allows the devices to operate down to 2 V at the input without seeing a drop on the buck regulator output stages. At light loads, one can enable the buck controllers to operate automatically in low-power mode, consuming just 30 μA of quiescent current. The buck controllers have independent soft-start capability and power-good indicators. Current foldback in the buck controllers and cycle-by-cycle current limitation in the boost controller provide external MOSFET protection. The switching frequency is programmable over 150 kHz to 600 kHz or can be synchronized to an external clock in the same range. The TPS43336-Q1 device also offers frequency-hopping spread-spectrum operation.

7.2 Functional Block Diagram

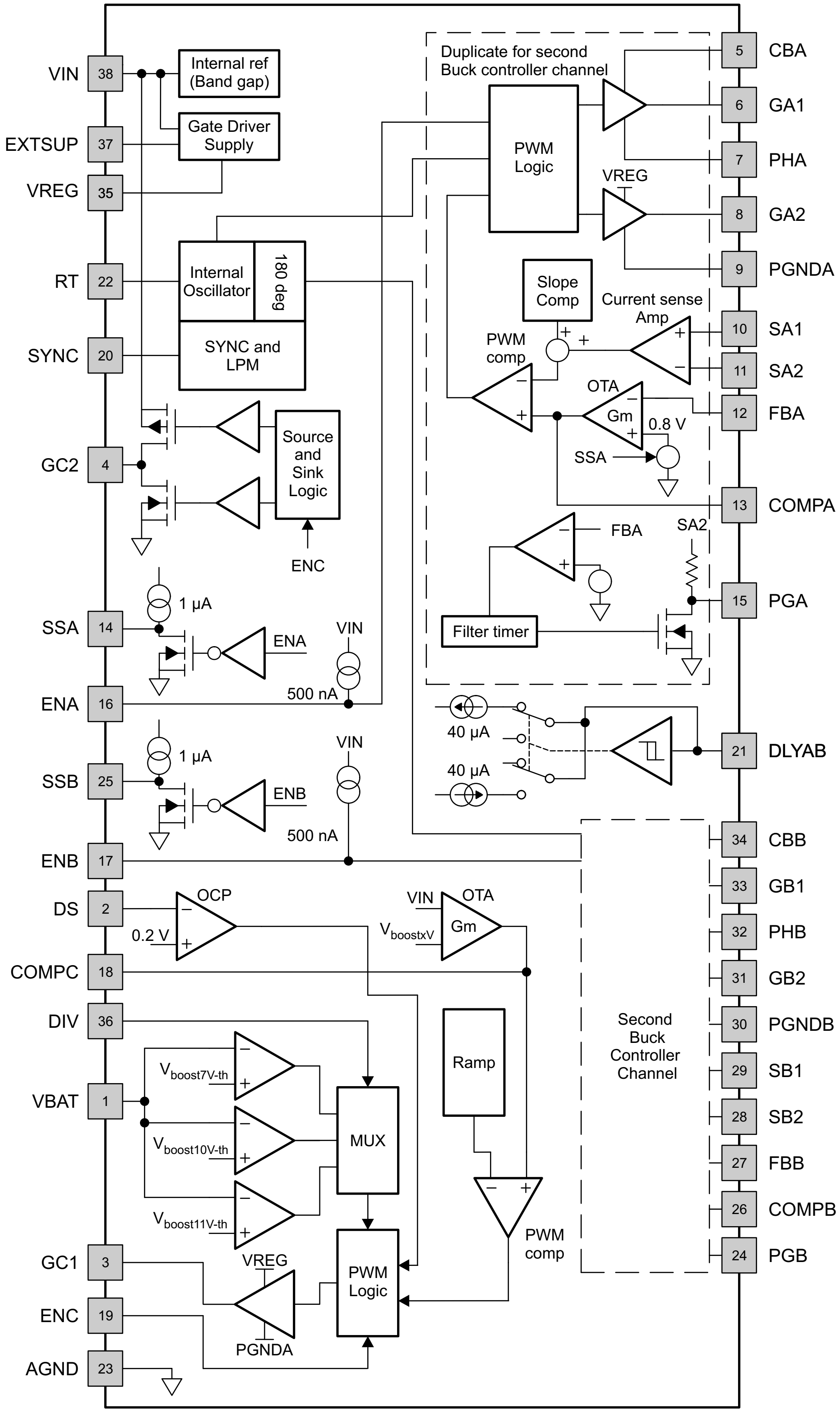


Figure 19. Functional Block Diagram

7.3 Feature Description

7.3.1 Buck Controllers: Normal Mode PWM Operation

7.3.1.1 Frequency Selection and External Synchronization

The buck controllers operate using constant-frequency peak-current-mode control for optimal transient behavior and ease of component choices. The switching frequency is programmable between 150 kHz and 600 kHz, depending upon the resistor value at the RT pin. A short circuit to ground at this pin sets the default switching frequency to 400 kHz. Using a resistor at RT, one can set another frequency according to the formula:

$$f_{SW} = \frac{X}{RT} \quad (X = 24\ k\Omega \times MHz)$$

$$f_{SW} = 24 \times \frac{10^9}{RT} \tag{1}$$

For example,

600 kHz requires 40 kΩ

150 kHz requires 160 kΩ

It is also possible to synchronize to an external clock at the SYNC pin in the same frequency range of 150 kHz to 600 kHz. The device detects clock pulses at this pin, and an internal PLL locks on to the external clock within the specified range. The device can also detect a loss of clock at this pin, and when this condition is detected, the device sets the switching frequency to the internal oscillator. The two buck controllers operate at identical switching frequencies, 180 degrees out-of-phase.

7.3.1.2 Enable Inputs

Independent enable inputs from the ENA and ENB pins enable the buck controllers. These are high-voltage pins, with a threshold of 1.7 V for the high level, and with direct connection to the battery permissible for self-bias. The low threshold is 0.7 V. Both these pins have internal pullup currents of 0.5 µA (typical). As a result, an open circuit on these pins enables the respective buck controllers. When both buck controllers are disabled, the device shuts down and consumes a current of less than 4 µA.

7.3.1.3 Feedback Inputs

The right resistor feedback divider network connected to the FBx (feedback) pins sets the output voltage. Choose this network such that the regulated voltage at the FBx pin equals 0.8 V. The FBx pins have a 100-nA pullup current source as a protection feature in case the pins open up as a result of physical damage.

7.3.1.4 Soft-Start Inputs

In order to avoid large inrush currents, each buck controller has an independent programmable soft-start timer. The voltage at the SSx pin acts as the soft-start reference voltage. The 1-µA pullup current available at the SSx pins, in combination with a suitably chosen capacitor, generates a ramp of the desired soft-start speed. After start-up, the pullup current ensures that SSx is higher than the internal reference of 0.8 V; 0.8 V then becomes the reference for the buck controllers. Use Equation 2 to calculate the soft-start ramp time.

$$C_{SS} = \frac{I_{SS} \times \Delta t}{\Delta V} \quad (Farads)$$

where

- I_{SS} = 1 µA (typical)
- ΔV = 0.8 V
- C_{SS} is the required capacitor for Δt, the desired soft-start time. (2)

An alternative use of the soft-start pins is as tracking inputs. In this case, connect them to the supply to be tracked via a suitable resistor-divider network.

Feature Description (continued)

7.3.1.5 Current-Mode Operation

Peak-current-mode control regulates the peak current through the inductor to maintain the output voltage at its set value. The error between the feedback voltage at FBx and the internal reference produces a signal at the output of the error amplifier (COMPx) which serves as the target for the peak inductor current. The device senses the current through the inductor as a differential voltage at Sx1–Sx2 and compares voltage with this target during each cycle. A fall or rise in load current produces a rise or fall in voltage at FBx, causing V_{COMPx} to fall or rise respectively, thus increasing or decreasing the current through the inductor until the average current matches the load. This process maintains the output voltage in regulation.

The top N-channel MOSFET turns on at the beginning of each clock cycle and stays on until the inductor current reaches its peak value. Once this MOSFET turns off, and after a small delay (shoot-through delay) the lower N-channel MOSFET turns on until the start of the next clock cycle. In dropout operation, the high-side MOSFET stays on continuously. In every fourth clock cycle, there is a limit on the duty cycle of 95% in order to charge the bootstrap capacitor at CBx. This allows a maximum duty cycle of 98.75% for the buck regulators. During dropout, the buck regulator switches at one-fourth of its normal frequency.

7.3.1.6 Current Sensing and Current Limit With Foldback

Clamping of the maximum value of COMPx is such as to limit the maximum current through the inductor to a specified value. When the output of the buck regulator (and hence the feedback value at FBx) falls to a low value due to a short circuit or overcurrent condition, the clamped voltage at COMPx successively decreases, thus providing current foldback protection, which protects the high-side external MOSFET from excess current (forward-direction current limit).

Similarly, if a fault condition shorts the output to a high voltage and the low-side MOSFET turns fully on, the COMPx node drops low. A clamp is on its lower end as well, in order to limit the maximum current in the low-side MOSFET (reverse-direction current limit).

An external resistor senses the current through the inductor. Choose the sense resistor such that the maximum forward peak current in the inductor generates a voltage of 75 mV across the sense pins. This specified value is for low duty cycles only. At typical duty-cycle conditions around 40% (assuming 5-V output and 12-V input), 50 mV is a more reasonable value, considering tolerances and mismatches. The *Typical Characteristics* section provides a guide for using the correct current-limit sense voltage.

The current-sense pins Sx1 and Sx2 are high-impedance pins with low leakage across the entire output range, thus allowing DCR current sensing using the dc resistance of the inductor for higher efficiency. Figure 20 shows DCR sensing. Here, the series resistance (DCR) of the inductor is the sense element. Place the filter components close to the device for noise immunity. Remember that while the DCR sensing gives high efficiency, it is inaccurate due to the temperature sensitivity and a wide variation of the parasitic inductor series resistance. Hence, it may often be advantageous to use the more-accurate sense resistor for current sensing.

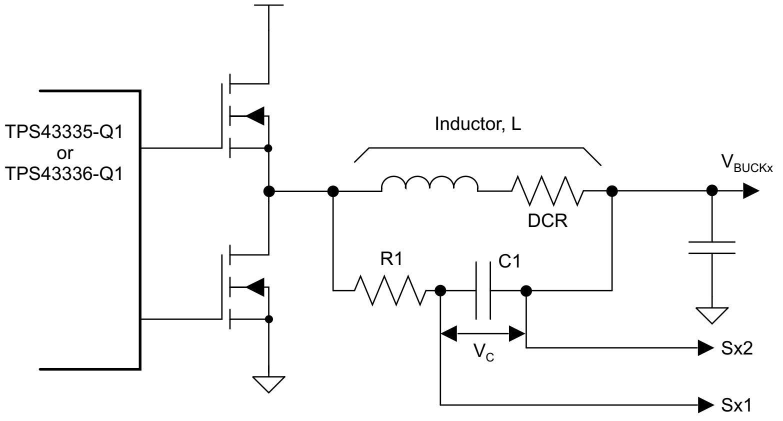


Figure 20. DCR Sensing Configuration

Feature Description (continued)

7.3.1.7 Slope Compensation

Optimal slope compensation which is adaptive to changes in input voltage and duty cycle allows stable operation under all conditions. For optimal performance of this circuit, choose the inductor and sense resistor according to the following:

$$\frac{L \times f_{SW}}{R_S} = 200$$

where

- L is the buck regulator inductor in henries.
- R_S is the sense resistor in ohms.
- f_{sw} is the buck-regulator switching frequency in hertz. (3)

7.3.1.8 Power-Good Outputs and Filter Delays

Each buck controller has an independent power-good comparator monitoring the feedback voltage at the FBx pins and indicating whether the output voltage has fallen below a specified power-good threshold. This threshold has a typical value of 93% of the regulated output voltage. The power-good indicator is available as an open-drain output at the PGx pins. An internal 50-kΩ pullup resistor to Sx2 is available, or use of an external resistor is possible. Shutdown of a buck controller causes an internal pulldown of the power-good indicator. Connecting the pullup resistor to a rail other than the output of that particular buck channel causes a constant current flow through the resistor when the buck controller is powered down.

In order to avoid triggering the power-good indicators due to noise or fast transients on the output voltage, the device uses an internal delay circuit for de-glitching. Similarly, when the output voltage returns to its set value after a long negative transient, assertion of the power-good indicator (release of the open-drain pin) occurs after the same delay. Use of this delay can pause the reset of circuits powered from the buck regulator rail. Program the duration of the delay of by using a suitable capacitor at the DLYAB pin according to the equation:

$$\frac{t_{DELAY}}{C_{DLYAB}} = \frac{1\,ms}{1\,nF} \tag{4}$$

When the DLYAB pin is open, the delay setting is for a default value of 20 µs typical. The power-good delay timing is common to both the buck rails, but the power-good comparators and indicators function independently.

7.3.1.9 Light-Load PFM Mode

An external clock or a high level on the SYNC pin results in forced continuous-mode operation of the bucks. An open or low on the SYNC pin allows the buck controllers to operate in discontinuous mode at light loads by turning off the low-side MOSFET on detection of a zero-crossing in the inductor current.

In discontinuous mode, as the load decreases, the duration when both the high-side and low-side MOSFETs turn off increases (deep discontinuous mode). In case the duration exceeds 60% of the clock period and $V_{BAT} > 8$ V, the buck controller switches to a low-power operation mode. The design ensures that this typically occurs at 1% of the set full-load current if the choice of the inductor and sense resistor is as recommended in the slope compensation section.

In low-power PFM mode, the buck monitors the FBx voltage and compares it with the 0.8-V internal reference. Whenever the FBx value falls below the reference, the high-side MOSFET turns on for a pulse duration inversely proportional to the difference VIN – Sx2. At the end of this on-time, the high-side MOSFET turns off and the current in the inductor decays until it becomes zero. The low-side MOSFET does not turn on. The next pulse occurs the next time FBx falls below the reference value. This results in a constant volt-second t_{on} hysteretic operation with a total device quiescent current consumption of 30 µA when a single buck channel is active and 35 µA when both channels are active.

As the load increases, the pulses become more and more frequent and move closer to each other until the current in the inductor becomes continuous. At this point, the buck controller returns to normal fixed-frequency current-mode control. Another criterion to exit the low-power mode is when VIN falls low enough to require higher than 80% duty cycle of the high-side MOSFET.

Feature Description (continued)

The TPS43335-Q1 and TPS43336-Q1 can support the full-current load during low-power mode until the transition to normal mode takes place. The design ensures that exit of the low-power mode occurs at 10% (typical) of full-load current if the selection of inductor and sense resistor is as recommended. Moreover, there is always a hysteresis between the entry and exit thresholds to avoid oscillating between the two modes.

In the event that both buck controllers are active, low-power mode is only possible when both buck controllers have light loads that are low enough for low-power mode entry. With the boost controller enabled, low-power mode is possible only if V_{BAT} is high enough to prevent the boost from switching and if DIV is open or set to GND. A high (V_{REG}) level on DIV inhibits low-power mode, unless ENC is set to low.

7.3.2 Boost Controller

The boost controller has a fixed-frequency voltage-mode architecture and includes cycle-by-cycle current-limit protection for the external N-channel MOSFET. The boost-controller switching-frequency setting is one-half of the buck-controller switching frequency. An internal resistor-divider network programmable to 7 V, 10 V, or 11 V sets the output voltage of the boost controller at the VIN pin, based on the low, open, or high status, respectively, of the DIV pin. The device does not recognize a change of the DIV setting while the in the low-power mode.

The active-high ENC pin enables the boost controller, which is active when the input voltage at the VBAT pin has crossed the unlock threshold of 8.5 V at least once. A single threshold crossing arms the boost controller, which starts switching as soon as V_{IN} falls below the value set by the DIV pin, regulating the VIN voltage. Thus, the boost regulator maintains a stable input voltage for the buck regulators during transient events such as a cranking pulse at VBAT.

The voltage at the DS pin exceeding 200 mV pulls the CG1 pin low, turning off the boost external MOSFET. Connecting the DS pin to the drain of the MOSFET or to a sense resistor between the MOSFET source and ground achieves cycle-by-cycle overcurrent protection for the MOSFET. Choose the on-resistance of the MOSFET or the value of the sense resistor in such a way that the on-state voltage at the DS does not exceed 200 mV at the maximum-load and minimum-input-voltage conditions. When using a sense resistor, TI recommends connecting a filter network between the DS pin and the sense resistor for better noise immunity.

One can use the boost output (VIN) to supply other circuits in the system. However, they should be high-voltage tolerant. The device regulates the boost output to the programmed value only when VIN is low, and so VIN can reach battery levels.

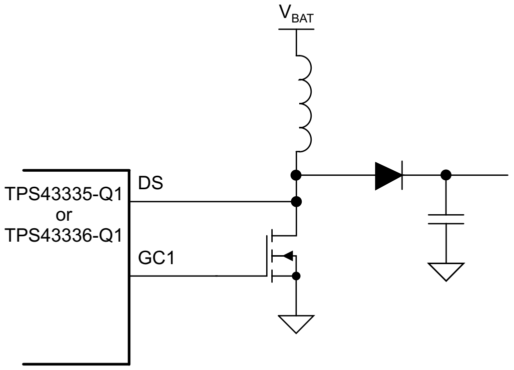


Figure 21. External Drain-Source Voltage Sensing

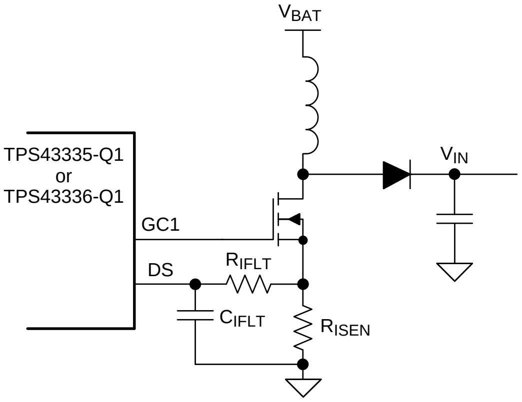


Figure 22. External Current Shunt Resistor

Feature Description (continued)

7.3.3 Frequency-Hopping Spread Spectrum (TPS43336-Q1 Only)

The TPS43336-Q1 features a frequency-hopping pseudo-random spectrum-spreading architecture. On this device, whenever the SYNC pin is high, the internal oscillator frequency varies from one cycle to the next within a band of ±5% around the value programmed by the resistor at the RT pin. The implementation uses a linear-feedback shift register that changes the frequency of the internal oscillator based on a digital code. The shift register is long enough to make the hops pseudo-random in nature and has a design such that the frequency shifts only by one step at each cycle to avoid large jumps in the buck and boost switching frequencies.

Table 1. Frequency-Hopping Control

SYNC TERMINAL	FREQUENCY SPREAD SPECTRUM (FSS)	COMMENTS
External clock	Not active	Device in forced continuous mode, internal PLL locks into external clock between 150 kHz and 600 kHz.
Low or open	Not active	Device can enter discontinuous mode. Automatic LPM entry and exit, depending on load conditions
High	TPS43335-Q1: FSS not active	Device in forced continuous mode
	TPS43336-Q1: FSS active	

7.3.4 Gate-Driver Supply (VREG, EXTSUP)

The gate-driver supplies of the buck and boost controllers are from an internal linear regulator whose output (5.8 V typical) is on the VREG pin and requires decoupling with a ceramic capacitor in the range of 3.3 µF to 10 µF. This pin has internal current-limit protection; do not use it to power any other circuits.

NOTE

VREG is not powered if no regulator is enabled, therefore it is not suitable to enable the regulators.

VIN powers the VREG linear regulator by default when the EXTSUP voltage is lower than 4.6 V (typical). If there is an expectation of V_{IN} going to high levels, there can be excessive power dissipation in this regulator, especially at high switching frequencies and when using large external MOSFETs. In this case, it is advantageous to power this regulator from the EXTSUP pin, which can have a connection to a supply lower than V_{IN} but high enough to provide the gate drive. When the voltage on EXTSUP is greater than 4.6 V, the linear regulator automatically switches to EXTSUP as its input, to provide this advantage. Efficiency improvements are possible when using one of the switching regulator rails from the TPS43335-Q1 or TPS43336-Q1 or any other voltage available in the system to power EXTSUP. The maximum voltage for application to EXTSUP is 9 V.

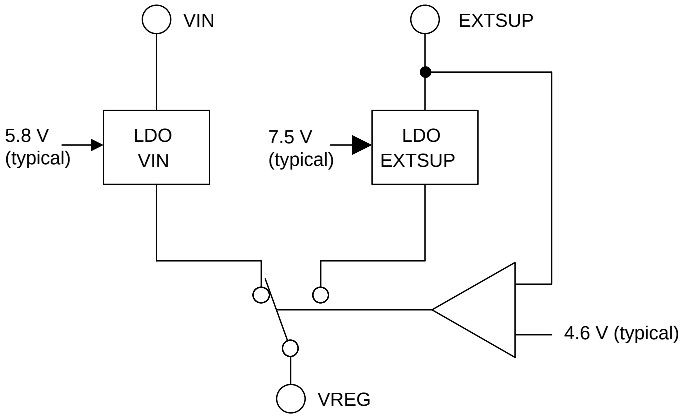


Figure 23. Internal Gate-Driver Supply

Using a voltage above 5.8 V (sourced by VIN) for EXTSUP is advantageous, as it provides a large gate drive and hence better on-resistance of the external MOSFETs.

When using EXTSUP, always keep the buck rail supplying EXTSUP enabled. Alternatively, if it is necessary to switch off the buck rail supplying EXTSUP, place a diode between the buck rail and EXTSUP.

During low-power mode, the EXTSUP functionality is not available. The internal regulator operates as a shunt regulator powered from VIN and has a typical value of 7.5 V. Current-limit protection for VREG is available in low-power mode as well. If EXTSUP is unused, leave the pin open without a capacitor installed.

7.3.5 External P-Channel Drive (GC2) and Reverse Battery Protection

The TPS43335-Q1 and TPS43336-Q1 include a gate driver for an external P-channel MOSFET which can connect across the rectifier diode of the boost regulator. Such connection is useful to reduce power losses when the boost controller is not switching. The gate driver provides a swing of 6 V typical below the VIN voltage in order to drive a P-channel MOSFET. When V_{BAT} falls below the boost-enable threshold, the gate driver turns off the P-channel MOSFET, eliminating the diode bypass.

Another use for the gate driver is to bypass any additional protection diodes connected in series, as shown in Figure 24.

The bypass-design should be chosen with the following considerations in mind:

The FETs need to have a current-rating to support the maximum output power at minimum voltage (before Boost gets activated, typically 1 V above the set boost-voltage). The FETs Drain-Source-Voltage also needs to support the worst case transients on VBAT, potentially causing a reverse voltage due to capacitors on the Source.

The Zener-Diode protects the FET against a too high Gate-Source-voltage. Typically a rating of ~7.5 V is suitable.

The resistor limits the current to the FET and over the diode. Considering the deep boost mode and a high boost-output voltage, up to 9 V may be present between GC2 and VBAT, reduced by the Zener-voltage. As GC2 has a drive capability of 10 mA, the current needs to be limited by a series resistance of about 1kOhm (depending on Vbat(min), V(boost) and Zener-voltage).

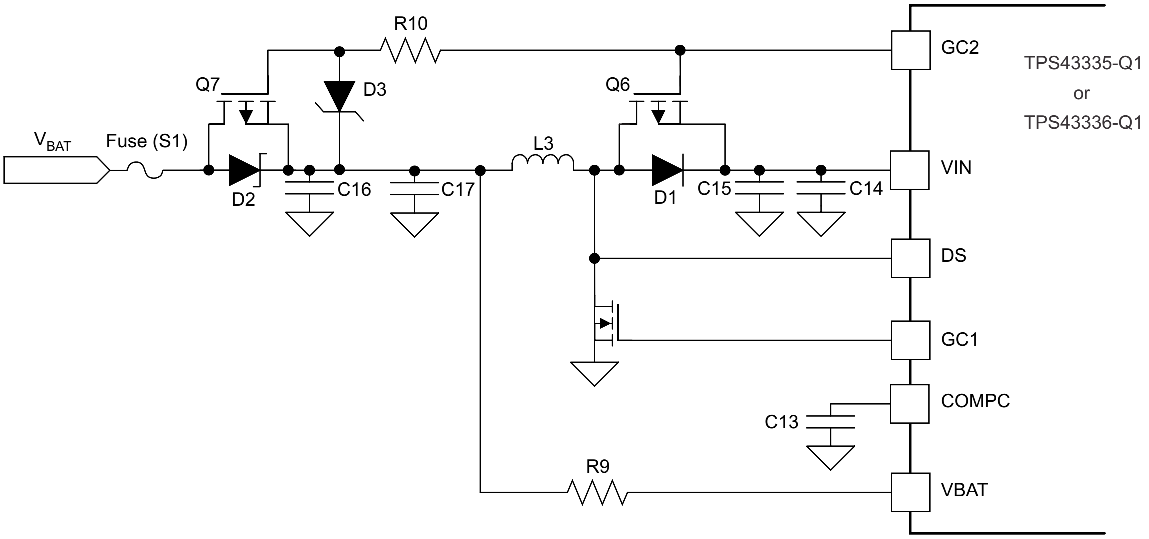


Figure 24. Reverse Battery Protection Option 1 for Buck Boost Configuration

Figure 25 also shows a different scheme of reverse battery protection, which may require only a smaller-sized diode to protect the N-channel MOSFET, as the diode conducts only for a part of the switching cycle. Because the diode is not always in the series path, the system efficiency can be improved.

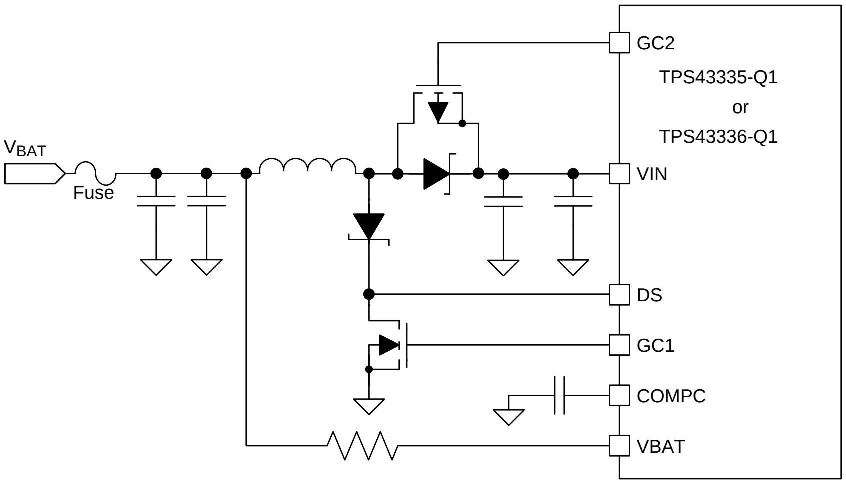


Figure 25. Reverse Battery Protection Option 2 for Buck Boost Configuration

7.3.6 Undervoltage Lockout and Overvoltage Protection

The TPS43335-Q1 and TPS43336-Q1 start up at a VIN voltage of 6.5 V (minimum), required for the internal supply (VREG). Once it has started up, the device operates down to a VIN voltage of 3.6 V; below this voltage level, the undervoltage lockout disables the device. Note: if V_{IN} drops, V_{REG}drops as well; hence, the gate-drive voltage is reduced, whereas the digital logic is fully functional. Note as well, even if ENC is high, there is a requirement to exceed the boost-unlock voltage of typically 8.5 V once, before boost activation can take place (see the *Boost Controller* section herein). A voltage of 46 V at VIN triggers the overvoltage comparator, which shuts down the device. In order to prevent transient spikes from shutting down the device, the under- and overvoltage protection have filter times of 5 µs (typical).

When the voltages return to the normal operating region, the enabled switching regulators start including a new soft-start ramp for the buck regulators.

With the boost controller enabled, a voltage less than 1.9 V (typical) on VBAT triggers an undervoltage lockout and pulls the boost gate driver (GC1) low (this action has a filter delay of 5 µs, typical). As a result, VIN falls at a rate dependent on its capacitor and load, eventually triggering VIN undervoltage. A short falling transient at VBAT even lower than 2 V can thus be survived, if V_{BAT} returns above 2.5 V before VIN is discharged to the undervoltage threshold.

7.3.7 Thermal Protection

The TPS43335-Q1 or TPS43336-Q1 protects itself from overheating using an internal thermal shutdown circuit. If the die temperature exceeds the thermal shutdown threshold of 165ºC due to excessive power dissipation (for example, due to fault conditions such as a short circuit at the gate drivers or VREG), the controllers turn off and then restart when the temperature has fallen by 15ºC.

7.4 Device Functional Modes

Table 2 lists the enable and inhibit pin configurations for the modes of operation.

Table 2. Mode of Operation

ENABLE AND INHIBIT PINS				DRIVER STATUS		DEVICE STATUS	QUIESCENT CURRENT
ENA	**ENB**	**ENC**	**SYNC**	**BUCK CONTROLLERS**	**BOOST CONTROLLER**		
Low	Low	Low	X	Shut down	Disabled	Shutdown	Approximately 4 µA
Low	High	Low	Low	BuckB running	Disabled	BuckB: LPM enabled	Approximately 30 µA (light loads)
			High			BuckB: LPM inhibited	mA range
High	Low	Low	Low	BuckA running	Disabled	BuckA: LPM enabled	Approximately 30 µA (light loads)
			High			BuckA: LPM inhibited	mA range
High	High	Low	Low	BuckA and BuckB running	Disabled	BuckA and BuckB: LPM enabled	Approximately 35 µA (light loads)
			High			BuckA and BuckB: LPM inhibited	mA range
Low	Low	Low	X	Shut down	Disabled	Shutdown	Approximately 4 µA
Low	High	High	Low	BuckB running	Boost running for V_{IN} < set boost output	BuckB: LPM enabled	Approximately 50 µA (no boost, light loads)
			High			BuckB: LPM inhibited	mA range
High	Low	High	Low	BuckA running	Boost running for V_{IN} < set boost output	BuckA: LPM enabled	Approximately 50 µA (no boost, light loads)
			High			BuckA: LPM inhibited	mA range
High	High	High	Low	BuckA and BuckB running	Boost running for V_{IN} < set boost output	BuckA and BuckB: LPM enabled	Approximately 60 µA (no boost, light loads)
			High			BuckA and BuckB: LPM inhibited	mA range

7.4.1 Buck Controllers: Current-Mode Operation

Peak-current-mode control regulates the peak current through the inductor to maintain the output voltage at its set value. The error between the feedback voltage at FBx and the internal reference produces a signal at the output of the error amplifier (COMPx) which serves as the target for the peak inductor current. The device senses the current through the inductor as a differential voltage at Sx1–Sx2 and compares voltage with this target during each cycle. A fall or rise in load current produces a rise or fall in voltage at FBx, causing V_{COMPx} to fall or rise respectively, thus increasing or decreasing the current through the inductor until the average current matches the load. This process maintains the output voltage in regulation.

The top N-channel MOSFET turns on at the beginning of each clock cycle and stays on until the inductor current reaches its peak value. Once this MOSFET turns off, and after a small delay (shoot-through delay) the lower N-channel MOSFET turns on until the start of the next clock cycle. In dropout operation, the high-side MOSFET stays on continuously. In every fourth clock cycle, a limit exists on the duty cycle of 95% to charge the bootstrap capacitor at CBx which allows a maximum duty cycle of 98.75% for the buck regulators. During dropout, the buck regulator switches at one-fourth of the normal frequency.

7.4.2 Buck Controllers: Light-Load PFM Mode

An external clock or a high level on the SYNC pin results in forced continuous-mode operation of the bucks. An open or low on the SYNC pin allows the buck controllers to operate in discontinuous mode at light loads by turning off the low-side MOSFET on detection of a zero-crossing in the inductor current.

In discontinuous mode, as the load decreases, the duration when both the high-side and low-side MOSFETs turn off increases (deep discontinuous mode). In case the duration exceeds 60% of the clock period and V_{BAT} > 8 V, the buck controller switches to a low-power operation mode. The design ensures that this typically occurs at 1% of the set full-load current if the choice of the inductor and sense resistor is as recommended in the slope-compensation section.

In low-power PFM mode, the buck monitors the FBx voltage and compares it with the 0.8-V internal reference. Whenever the FBx value falls below the reference, the high-side MOSFET turns on for a pulse duration inversely proportional to the difference VIN – Sx2. At the end of this on-time, the high-side MOSFET turns off and the current in the inductor decays until it becomes zero. The low-side MOSFET does not turn on. The next pulse occurs the next time FBx falls below the reference value. This results in a constant volt-second t_{on} hysteretic operation with a total device quiescent current consumption of 30 µA when a single buck channel is active and 35 µA when both channels are active.

As the load increases, the pulses become more and more frequent and move closer to each other until the current in the inductor becomes continuous. At this point, the buck controller returns to normal fixed-frequency current-mode control. Another criterion to exit the low-power mode is when VIN falls low enough to require higher than 80% duty cycle of the high-side MOSFET.

The TPS4333x-Q1 family of devices can support the full-current load during low-power mode until the transition to normal mode takes place. The design ensures that exit of the low-power mode occurs at 10% (typical) of full-load current if the selection of inductor and sense resistor is as recommended. Moreover, a hysteresis also exists between the entry and exit thresholds to avoid oscillating between the two modes.

In the event that both buck controllers are active, low-power mode is only possible when both buck controllers have light loads that are low enough for low-power mode entry. With the boost controller enabled, low-power mode is possible only if V_{BAT} is high enough to prevent the boost from switching and if DIV is open or set to GND. A high (V_{REG}) level on DIV inhibits low-power mode, unless the ENC pin is set to low.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS43335-Q1 and TPS43336-Q1 devices are ideally suited as a pre-regulator stage with low Iq requirements and for applications that must survive supply drops due to cranking events. The integrated boost controller allows the devices to operate down to 2 V at the input without seeing a drop on the buck regulator output stages. Below component values and calculations are a good starting point and theoretical representation of the values for use in the application; improving the performance of the device may require further optimization of the derived components.

8.2 Typical Applications

8.2.1 Automotive Infotainment Supply

This is a starting point and theoretical representation of the values for use in the application; improving the performance of the device may require further optimization of the derived components.

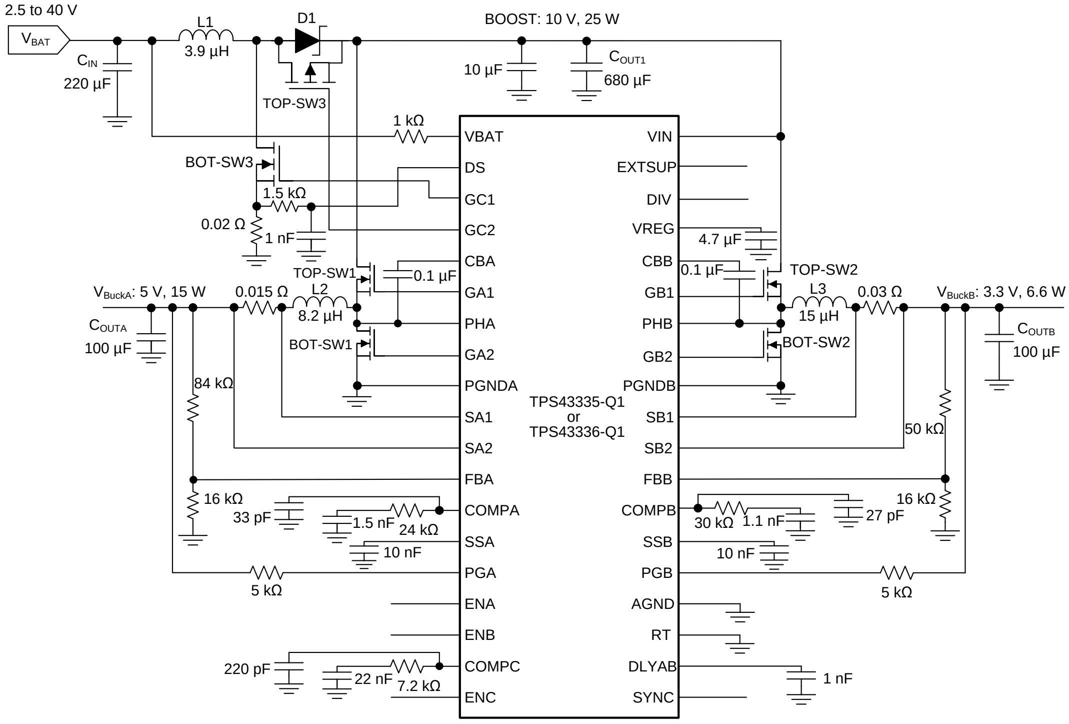


Figure 26. Simplified Automotive Infotainment Supply Schematic

Typical Applications (continued)

8.2.1.1 Design Requirements

Table 3 lists the design-goal parameters.

Table 3. Design-Goal Parameters

PARAMETER	V_{BuckA}	V_{BuckB}	BOOST
Input voltage	V_{IN} = 6 V to 30 V 12 V - typical	V_{IN} = 6 V to 30 V 12 V - typical	V_{BAT} = 5 V (cranking pulse input) to 30 V
Output voltage, V_{OUTx}	5 V	3.3 V	10 V
Maximum output current, I_{OUTx}	3 A	2 A	2.5 A
Load-step output tolerance, $\Delta V_{OUT} + \Delta V_{OUT(Ripple)}$	±0.2 V	±0.12 V	±0.5 V
Current output load step, ΔI_{OUTx}	0.1 A to 3 A	0.1 A to 2 A	0.1 A to 2.5 A
Converter switching frequency, f_{SW}	400 kHz	400 kHz	200 kHz

8.2.1.2 Detailed Design Procedure

Table 4 illustrates the design process and component selection for the TPS43335-Q1 and TPS43336-Q1.

Table 4. Automotive Infotainment Supply – Component Proposals

NAME	COMPONENT PROPOSAL	VALUE
L1	MSS1278T-392NL (Coilcraft)	4 µH
L2	MSS1278T-822ML (Coilcraft)	8.2 µH
L3	MSS1278T-153ML (Coilcraft)	15 µH
D1	SK103 (Micro Commercial Components)	
TOP_SW3	IRF7416 (International Rectifier)	
TOP_SW1, TOP_SW2	Si4840DY-T1-E3 (Vishay)	
BOT_SW1, BOT_SW2	Si4840DY-T1-E3 (Vishay)	
BOT_SW3	IRFR3504ZTRPBF (International Rectifier)	
C_{OUT1}	EEVFK1J681M (Panasonic)	680 µF
C_{OUTA}, C_{OUTB}	ECASD91A107M010K00 (Murata)	100 µF
C_{IN}	EEEFK1V331P (Panasonic)	220 µF

8.2.1.2.1 Boost Component Selection

A boost converter operating in continuous-conduction mode (CCM) has a right-half-plane (RHP) zero in its transfer function. The RHP zero relates inversely to the load current and inductor value and directly to the input voltage. The RHP zero limits the maximum bandwidth achievable for the boost regulator. If the bandwidth is too close to the RHP zero frequency, the regulator may become unstable.

Thus, for high-power systems with low input voltages, choose a low inductor value. A low value increases the amplitude of the ripple currents in the N-channel MOSFET, the inductor, and the capacitors for the boost regulator. Select these components with the ripple-to-RHP zero trade-off in mind and considering the power dissipation effects in the components due to parasitic series resistance.

A boost converter that operates always in the discontinuous mode does not contain the RHP zero in its transfer function. However, designing for the discontinuous mode demands an even lower inductor value that has high ripple currents. Also, ensure that the regulator never enters the continuous-conduction mode; otherwise, it may become unstable.

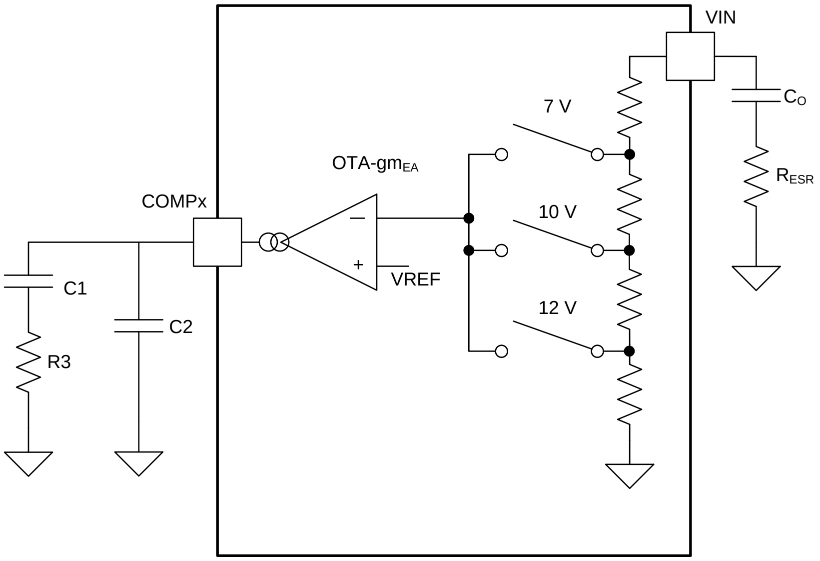


Figure 27. Boost Compensation Components

This design assumes operation in continuous-conduction mode. During light load conditions, the boost converter operates in discontinuous mode without affecting stability. Hence, the assumptions here cover the worst case for stability.

8.2.1.2.2 Boost Maximum Input Current I_{IN_MAX}

The maximum input current flows at the minimum input voltage and maximum load. The efficiency for V_{BAT} = 5 V at 2.5 A is 80%, based on the typical characteristics plot.

$$P_{INmax} = \frac{P_{OUT}}{Efficiency} = \frac{25\ W}{0.8} = 31.3\ W \tag{5}$$

Hence,

$$I_{INmax}(at\ V_{BAT} = 5\ V) = \frac{31.3\ W}{5\ V} = 6.3\ A \tag{6}$$

8.2.1.2.3 Boost Inductor Selection, L

Allow input ripple current of 40% of $I_{IN\ max}$ at V_{BAT} = 5 V.

$$L = \frac{V_{BAT} \times t_{ON}}{I_{INripple\,max}} = \frac{V_{BAT}}{I_{INripple\,max} \times 2 \times f_{SW}} = \frac{5\ V}{2.52\ A \times 2 \times 200\ kHz} = 4.9\ \mu H \tag{7}$$

Choose a lower value of 4 µH in order to ensure a high RHP-zero frequency while making a compromise that expects a high current ripple. This inductor selection also makes the boost converter operate in discontinuous conduction mode, where it is easier to compensate.

The inductor saturation current must be higher than the peak inductor current and some percentage higher than the maximum current-limit value set by the external resistive sensing element.

Determine the saturation rating at the minimum input voltage, maximum output current, and maximum core temperature for the application.

8.2.1.2.4 Inductor Ripple Current, I_{RIPPLE}

Based on an inductor value of 4 µH, the ripple current is approximately 3.1 A.

8.2.1.2.5 Peak Current in Low-Side FET, I_{PEAK}

$$I_{PEAK} = I_{INmax} + \frac{I_{RIPPLE}}{2} = 6.3\ A + \frac{3.1\ A}{2} = 7.85\ A \tag{8}$$

Based on this peak current value, calculate the external current-sense resistor R_{SENSE}.

$$R_{SENSE} = \frac{0.2\ V}{7.85\ A} = 25\ m\Omega \tag{9}$$

Select 20 mΩ, allowing for tolerance.

The filter component values R_{IFLT} and C_{IFLT} for current sense are 1.5 kΩ and 1 nF, respectively, which allows for good noise immunity.

8.2.1.2.6 Right Half-Plane Zero RHP Frequency, f_{RHP}

$$f_{RHP} = \frac{V_{BAT\,min}}{2\pi \times I_{INmax} \times L} = 32\ kHz \tag{10}$$

8.2.1.2.7 Output Capacitor, C_{OUTx}

To ensure stability, choose output capacitor C_{OUTx} such that

$$f_{LC} \le \frac{f_{RHP}}{10}$$

$$\frac{10}{2\pi \times \sqrt{L \times C_{OUTx}}} \le \frac{V_{BAT\,min}}{2\pi \times I_{INmax} \times L}$$

$$C_{OUTx} \ge \left(\frac{10 \times I_{INmax}}{V_{BAT\,min}}\right)^2 \times L = \left(\frac{10 \times 6.3\ A}{5\ V}\right)^2 \times 4\ \mu H$$

$$C_{OUTx\,min} \ge 635\ \mu F \tag{11}$$

Select C_{OUTx} = 680 µF.

This capacitor is usually aluminum electrolytic with ESR in the tens of milliohms. ESR in this range is good for loop stability, because it provides a phase boost. The output filter components, L and C, create a double pole (180-degree phase shift) at a frequency f_{LC} and the ESR of the output capacitor R_{ESR} creates a *zero* for the modulator at frequency f_{ESR}. These frequencies can be determined by the following:

$$f_{ESR} = \frac{1}{2\pi \times C_{OUTx} \times R_{ESR}} \text{Hz, assume } R_{ESR} = 40\ m\Omega$$

$$f_{ESR} = \frac{1}{2\pi \times 660\ \mu F \times 0.04\ \Omega} = 6\ kHz$$

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUTx}}} = \frac{1}{2\pi \times \sqrt{4\ \mu H \times 660\ \mu F}} = 3.1\ kHz \tag{12}$$

This satisfies $f_{LC} \le 0.1\ f_{RHP}$.

8.2.1.2.8 Bandwidth of Boost Converter, f_C

Use the following guidelines to set the frequency poles, zeroes, and crossover values for the trade-off between stability and transient response:

$f_{LC} < f_{ESR} < f_C < f_{RHP\ Zero}$

$f_C < f_{RHP\ Zero} / 3$

$f_C < f_{SW} / 6$

$f_{LC} < f_C / 3$

8.2.1.2.9 Output Ripple Voltage Due to Load Transients, ΔV_{OUTx}

Assume a bandwidth of f_C = 10 kHz.

$$\Delta V_{OUTx} = R_{ESR} \times \Delta I_{OUTx} + \frac{\Delta I_{OUTx}}{4 \times C_{OUTx} \times f_C}$$

$$= 0.04\ \Omega \times 2.5\ \text{A} + \frac{2.5\ \text{A}}{4 \times 660\ \mu\text{F} \times 10\ \text{kHz}} = 0.19\ \text{V} \tag{13}$$

Because the boost converter is active only during brief events such as a cranking pulse, and the buck converters are high-voltage tolerant, a higher excursion on the boost output may be tolerable in some cases. In such cases, one can choose smaller components for the boost output.

8.2.1.2.10 Selection of Components for Type II Compensation

The required loop gain for unity-gain bandwidth (UGB) is

$$G = 40\ \log\left(\frac{f_C}{f_{LC}}\right) - 20\ \log\left(\frac{f_C}{f_{ESR}}\right)$$

$$G = 40\ \log\left(\frac{10\ \text{kHz}}{3.1\ \text{kHz}}\right) - 20\ \log\left(\frac{10\ \text{kHz}}{6\ \text{kHz}}\right) = 15.9\ \text{dB} \tag{14}$$

The boost-converter error amplifier (OTA) has a Gm that is proportional to the VBAT voltage. This allows a constant loop response across the input-voltage range and makes it easier to compensate by removing the dependency on V_{BAT}.

$$R3 = \frac{10^{G/20}}{85 \times 10^{-6}\ \text{A} / \text{V}^2 \times V_{OUTx}} = 7.2\ \text{k}\Omega$$

$$C1 = \frac{10}{2\pi \times f_C \times R3} = \frac{10}{2\pi \times 10\ \text{kHz} \times 7.2\ \text{k}\Omega} = 22\ \text{nF}$$

$$C2 = \frac{C1}{2\pi \times R3 \times C1 \times \left(\frac{f_{SW}}{2}\right) - 1} = \frac{22\ \text{nF}}{2\pi \times 7.2\ \text{k}\Omega \times 22\ \text{nF} \times \left(\frac{200\ \text{kHz}}{2}\right) - 1} = 223\ \text{pF} \tag{15}$$

8.2.1.2.11 Input Capacitor, C_{IN}

The input ripple required is lower than 50 mV.

$$\Delta V_{C1} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{IN}} = 10\ \text{mV}$$

$$C_{IN} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times \Delta V_{C1}} = 194\ \mu\text{F}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR} = 40\ \text{mV} \tag{16}$$

Therefore, TI recommends 220 µF with 10-mΩ ESR.

8.2.1.2.12 Output Schottky Diode D1 Selection

Maximizing efficiency requires a Schottky diode with low forward-conducting voltage V_F over temperature and fast switching characteristics. The reverse breakdown voltage should be higher than the maximum input voltage, and the component should have low reverse leakage current. Additionally, the peak forward current should be higher than the peak inductor current. The power dissipation in the Schottky diode is given by:

$$P_D = I_{D(PEAK)} \times V_F \times (1 - D)$$

$$D = 1 - \frac{V_{INMIN}}{V_{OUT} + V_F} = 1 - \frac{5\ \text{V}}{10\ \text{V} + 0.6\ \text{V}} = 0.53$$

$$P_D = 7.85\ \text{A} \times 0.6\ \text{V} \times (1 - 0.53) = 2.2\ \text{W} \tag{17}$$

8.2.1.2.13 Low-Side MOSFET (BOT_SW3)

$$P_{BOOSTFET} = (I_{Pk})^2 \times r_{DS(on)}(1 + TC) \times D + \left(\frac{V_I \times I_{Pk}}{2}\right) \times (t_r + t_f) \times f_{SW}$$

$$P_{BOOSTFET} = (7.85\ \text{A})^2 \times 0.02\ \Omega \times (1 + 0.4) \times 0.53 + \left(\frac{V_I \times I_{Pk}}{2}\right) \times (20\ \text{ns} + 20\ \text{ns}) \times 200\ \text{kHz} = 1.07\ \text{W} \tag{18}$$

The times t_r and t_f denote the rising and falling times of the switching node and relate to the gate-driver strength of the TPS43335-Q1 and TPS43336-Q1 and the gate Miller capacitance of the MOSFET. The first term denotes the conduction losses, which the low on-resistance of the MOSFET minimizes. The second term denotes the transition losses which arise due to the full application of the input voltage across the drain-source of the MOSFET as it turns on or off. Transition losses are higher at high output currents and low input voltages (due to the large input peak current) and when the switching time is low.

Note: The on-resistance, $r_{DS(on)}$, has a positive temperature coefficient, which produces the (TC = d × ΔT) term that signifies the temperature dependence. (Temperature coefficient d is available as a normalized value from MOSFET data sheets and can have an assumed starting value of 0.005 / °C.)

8.2.1.2.14 BuckA Component Selection

8.2.1.2.14.1 BuckA Component Selection

$$t_{ON\,min} = \frac{V_{OUTA}}{V_{IN\,max} \times f_{SW}} = \frac{3.3\ \text{V}}{30\ \text{V} \times 400\ \text{kHz}} = 275\ \text{ns} \tag{19}$$

$t_{ON\ min}$is higher than the minimum duty cycle specified (100 ns typical). Hence, the minimum duty cycle is achievable at this frequency.

8.2.1.2.14.2 *Current-Sense Resistor R_{SENSE}*

Based on the typical characteristics for the V_{SENSE} limit with V_{IN} versus duty cycle, the sense limit is approximately 65 mV (at V_{IN} = 12 V and duty cycle of 5 V / 12 V = 0.416). Allowing for tolerances and ripple currents, choose a V_{SENSE} maximum of 50 mV.

$$R_{SENSE} = \frac{50\ \text{mV}}{3\ \text{A}} = 17\ \text{m}\Omega \tag{20}$$

Select 15 mΩ.

8.2.1.2.15 Inductor Selection L

As explained in the description of the buck controllers, for optimal slope compensation and loop response, choose the inductor such that:

$$L = K_{FLR} \times \frac{R_{SENSE}}{f_{SW}} = 200 \times \frac{15\ \text{m}\Omega}{400\ \text{kHz}} = 7.5\ \mu\text{H} \tag{21}$$

K_{FLR} = coil-selection constant = 200

Choose a standard value of 8.2 µH. For the buck converter, choose the inductor saturation currents and core to sustain the maximum currents.

8.2.1.2.16 Inductor Ripple Current I_{RIPPLE}

At the nominal input voltage of 12 V, this inductor value causes a ripple current of 30% of $I_{OUT\ max}$ ≈ 1 A.

8.2.1.2.17 Output Capacitor C_{OUTA}

Select an output capacitance C_{OUTA} of 100 µF with low ESR in the range of 10 mΩ, giving $\Delta V_{OUT(Ripple)}$ ≈ 15 mV and a ΔV drop of ≈ 180 mV during a load step, which does not trigger the power-good comparator and is within the required limits.

$$C_{OUTA} \approx \frac{2 \times \Delta I_{OUTA}}{f_{SW} \times \Delta V_{OUTA}} = \frac{2 \times 2.9\ \text{A}}{400\ \text{kHz} \times 0.2\ \text{V}} = 72.5\ \mu\text{F} \tag{22}$$

$$V_{OUTA(Ripple)} = \frac{I_{OUTA(Ripple)}}{8 \times f_{SW} \times C_{OUTA}} + I_{OUTA(Ripple)} \times ESR = \frac{1\ \text{A}}{8 \times 400\ \text{kHz} \times 100\ \mu\text{F}} + 1\ \text{A} \times 10\ \text{m}\Omega = 13.1\,\text{mV} \tag{23}$$

$$\Delta V_{OUTA} = \frac{\Delta I_{OUTA}}{4 \times f_C \times C_{OUTA}} + \Delta I_{OUTA} \times ESR = \frac{2.9\ \text{A}}{4 \times 50\ \text{kHz} \times 100\ \mu\text{F}} + 2.9\ \text{A} \times 10\ \text{m}\Omega = 174\ \text{mV} \tag{24}$$

8.2.1.2.18 Bandwidth of Buck Converter f_C

Use the following guidelines to set frequency poles, zeroes, and crossover values for the trade-off between stability and transient response.

- Crossover frequency f_C between f_{SW} / 6 and f_{SW} / 10. Assume f_C = 50 kHz.
- Select the zero $f_z \approx f_C / 10$
- Make the second pole $f_{P2} \approx f_{SW} / 2$

8.2.1.2.19 Selection of Components for Type II Compensation

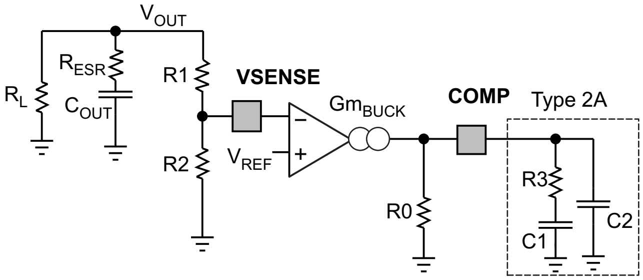


Figure 28. Buck Compensation Components

$$R3 = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUTx}}{Gm_{BUCK} \times K_{CFB} \times V_{REF}} = \frac{2\pi \times 50\ kHz \times 5\ V \times 100\mu F}{Gm_{BUCK} \times K_{CFB} \times V_{REF}} = 23.57\ k\Omega$$

where

- V_{OUT} = 5 V
- C_{OUT} = 100 µF
- Gm_{BUCK} = 1 mS
- V_{REF} = 0.8 V
- K_{CFB} = 0.125 / R_{SENSE} = 8.33 S (0.125 is an internal constant) (25)

Use the standard value of R3 = 24 kΩ.

$$C1 = \frac{10}{2\pi \times R3 \times f_C} = \frac{10}{2\pi \times 24\ k\Omega \times 50\ kHz} = 1.33\ nF \tag{26}$$

Use the standard value of 1.5 nF.

$$C2 = \frac{C1}{2\pi \times R3 \times C1\left(\frac{f_{SW}}{2}\right) - 1} = \frac{1.5\ nF}{2\pi \times 24 k\Omega \times 1.5\ nF\left(\frac{400\ kHz}{2}\right) - 1} = 33\ pF \tag{27}$$

The resulting bandwidth of buck converter f $_C$

$$f_C = \frac{Gm_{BUCK} \times R3 \times K_{CFB}}{2\pi \times C_{OUTx}} \times \frac{V_{REF}}{V_{OUT}}$$

$$f_C = \frac{1 mS \times 24\ k\Omega \times 8.33\ S \times 0.8\ V}{2\pi \times 100\ \mu F \times 5\ V} = 50.9\ kHz \tag{28}$$

f_C is close to the target bandwidth of 50 kHz.

The resulting zero frequency f_{Z1}

$$f_{Z1} = \frac{1}{2\pi \times R3 \times C1} = \frac{1}{2\pi \times 24\ k\Omega \times 1.5\ nF} = 4.42\ kHz \tag{29}$$

f_{Z1} is close to the f_C / 10 guideline of 5 kHz.

The second pole frequency f_{P2}

$$f_{P2} = \frac{1}{2\pi \times R3 \times C2} = \frac{1}{2\pi \times 24\ k\Omega \times 33\ pF} = 201\ kHz \tag{30}$$

f_{P2} is close to the f_{SW} / 2 guideline of 200 kHz. Hence, the design satisfies all requirements for a good loop.

8.2.1.2.20 Resistor Divider Selection for Setting V_{OUTA} Voltage

$$\beta = \frac{V_{REF}}{V_{OUTA}} = \frac{0.8\ V}{5\ V} = 0.16 \tag{31}$$

Choose the divider current through R1 and R2 to be 50 μA. Then

$$R1 + R2 = \frac{5\ V}{50\ \mu A} = 66\ k\Omega \tag{32}$$

and

$$\frac{R2}{R1 + R2} = 0.16 \tag{33}$$

Therefore, R2 = 16 kΩ and R1 = 84 kΩ.

8.2.1.2.21 BuckB Component Selection

Using the same method as for V_{BuckA} produces the following parameters and components.

$$t_{ON\,min} = \frac{V_{OUTB}}{V_{IN\,max} \times f_{SW}} = \frac{3.3\ V}{30\ V \times 400\ kHz} = 275\ ns \tag{34}$$

This is higher than the minimum duty cycle specified (100 ns typical).

$$\begin{aligned} R_{SENSE} &= \frac{60\ mV}{2\ A} = 30\ m\Omega \\ L &= 200 \times \frac{30\ m\Omega}{400\ kHz} = 15\ \mu H \end{aligned} \tag{35}$$

ΔI_{ripple} current ≈ 0.4 A (approximately 20% of $I_{OUT\ max}$)

Select an output capacitance C_{OUTB} of 100 µF with low ESR in the range of 10 mΩ.

Assume f_C = 50 kHz.

$$C_{OUTB} \approx \frac{2 \times \Delta I_{OUTB}}{f_{SW} \times \Delta V_{OUTB}} = \frac{2 \times 1.9\ A}{400\ kHz \times 0.12\ V} = 46\ \mu F \tag{36}$$

$$V_{OUTB(Ripple)} = \frac{I_{OUTB(Ripple)}}{8 \times f_{SW} \times C_{OUTB}} + I_{OUTB(Ripple)} \times ESR = \frac{0.4\ A}{8 \times 400\ kHz \times 100\ \mu F} + 0.4\ A \times 10\ m\Omega = 5.3\ mV \tag{37}$$

$$\Delta V_{OUTB} = \frac{\Delta I_{OUTB}}{4 \times f_C \times C_{OUTB}} + \Delta I_{OUTB} \times ESR = \frac{1.9\ A}{4 \times 50\ kHz \times 100\ \mu F} + 1.9\ A \times 10\ m\Omega = 114\ mV \tag{38}$$

$$\begin{aligned} R3 &= \frac{2\pi \times f_C \times V_{OUTB} \times C_{OUTB}}{Gm_{BUCK} \times K_{CFB} \times V_{REF}} \\ &= \frac{2\pi \times 50\ kHz \times 3.3\ V \times 100\ \mu F}{1\,mS \times 4.16\ S \times 0.8\ V} = 31\,k\Omega \end{aligned} \tag{39}$$

Use the standard value of R3 = 30 kΩ.

$$C1 = \frac{10}{2\pi \times R3 \times f_C} = \frac{10}{2\pi \times 30\ k\Omega \times 50\ kHz} = 1.1\,nF \tag{40}$$

$$C2 = \frac{C1}{2\pi \times R3 \times C1 \times \left(\frac{f_{SW}}{2}\right) - 1}$$

$$= \frac{1.1\,nF}{2\pi \times 30\ k\Omega \times 1.1\,nF \times \left(\frac{400\ kHz}{2}\right) - 1} = 27\ pF \tag{41}$$

$$f_C = \frac{Gm_{BUCK} \times R3 \times K_{CFB}}{2\pi \times C_{OUTB}} \times \frac{V_{REF}}{V_{OUTB}}$$

$$= \frac{1\,mS \times 30\ k\Omega \times 4.16\ S \times 0.8\ V}{2\pi \times 100\ \mu F \times 3.3\ V} = 48\ kHz \tag{42}$$

f_C is close to the target bandwidth of 50 kHz.

The resulting zero frequency f_{Z1}

$$f_{Z1} = \frac{1}{2\pi \times R3 \times C1} = \frac{1}{2\pi \times 30\ k\Omega \times 1.1\,nF} = 4.8\ kHz \tag{43}$$

f_{Z1} is close to the f_C guideline of 5 kHz.

The second pole frequency f_{P2}

$$f_{P2} = \frac{1}{2\pi \times R3 \times C2} = \frac{1}{2\pi \times 30\ k\Omega \times 27\ pF} = 196\ kHz \tag{44}$$

f_{P2} is close to the f_{SW} / 2 guideline of 200 kHz.

Hence, the design satisfies all requirements for a good loop.

8.2.1.2.22 Resistor Divider Selection for Setting V_{OUT} Voltage

$$\beta = \frac{V_{REF}}{V_{OUT}} = \frac{0.8\ V}{3.3\ V} = 0.242 \tag{45}$$

Choose the divider current through R1 and R2 to be 50 µA. Then

$$R1 + R2 = \frac{3.3\ V}{50\ \mu A} = 66\ k\Omega \tag{46}$$

and

$$\frac{R2}{R1 + R2} = 0.242 \tag{47}$$

Therefore, R2 = 16 kΩ and R1 = 50 kΩ.

8.2.1.2.23 BuckX High-Side and Low-Side N-Channel MOSFETs

An internal supply, which is 5.8 V typical under normal operating conditions, provides the gate-drive supply for these MOSFETs. The output is a totem pole, allowing full-voltage drive of V_{REG} to the gate with peak output current of 0.7 A. The reference for the high-side MOSFET is a floating node at the phase terminal (PHx), and the reference for the low-side MOSFET is the power-ground (PGx) terminal. For a particular application, select these MOSFETs with consideration for the following parameters: $r_{DS(on)}$, gate charge Qg, drain-to-source breakdown voltage BVDSS, maximum dc current IDC(max), and thermal resistance for the package.

The times $t_r$and t_f denote the rising and falling times of the switching node and have a relationship to the gate-driver strength of the TPS43335-Q1 and TPS43336-Q1 and to the gate Miller capacitance of the MOSFET. The first term denotes the conduction losses, which are minimimal when the on-resistance of the MOSFET is low. The second term denotes the transition losses, which arise due to the full application of the input voltage across the drain-source of the MOSFET as it turns on or off. Transition losses are lower at low currents and when the switching time is low.

$$P_{BuckTOPFET} = (I_{OUT})^2 \times r_{DS(on)}(1+TC) \times D + \left(\frac{V_{IN} \times I_{OUT}}{2}\right) \times (t_r + t_f) \times f_{SW} \tag{48}$$

$$P_{BuckLOWERFET} = (I_{OUT})^2 \times r_{DS(on)}(1+TC) \times (1-D) + V_F \times I_{OUT} \times (2 \times t_d) \times f_{SW} \tag{49}$$

In addition, during the dead time t_d when both the MOSFETs are off, the body diode of the low-side MOSFET conducts, increasing the losses. The second term in the preceding equation denotes this. Using external Schottky diodes in parallel with the low-side MOSFETs of the buck converters helps to reduce this loss.

Note: $r_{DS(on)}$ has a positive temperature coefficient, and TC term for $r_{DS(on)}$ accounts for that fact. TC = d × ΔT[°C]. The temperature coefficient d is available as a normalized value from MOSFET data sheets and can have an assumed starting value of 0.005 / ºC.

8.2.1.3 Application Curves

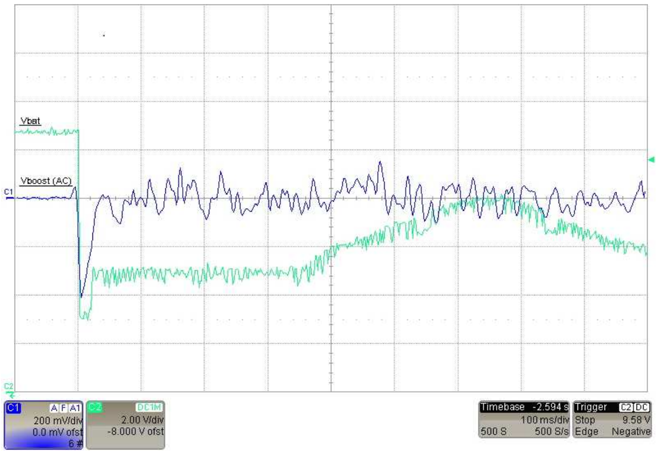


Figure 29. Boost Cranking Pulse Response with 2 A Load on Boost

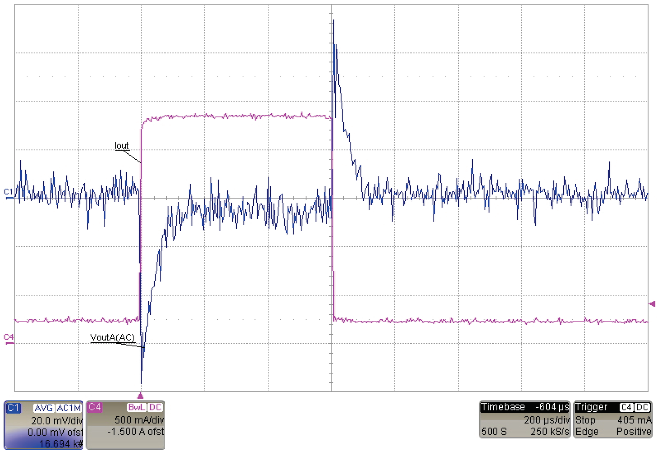


Figure 30. Buck Load-Step Response: BuckA 5 V, 200 mA to 2.4 A to 200 mA

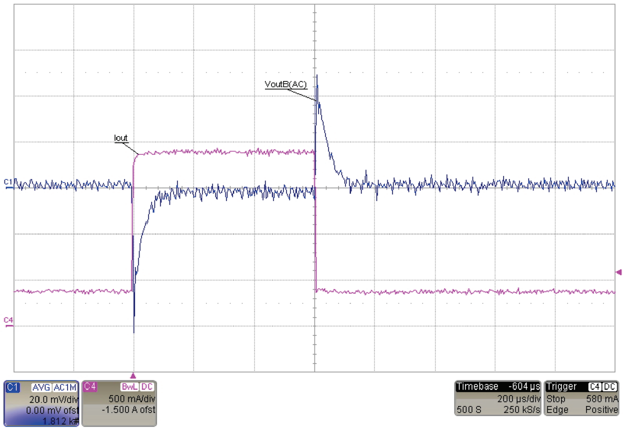


Figure 31. Buck Load-Step Response: BuckB 3.3 V, 400 mA to 1.8 A to 400 mA

8.2.2 Automotive ADAS Supply

The following example shows an application with lower output voltage and reduced load on BuckB (2.5 V, 1 A)

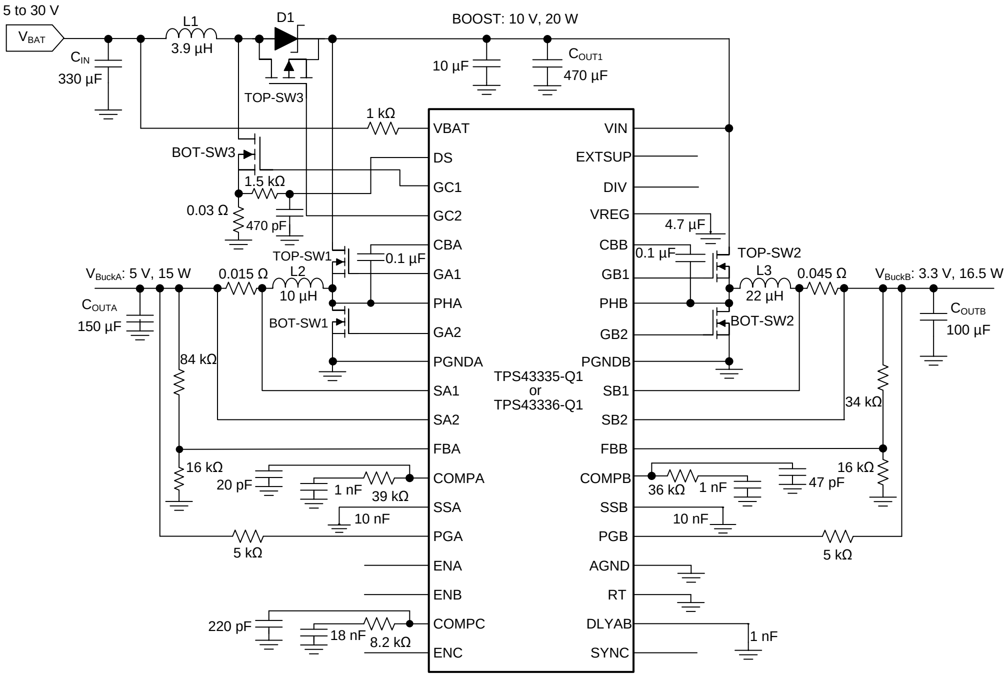


Figure 32. Simplified Automotive ADAS Supply Schematic

8.2.2.1 Design Requirements

Table 5 lists the design-goal parameters.

Table 5. Design-Goal Parameters

PARAMETER	V_{BuckA}	V_{BuckB}	BOOST
Input voltage	V_{IN} = 5 V to 30 V 12 V - typical	V_{IN} = 6 V to 30 V 12 V - typical	V_{BAT} = 5 V (cranking pulse input) to 30 V
Output voltage, V_{OUTx}	5 V	2.5 V	10 V
Maximum output current, I_{OUTx}	3 A	1 A	2 A
Load-step output tolerance, $\Delta V_{OUT} + \Delta V_{OUT(Ripple)}$	±0.2 V	±0.12 V	±0.5 V
Current output load step, ΔI_{OUTx}	0.1 A to 3 A	0.1 A to 1 A	0.1 A to 2 A
Converter switching frequency, f_{SW}	400 kHz	400 kHz	200 kHz

8.2.2.2 Detailed Design Procedure

Table 6 illustrates the design process and component selection for the TPS43335-Q1 and TPS43336-Q1.

Table 6. Automotive ADAS Supply – Component Proposals

NAME	COMPONENT PROPOSAL	VALUE
L1	MSS1278T-392NL (Coilcraft)	3.9 µH
L2	MSS1278T-822ML (Coilcraft)	8.2 µH
L3	MSS1278T-223ML (Coilcraft)	22 µH
D1	SK103 (Micro Commercial Components)	
TOP_SW3	IRF7416 (International Rectifier)	
TOP_SW1, TOP_SW2	Si4840DY-T1-E3 (Vishay)	
BOT_SW1, BOT_SW2	Si4840DY-T1-E3 (Vishay)	
BOT_SW3	IRFR3504ZTRPBF (International Rectifier)	
C_{OUT1}	EEVFK1V471Q (Panasonic)	470 µF
C_{OUTA}	ECASD91A157M010K00 (Murata)	150 µF
C_{OUTB}	ECASD40J107M015K00 (Murata)	100 µF
C_{IN}	EEEFK1V331P (Panasonic)	330 µF

9 Power Supply Recommendations

The TPS43335-Q1 and TPS43336-Q1 devices are designed to operate from an input voltage up to 40 V. Ensure that the input supply is well regulated. Furthermore, if the supply voltage in the application is likely to reach negative voltage (for example, reverse battery) a forward diode must be placed at the input of the supply. For the VIN pin, a good quality X7R ceramic capacitor is recommended. Capacitance derating for aging, temperature, and DC bias must be taken into account while determining the capacitor value. Connect a local decoupling capacitor close to the Vreg for proper filtering. The PowerPAD™ package, which offers an exposed thermal pad to enhance thermal performance, must be soldered to the copper landing on the PCB for optimal performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Grounding and PCB Circuit Layout Considerations

10.1.1.1 Boost converter

1. The path formed from the input capacitor to the inductor and BOT_SW3 with the low-side current-sense resistor should have short leads and PC trace lengths. The same applies for the trace from the inductor to Schottky diode D1 to the C_{OUT1} capacitor. Connect the negative terminal of the input capacitor and the negative terminal of the sense resistor together with short trace lengths.
2. The overcurrent-sensing shunt resistor may require noise filtering, and the filter capacitor should be close to the IC pin.

10.1.1.2 Buck Converter

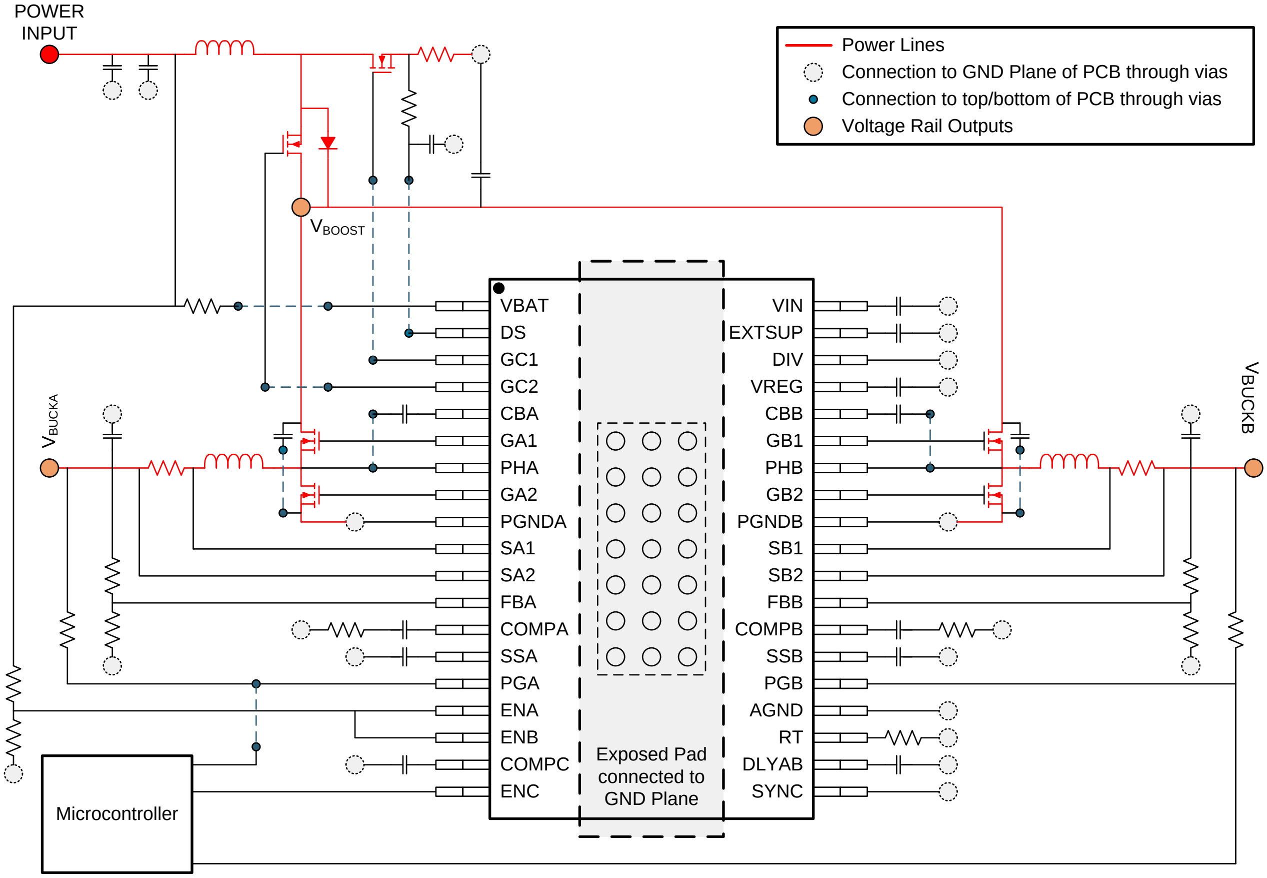
1. Connect the drain of TOP_SW1 and TOP_SW2 together with the positive terminal of input capacitor C_{OUT1}. The trace length between these terminals should be short.
2. Connect a local decoupling capacitor between the drain of TOP_SWx and the source of BOT_SWx.
3. The Kelvin-current sensing for the shunt resistor should have traces with minimum spacing, routed in parallel with each other. Place any filtering capacitors for noise near the IC pins.
4. The resistor divider for sensing the output voltage connects between the positive terminal of its respective output capacitor and C_{OUTA} or C_{OUTB} and the IC signal ground. Do not locate these components and their traces near any switching nodes or high-current traces.

Layout Guidelines (continued)

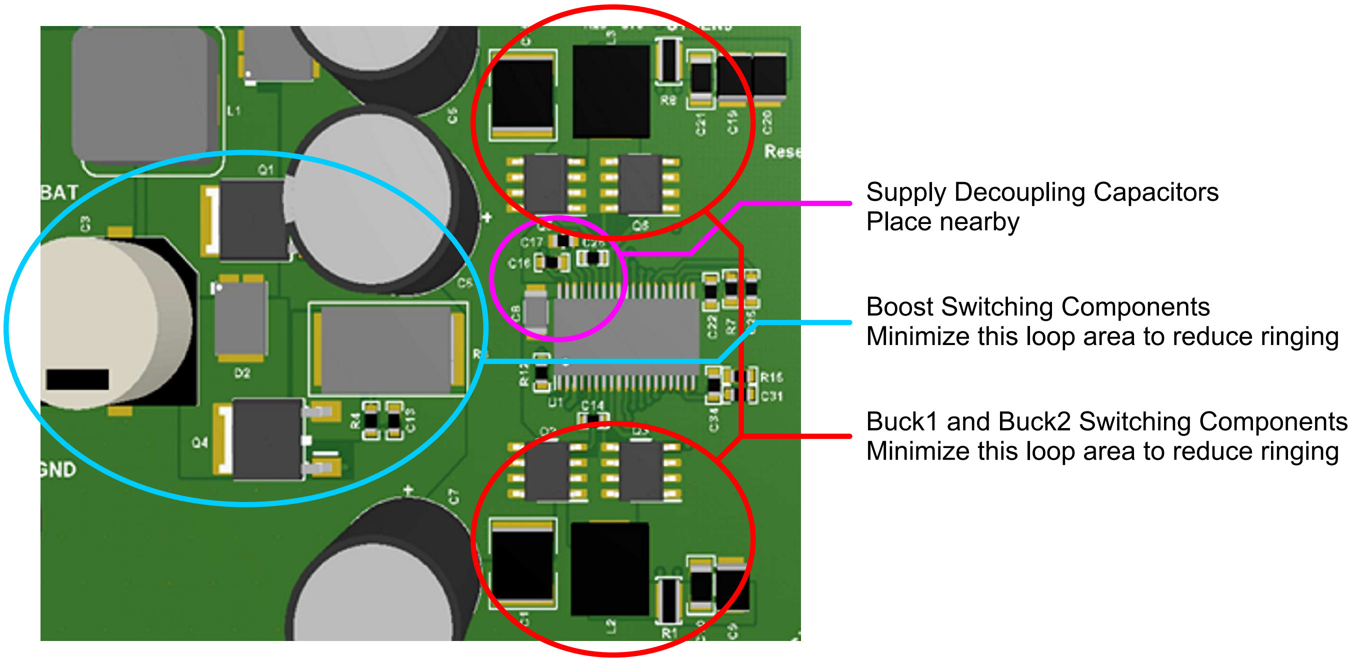
10.1.2 Other Considerations

1. Short PGNDx and AGND to the thermal pad. Use a star ground configuration if connecting to a non-ground plane system. Use tie-ins for the EXTSUP capacitor, compensation-network ground, and voltage-sense feedback ground networks to this star ground.
2. Connect a compensation network between the compensation pins and IC signal ground. Connect the oscillator resistor (frequency setting) between the RT pin and IC signal ground. Do not locate these sensitive circuits near the dv/dt nodes; these include the gate-drive outputs, phase pins, and boost circuits (bootstrap).
3. Reduce the surface area of the high-current-carrying loops to a minimum by ensuring optimal component placement. Locate the bypass capacitors as close as possible to their respective power and ground pins.

10.2 Layout Example



Layout Example (continued)



Supply Decoupling Capacitors
Place nearby

Boost Switching Components
Minimize this loop area to reduce ringing

Buck1 and Buck2 Switching Components
Minimize this loop area to reduce ringing

10.3 Power Dissipation Derating Profile, 38-Pin HTTSOP PowerPAD Package

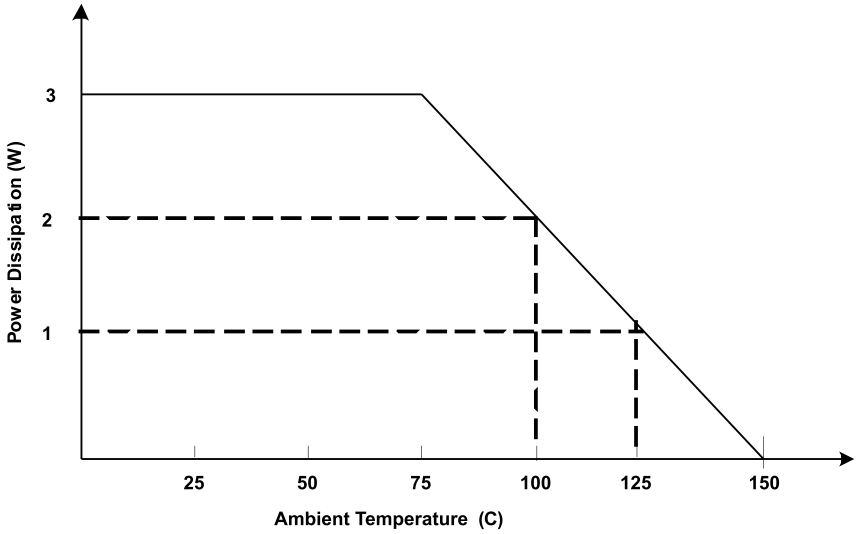


Figure 33. Derating Profile for Power Dissipation Based on High-K JEDEC PCB

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

TPS4333xEVM, SLVU457

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS43335-Q1	Click here	Click here	Click here	Click here	Click here
TPS43336-Q1	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS43335QDAPRQ1	ACTIVE	HTSSOP	DAP	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS43335Q1	Samples
TPS43336QDAPRQ1	ACTIVE	HTSSOP	DAP	38	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS43336Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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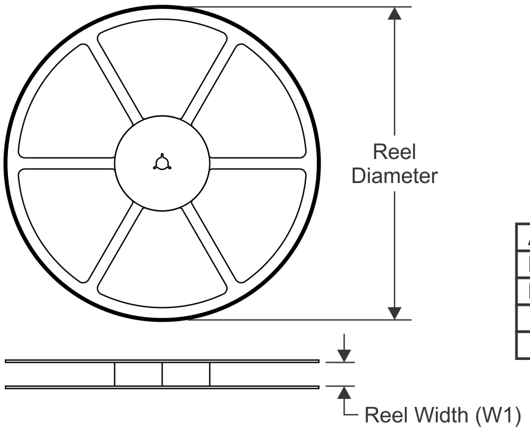
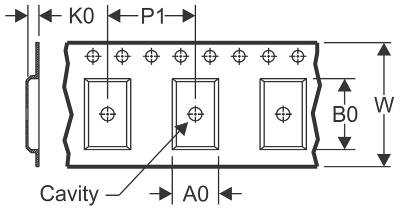
TAPE AND REEL INFORMATION

REEL DIMENSIONS

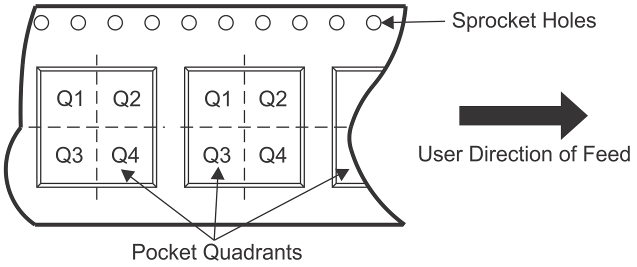


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

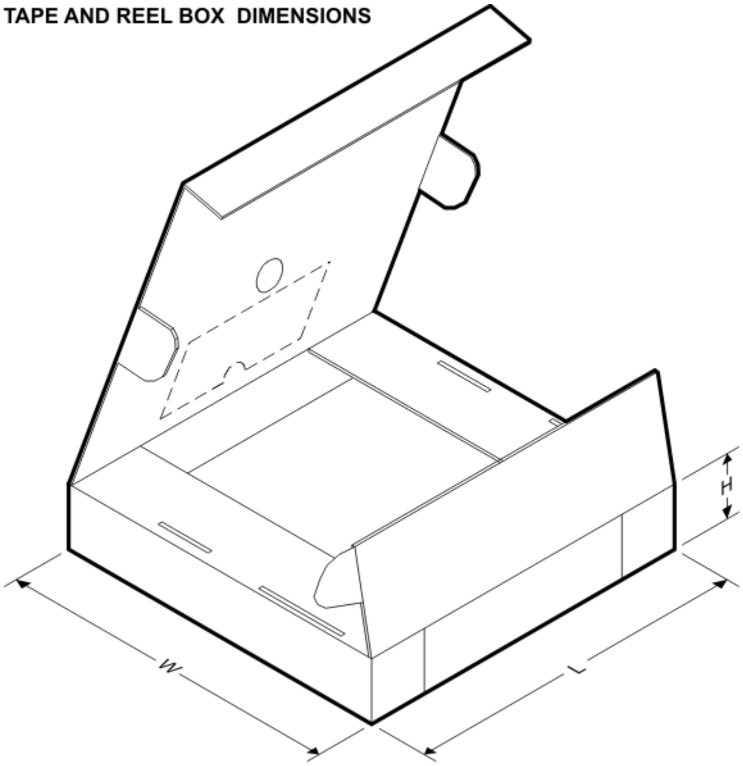
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS43335QDAPRQ1	HTSSOP	DAP	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
TPS43336QDAPRQ1	HTSSOP	DAP	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

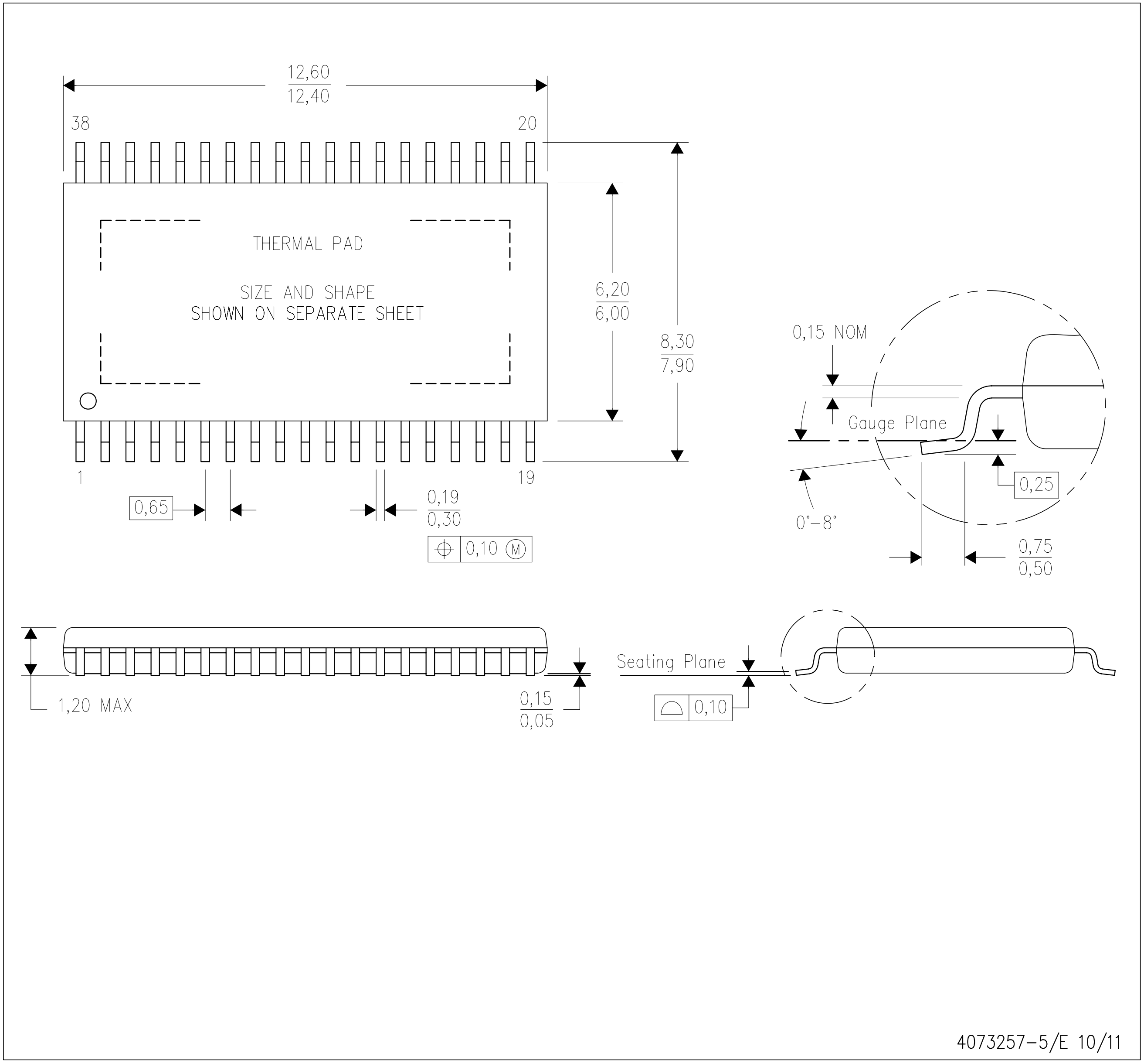
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS43335QDAPRQ1	HTSSOP	DAP	38	2000	350.0	350.0	43.0
TPS43336QDAPRQ1	HTSSOP	DAP	38	2000	350.0	350.0	43.0

DAP (R–PDSO–G38) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F Falls within JEDEC MO–153 Variation DDT–1.

PowerPAD is a trademark of Texas Instruments.

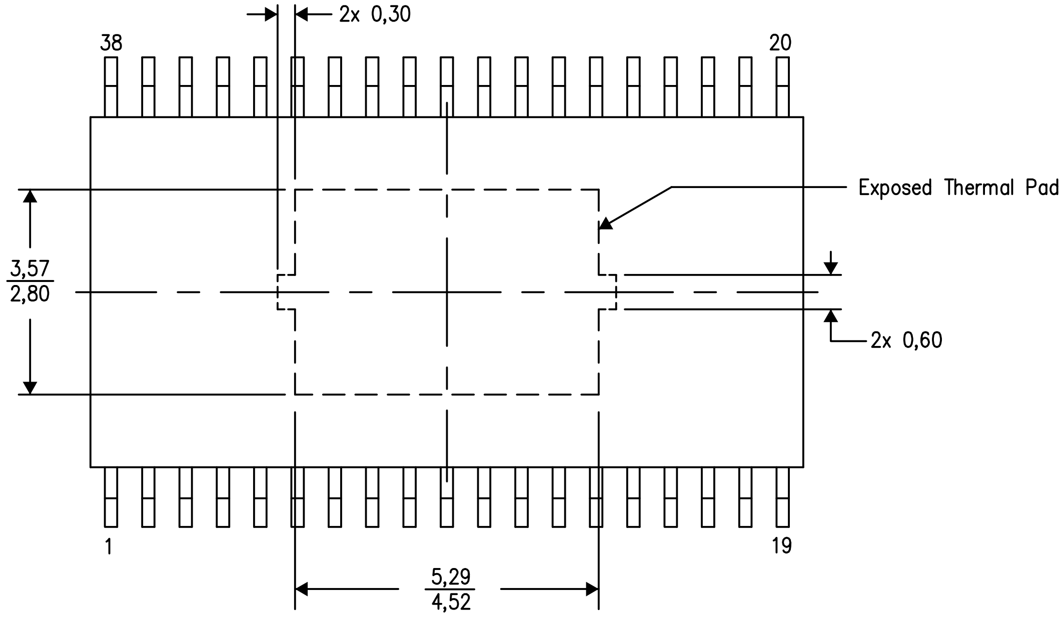
DAP (R-PDSO-G38) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

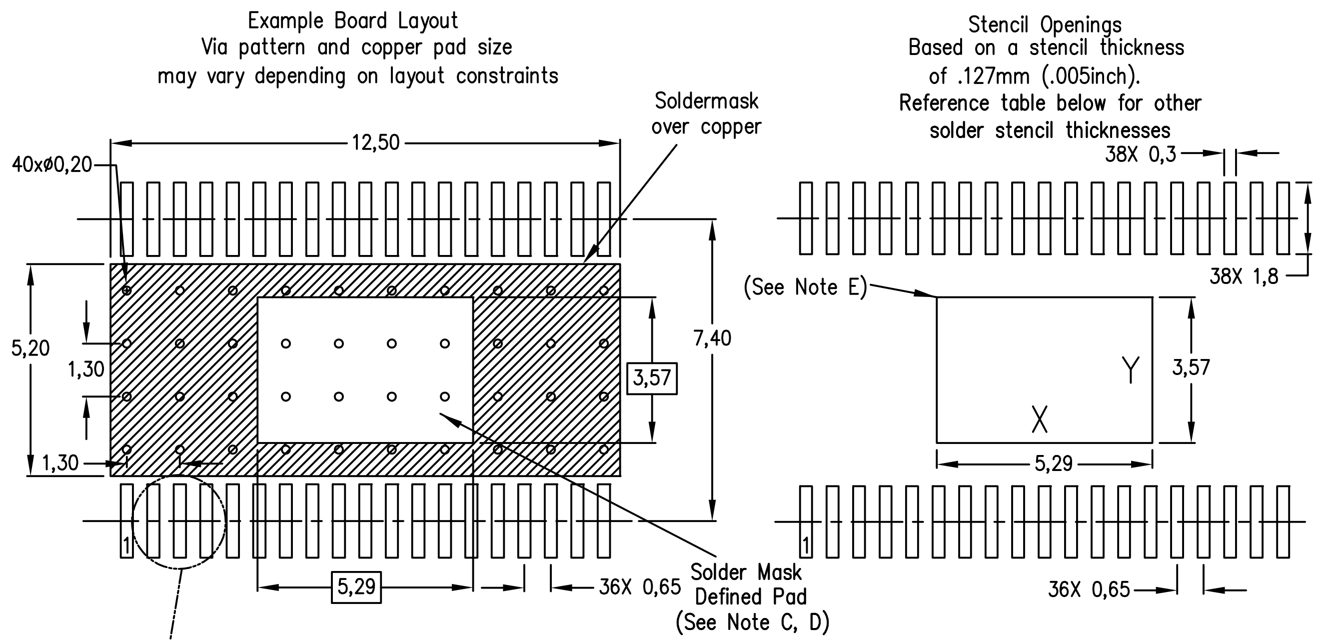
Exposed Thermal Pad Dimensions

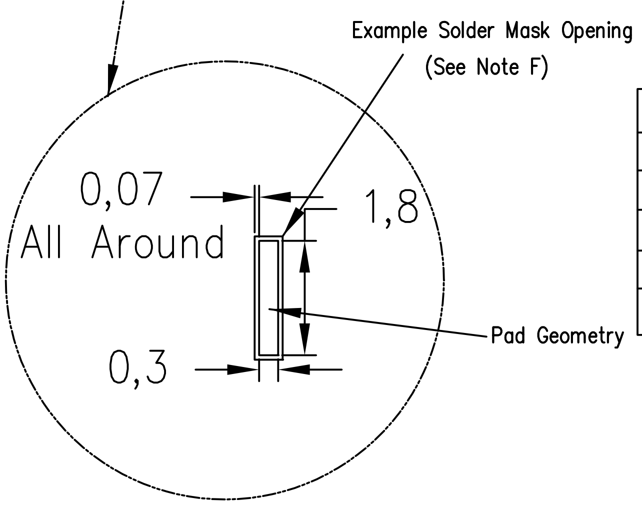
4206319-9/M 09/13

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

DAP (R–PDSO–G38) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5,96	4.02
0.127mm	5,29	3,57
0.152mm	4.84	3.26
0.178mm	4.47	3.02

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- F. Contact the board fabrication site for recommended soldermask tolerances.

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