Application Note:

HFAN-06.1

Rev 1, 11/07

Input/Output Models for Maxim Fiber Components

Maxim High-Frequency/Fiber Communications Group

maxim integrated™

Input/Output Models for Maxim Fiber Components

1 Abstract

The objective of this note is to discuss the use of input and output models for Maxim fiber parts. This is accomplished utilizing the MAX3801 *adaptive equalizer.*

2 Introduction

When a customer uses a Maxim Fiber component in a prototype, it is easily determined whether the component meets the functional requirements of that system. Prototyping also confirms whether this sample of the Maxim part performs at the data rate required by the system. However the question remains as to whether the system will still function when parts, components and boards are assembled in production to make many systems.

Most fiber communication systems are made of many integrated circuits, passive components such as resistors, capacitors and inductors and the PC board. All of these components affect the system performance. For example, the shape and speed of high speed data signals leaving one part and being delivered to another part on a PC board are determined by the rise and fall time of the part, the impedance of its output stage, the bond wire length, the component package, the series capacitance, the impedance of the transmission line, and the input impedance of the next stage. Thus it is difficult to determine exactly what will happen to signals connected from one IC to another IC in a system by prototyping alone. Simulation is required.

3 Definitions, Conventions, and Assumptions

Most fiber integrated circuits from Maxim use Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) I/O formats. Models are provided for all these input/output (I/O) formats, however this application note will focus on CML.

Fiber I/O models are provided on the Maxim webpage as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. The models are contained as subcircuits. Since the original SPICE simulator does not accept alphabetic characters for node labels, specific node numbers are used for common nodes such as signal inputs, outputs and power supply. For example, the positive signal (IN+) to a part is called node 2101 in the SPICE netlist. Table 1 describes the convention for common signals.

Table 1. Conventions for Parameters and Variables

Schematic Node Name	Description	Netlist Node Number
VCC	Power Supply (3.3V typ.)	101
GND	Ground (0.0 Volts)	0, 21
IN+	Positive Input Signal	2101
IN-	Negative Input Signal	2102
OUT+	Positive Output Signal	2001
OUT-	Negative Output Signal	2002

The models discussed in this article describe the input and output stages of the Maxim part only. The input/output model does not provide functional or behavioral information. The models provided include the effects of I/O transistors, the ESD devices, and the bond wire and package capacitances. They are nominal models at room temperature. Variation of the characteristics of the signals with changes in process is not modeled.

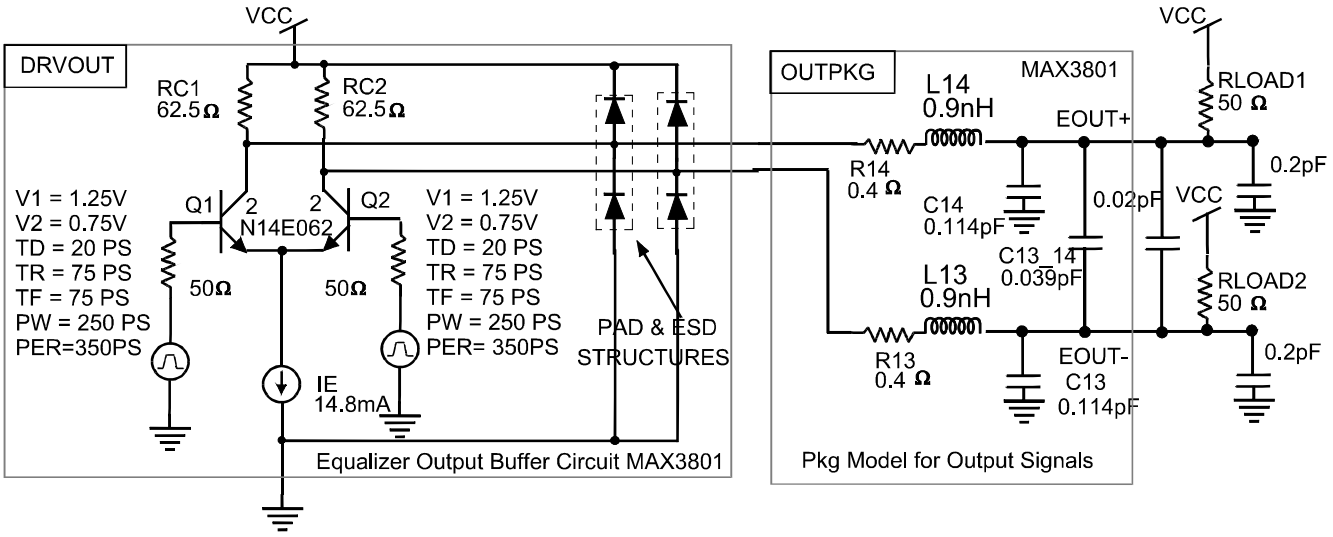

Figure 1. Equalizer output stage for the MAX3801 including a simplified package model.

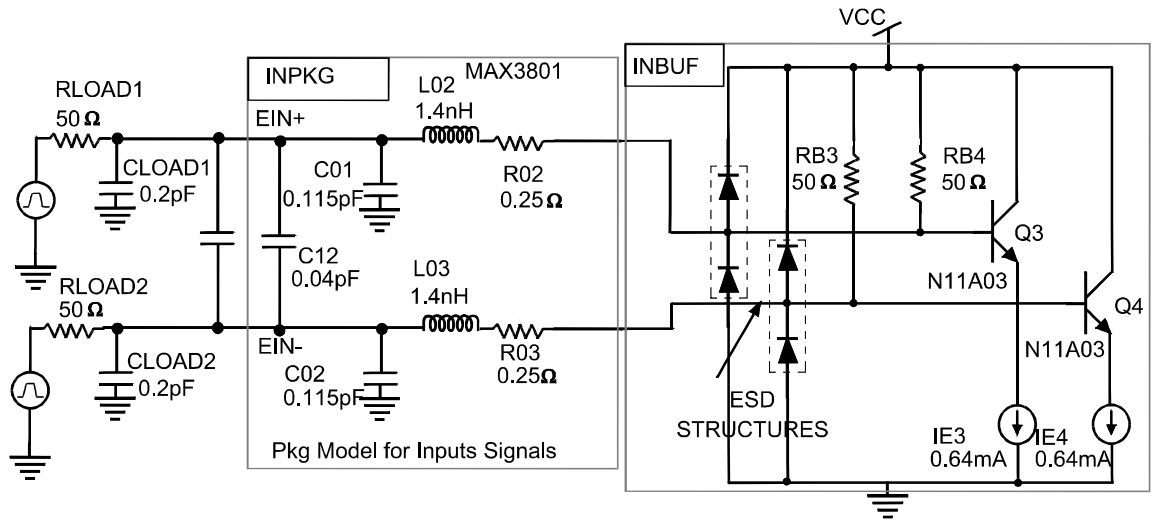

Figure 2. Simplified input package model and input circuitry for the MAX3801 equalizer.

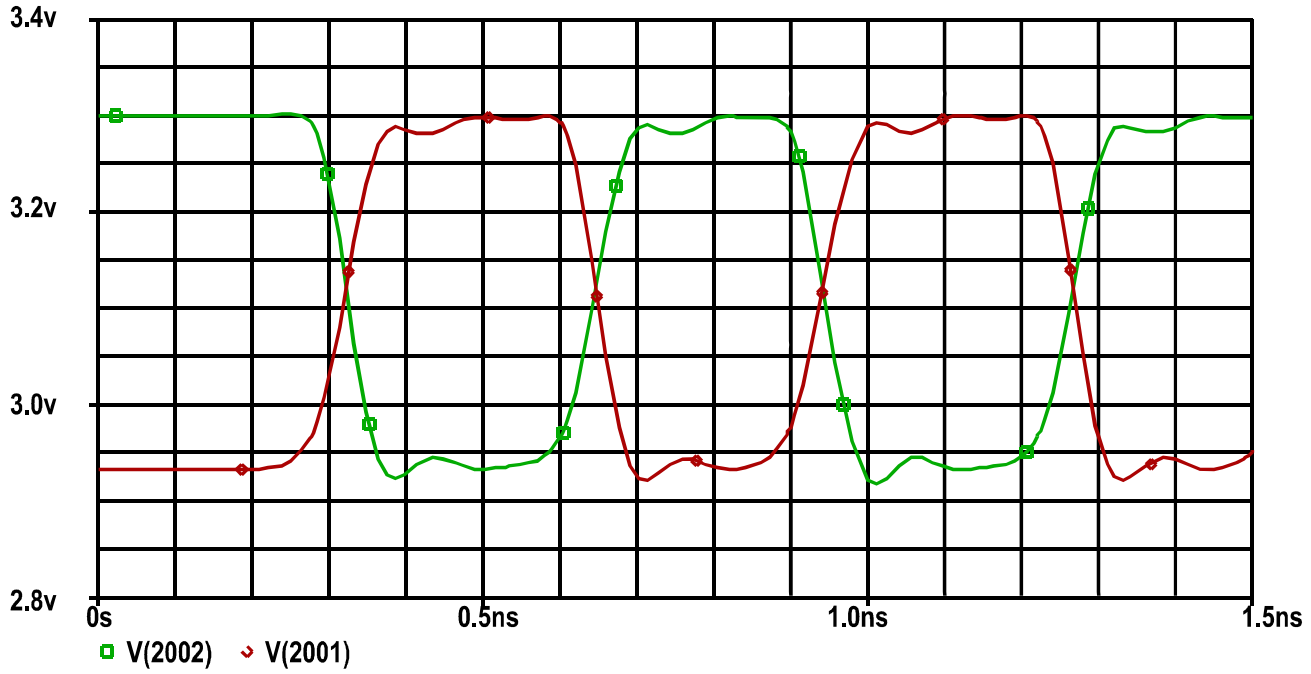

Figure 3. PSPICE simulation waveform showing the response of the output driver. Levels and rise times with the data sheet. Note as per Table 1, the waveforms are labeled V(2001), V(2002) for V(EOUT+) and V(EOUT-)

4 The Output Buffer

The output stage of the MAX3801 equalizer is shown in Figure 1. It is comprised of an output buffer subcircuit named DRVOUT. The subcircuit describing the package parasitic and the bond wires is named OUTPKG. The simulation SPICE netlist given in the appendix has both subcircuits plus a load for simulation.

The DRVOUT subcircuit represents the actual circuitry of the last stage. Signals from the internal circuitry are represented by two pulse sources driving output transistors Q1 and Q2 through 50Ω resistances. Transistors Q1 and Q2 called N14E062 make up the differential stage. Their emitters are biased by a 14.8 mA current source. The collectors of Q1 and Q2 are connected to the die pad and electrostatic protection devices (ESD diodes). The pad subcircuit is modeled by a 0.05pF capacitor and includes models for the ESD diodes.

Figure 3 shows the PSPICE simulation results of the output buffer driving 50 Ohm resistors in parallel with 0.2pF capacitors. The output loads at nodes EOUT+ and EOUT- are shown in Figure 1 and consist of 50 Ohm loads in parallel with 0.2pF capacitors. Also there is a 0.05pF capacitor between the two outputs. Note the labels for the outputs EOUT+ and EOUT- are 2001 and 2002.

In the package subcircuit OUTPKG shown in Figure 1, the path of each signal is modeled by series resistances R13, R14, inductances L13, L14 and capacitances to ground C13, C14. This subcircuit includes the coupling capacitance C13-14 between the capacitors C13 and C14.

For some models of Maxim Fiber components, the complete model of the package is given including all mutual inductances and coupling capacitors. For this subcircuit model, all unused terminals are connected to ground or the power supply V_{CC}.

5 The Input Buffer

The model for the input buffer is shown in Figure 2. It consists of a package subcircuit called INPKG and an input buffer subcircuit called INBUF. The simulation SPICE netlist has both subcircuits plus pulse generators and resistors to emulate signal input.

As seen in Figure 2, input signals to the model have been emulated by two pulse sources in series with series 50Ω resistors and 0.2pF shunt capacitors tied to ground. The signal passes through a Capacitance–Inductance–Resistance network. The the input signal lines are then connected to a pad and two ESD diodes, two 50Ω termination resistors and two input NPN transistors, Q3 and Q4.

Figure 4 shows the waveforms seen at the input of the part as well as the bases of transistors Q3 and Q4. The response at the input of the part represents how the part reacts to a signal from a 50 Ω source such as a transmission line. The termination resistors and package components such as the bond wire and package capacitance largely determine this response. The signals at the bases are labeled V(8) and V(9).

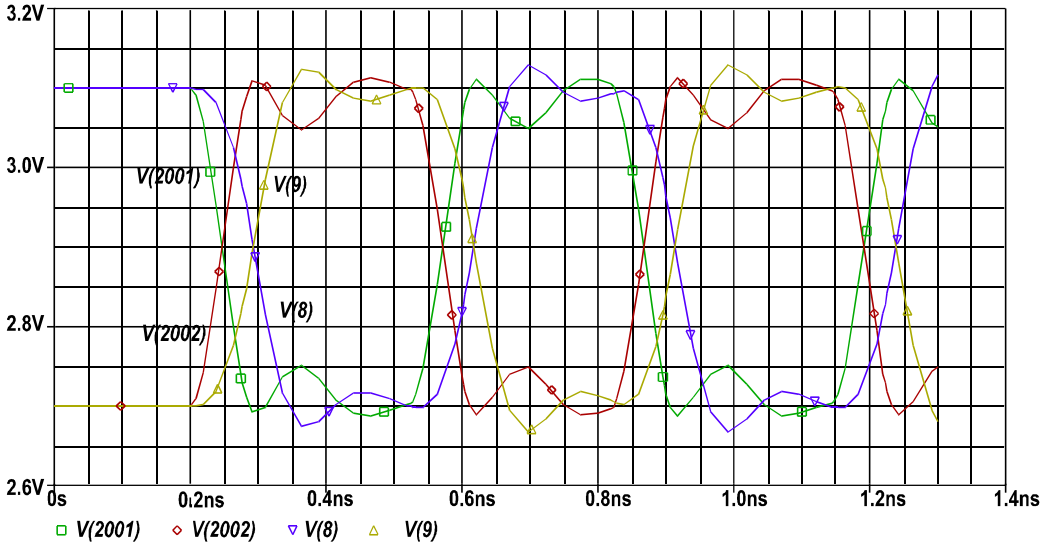

Figure 4. PSPICE simulation waveforms at the input to the MAX3801 Input model.

6 Document Format

The documentation for each model in the library comes with a schematic page, a notes page and a simulation netlist.

The schematic page gives both the input and output circuitry.

The notes page discusses assumptions, simplifications and additions which the modeler used to generate the input/output model. For example the MAX3640 has LVDS output logic levels. The model notes page for this part discusses how a the output signal level was set with a common mode voltage of 1.2V. This simplification doesn't reflect the actual device but is quite acceptable for signal integrity.

The netlist gives simulation files for both the input and output structure of the part. It is in a generic SPICE format and is suitable for PSPICE, HPSPICE and all other SPICE compatible simulators. Models for transistors, pads, ESD diodes, etc are given as subcircuits. Users can modify the netlist for their own applications.

7 Appendix

7.1 Output Netlist

```
INPUT -  MAX3801 EQUALIZER OUTPUT CIRCUIT
*
* THIS IS THE TYPICAL CML OUTPUT OF THE MAX#3801
*
.OPTIONS ACCT NOMOD NOPAGE LIMPTS=10000 RELTOL=.001
.WIDTH OUT=80
.TEMP 80
* TYPICAL DIE TEMP = 25C + 2.2W*(26C/W) = 80C
.OP
.TRAN 5PS 1500PS
*
* CONVENTIONS VCC = 101, VEE = 102, + OUT = 2000, - OUT = 2002
*
VCC 101 0 DC 3.3
RLOAD1 2001 101 50
RLOAD2 2002 101 50
CLOAD1 2001 101 0.20P
CLOAD2 2002 101 0.20P
CLOAD3 2001 2002 0.05P
XPK1 2001 2002 4 5 0 0 0 OUTPKG
XCIROUT 4 5 101 OUTDRV
*
.SUBCKT OUTDRV 1001 1002 101
VINP 2 0 PULSE (1.25 0.95 0.2N 0.075N 0.075N 0.250N 0.620N)
VINN 3 0 PULSE (0.95 1.25 0.2N 0.075N 0.075N 0.250N 0.620N)
*
RB1 2 22 50
RB2 3 32 50
*
XQ1 1001 22 61 0 N14E062
XQ2 1002 32 62 0 N14E062
*
RC1 1001 101 50



RC2 1002 101 50
*
IB1 61 0 7.4M
IB2 62 0 7.4M
RC3 61 62 0.1
*
XPAD1 1001 101 0 0 PADESD100
XPAD2 1002 101 0 0 PADESD100
*
.ENDS OUTDRV
*
.SUBCKT OUTPKG 101 102 201 202 401 402 403
*
* resistors
*
R14 201 301 400M
R13 202 302 402M
*
* inductors
*
L14 101 301 0.9N
L13 102 302 0.9N
*
```

```
* capacitors
*
C13 101 403 114F
C14 102 403 114F
*
* mutual capacitors
*
C13_14 101 102 39F
.ENDS OUTPKG
*
** BEGINNING OF PROCESS LIB
*
.SUBCKT N11A03 1 2 3 21
CP1EPI 10 12 3.539F
CP1P2 12 3 2.985F
CTRENCH 1 20 6.455F
RBX 2 12 118.779 TC=2.556M
RCX 1 10 58.217 TC=2.576M,499.699N
RCI 10 11 14.554 TC=2.576M,499.699N
REX 13 3 18.075 TC=192.895U
RSUB 20 21 16.621K
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
.MODEL TX NPN( IS=6.897E-018 XTI=3 EG=1.155 BF=331.407 BR=36 XTB=0
+   VAF=100 VAR=2 NF=1.018 NR=1.018 NE=2 NC=1.560 IKF=22.765M
+   IKR=556.875U ISE=4.455E-016 ISC=2.005E-030 RB=29.695 RBM=22.271
+   IRB=2.005M CJE=10.919F MJE=463M VJE=1.040 FC=990M CJC=7.144F
+   MJC=400M VJC=890M TF=2.631P TR=19N XTF=100 VTF=5 ITF=65.510M PTF=5
+   KF=9.000E-016 AF=1.500 )
.MODEL TXP PNP( IS=5.724E-020 CJE=7.216E-017 MJE=400M VJE=890M
+   CJC=5.346F MJC=460M VJC=790M BF=10K BR=55.381M TF=1N FC=900M )
.ENDS N11A03

.SUBCKT N12A04 1 2 3 21
CP1EPI 10 12 8.626F
CP1P2 12 3 7.236F
CTRENCH 1 20 9.222F
RBX 2 12 36.927 TC=2.542M
RCX 1 10 37.004 TC=2.053M,235.845N
RCI 10 11 9.251 TC=2.053M,235.845N
REX 13 3 6.092 TC=303.554U
RSUB 20 21 10.427K
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
.MODEL TX NPN( IS=2.299E-017 XTI=3 EG=1.155 BF=315.986 BR=36 XTB=0
+   VAF=100 VAR=2 NF=1.018 NR=1.018 NE=2 NC=1.560 IKF=75.884M IKR=1.856M
+   ISE=1.485F ISC=6.683E-030 RB=9.232 RBM=6.924 IRB=6.683M CJE=36.362F
+   MJE=463M VJE=1.040 FC=990M CJC=21.321F MJC=400M VJC=890M TF=2.668P
+   TR=19N XTF=100 VTF=5 ITF=215.178M PTF=5 KF=9.000E-016 AF=1.500 )
.MODEL TXP PNP( IS=1.728E-019 CJE=2.154E-016 MJE=400M VJE=890M
+   CJC=11.360F MJC=460M VJC=790M BF=10K BR=78.677M TF=1N FC=900M )
.ENDS N12A04

.SUBCKT N14E062 1 2 3 21
CP1EPI 10 12 54.836F
CP1P2 12 3 47.402F
CTRENCH 1 20 33.198F
RBX 2 12 7.424 TC=2.556M
RCX 1 10 10.819 TC=1.887M,168.060N
RCI 10 11 2.705 TC=1.887M,168.060N
REX 13 3 1.130 TC=192.895U
RSUB 20 21 2.392K
QP 20 10 12 20 TXP 2 OFF
```

```
QN 11 12 13 11 TX 2
.MODEL TX NPN( IS=5.518E-017 XTI=3 EG=1.155 BF=331.407 BR=36 XTB=0
+   VAF=100 VAR=2 NF=1.018 NR=1.018 NE=2 NC=1.560 IKF=182.120M
+   IKR=4.455M ISE=3.564F ISC=1.604E-029 RB=3.712 RBM=2.784 IRB=16.038M
+   CJE=87.348F MJE=463M VJE=1.040 FC=990M CJC=57.150F MJC=400M VJC=890M
+   TF=2.631P TR=19N XTF=100 VTF=5 ITF=524.080M PTF=5 KF=9.000E-016
+   AF=1.500 )
.MODEL TXP PNP( IS=4.579E-019 CJE=5.773E-016 MJE=400M VJE=890M
+   CJC=34.020F MJC=460M VJC=790M BF=10K BR=139.245M TF=1N FC=900M )
.ENDS N14E062

.SUBCKT DESD 1 2 21
CP1EPI 1 4 8.743F
QD 5 4 1 5 QESD
*dd 1 4 dcb : area=count
*ds 5 4 dsub : area=count
RS 4 2 32.058 TC=2.813M,2.043U
RSUB 5 21 16.621K
CTRENCH 2 5 6.455F
.MODEL QESD PNP( IS=6.109E-019 NF=1.050 BF=800M BR=600U CJE=12.463F
+   VJE=640M MJE=330M CJC=5.346F VJC=790M MJC=460M )
.ENDS DESD

.SUBCKT PADESD100 2 3 4 5
CXP1 2 5 50F
XQ1 2 3 5 DE381011
XQ2 4 2 5 DE381011
.ENDS PADESD100

.SUBCKT DE381011 1 2 21
CP1EPI 1 4 132.715F
QD 5 4 1 5 QESD
RS 4 2 2.024 TC=2.615M,1.746U
RSUB 5 21 2.318K
CTRENCH 2 5 38.731F
.MODEL QESD PNP( IS=1.080E-017 NF=1.050 BF=800M BR=600U CJE=220.280F
+   VJE=640M MJE=330M CJC=75.512F VJC=790M MJC=460M )
.ENDS DE381011
*
*
*
.PRINT TRAN V(2001) V(2002)
*.PROBE
*
.END
```

7.2 Input Netlist

```
INPUT -  MAX3801 EQUALIZER INPUT CIRCUIT
*
* THIS IS THE TYPICAL CML INPUT OF THE MAX3800 EQUALIZER
*
.OPTIONS ACCT NOMOD NOPAGE LIMPTS=10000 RELTOL=.001
.WIDTH OUT=80
.TEMP 80
* TYPICAL DIE TEMP = 25C + 2.2W*(26C/W) = 79C
*
* INPUT SIGNALS +IN = 2101, -IN = 2102
.OP
.TRAN 5PS 1.3NS
VCC 101 0 DC 3.3
* The power supply is 3.3Volts.
*
VINA 2 0 PULSE (3.3 2.5 0.2n 0.075n 0.075n 0.250n 0.620n)
VINB 3 0 PULSE (2.5 3.3 0.2n 0.075n 0.075n 0.250n 0.620n)
RLOAD1 2 2101 50
CLOAD1 101 2101 0.2p
RLOAD2 3 2102 50
CLOAD2 101 2102 0.2p
CLOAD3 2101 2102 0.05p
*
XPK1 2101 2102 8 9 0 0 0 INPKG
*
XCIROUT 8 9 101 INBUF
*
.SUBCKT INBUF 1001 1002 101
*
*
XQ3 101 1001 4 0 N12A04
XQ4 101 1002 5 0 N12A04
*
R1 1 1001 50
R2 1 1002 50
*
IE3 4 0 0.20M
IE4 5 0 0.20M
*
XPAD1 1001 101 0 0 PADESD100
XPAD2 1002 101 0 0 PADESD100
*
.ENDS INBUF
*
*
.SUBCKT INPKG 1101 1102 1201 1202 110 111 112
*
* resistors
*
R02 1201 1203 400M
R03 1202 1204 400M
*
* inductors
*
L02 1101 1203 1.4N
L03 1102 1204 1.4N
*
* capacitors
*
```

```
C01 1101 0 115F
C02 1102 0 114F
*
* mutual capacitors
*
C12 1101 1102 70.000F
.ENDS INPKG
*
*
*BEGIN PROCESS MODELS
*
.SUBCKT N11A03 1 2 3 21
CP1EPI 10 12 3.539F
CP1P2 12 3 2.985F
CTRENCH 1 20 6.455F
RBX 2 12 118.779 TC=2.556M
RCX 1 10 58.217 TC=2.576M,499.699N
RCI 10 11 14.554 TC=2.576M,499.699N
REX 13 3 18.075 TC=192.895U
RSUB 20 21 16.621K
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
.MODEL TX NPN( IS=6.897E-018 XTI=3 EG=1.155 BF=331.407 BR=36 XTB=0
+   VAF=100 VAR=2 NF=1.018 NR=1.018 NE=2 NC=1.560 IKF=22.765M
+   IKR=556.875U ISE=4.455E-016 ISC=2.005E-030 RB=29.695 RBM=22.271
+   IRB=2.005M CJE=10.919F MJE=463M VJE=1.040 FC=990M CJC=7.144F
+   MJC=400M VJC=890M TF=2.631P TR=19N XTF=100 VTF=5 ITF=65.510M PTF=5
+   KF=9.000E-016 AF=1.500 )
.MODEL TXP PNP( IS=5.724E-020 CJE=7.216E-017 MJE=400M VJE=890M
+   CJC=5.346F MJC=460M VJC=790M BF=10K BR=55.381M TF=1N FC=900M )
.ENDS N11A03
*
.SUBCKT N12A04 1 2 3 21
CP1EPI 10 12 8.626F
CP1P2 12 3 7.236F
CTRENCH 1 20 9.222F
RBX 2 12 36.927 TC=2.542M
RCX 1 10 37.004 TC=2.053M,235.845N
RCI 10 11 9.251 TC=2.053M,235.845N
REX 13 3 6.092 TC=303.554U
RSUB 20 21 10.427K
QP 20 10 12 20 TXP OFF
QN 11 12 13 11 TX
.MODEL TX NPN( IS=2.299E-017 XTI=3 EG=1.155 BF=315.986 BR=36 XTB=0
+   VAF=100 VAR=2 NF=1.018 NR=1.018 NE=2 NC=1.560 IKF=75.884M IKR=1.856M
+   ISE=1.485F ISC=6.683E-030 RB=9.232 RBM=6.924 IRB=6.683M CJE=36.362F
+   MJE=463M VJE=1.040 FC=990M CJC=21.321F MJC=400M VJC=890M TF=2.668P
+   TR=19N XTF=100 VTF=5 ITF=215.178M PTF=5 KF=9.000E-016 AF=1.500 )
.MODEL TXP PNP( IS=1.728E-019 CJE=2.154E-016 MJE=400M VJE=890M
+   CJC=11.360F MJC=460M VJC=790M BF=10K BR=78.677M TF=1N FC=900M )
.ENDS N12A04
*
.SUBCKT N14E062 1 2 3 21
CP1EPI 10 12 54.836F
CP1P2 12 3 47.402F
CTRENCH 1 20 33.198F
RBX 2 12 7.424 TC=2.556M
RCX 1 10 10.819 TC=1.887M,168.060N
RCI 10 11 2.705 TC=1.887M,168.060N
REX 13 3 1.130 TC=192.895U
RSUB 20 21 2.392K
QP 20 10 12 20 TXP 2 OFF
QN 11 12 13 11 TX 2
```

```
.MODEL TX NPN( IS=5.518E-017 XTI=3 EG=1.155 BF=331.407 BR=36 XTB=0
+   VAF=100 VAR=2 NF=1.018 NR=1.018 NE=2 NC=1.560 IKF=182.120M
+   IKR=4.455M ISE=3.564F ISC=1.604E-029 RB=3.712 RBM=2.784 IRB=16.038M
+   CJE=87.348F MJE=463M VJE=1.040 FC=990M CJC=57.150F MJC=400M VJC=890M
+   TF=2.631P TR=19N XTF=100 VTF=5 ITF=524.080M PTF=5 KF=9.000E-016
+   AF=1.500 )
.MODEL TXP PNP( IS=4.579E-019 CJE=5.773E-016 MJE=400M VJE=890M
+   CJC=34.020F MJC=460M VJC=790M BF=10K BR=139.245M TF=1N FC=900M )
.ENDS N14E062
*
.SUBCKT DESD 1 2 21
CP1EPI 1 4 8.743F
QD 5 4 1 5 QESD
*dd 1 4 dcb : area=count
*ds 5 4 dsub : area=count
RS 4 2 32.058 TC=2.813M,2.043U
RSUB 5 21 16.621K
CTRENCH 2 5 6.455F
.MODEL QESD PNP( IS=6.109E-019 NF=1.050 BF=800M BR=600U CJE=12.463F
+   VJE=640M MJE=330M CJC=5.346F VJC=790M MJC=460M )
.ENDS DESD
*
.SUBCKT PADESD100 2 3 4 5
CXP1 2 5 50F
XQ1 2 3 5 DE381011
XQ2 4 2 5 DE381011
.ENDS PADESD100
*
.SUBCKT DE381011 1 2 21
CP1EPI 1 4 132.715F
QD 5 4 1 5 QESD
RS 4 2 2.024 TC=2.615M,1.746U
RSUB 5 21 2.318K
CTRENCH 2 5 38.731F
*
.MODEL QESD PNP( IS=1.080E-017 NF=1.050 BF=800M BR=600U CJE=220.280F
+   VJE=640M MJE=330M CJC=75.512F VJC=790M MJC=460M )
.ENDS DE381011
*
*
*
*
.PRINT TRAN  V(8) V(9)
*.PROBE
.EN
```